

Table 1. 4-Level Control Pin Settings

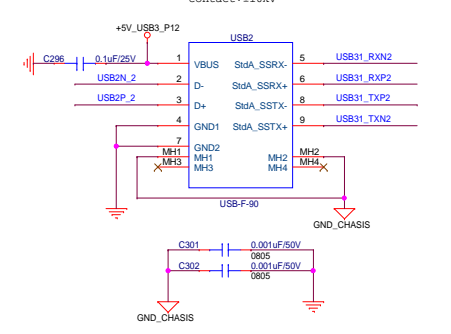
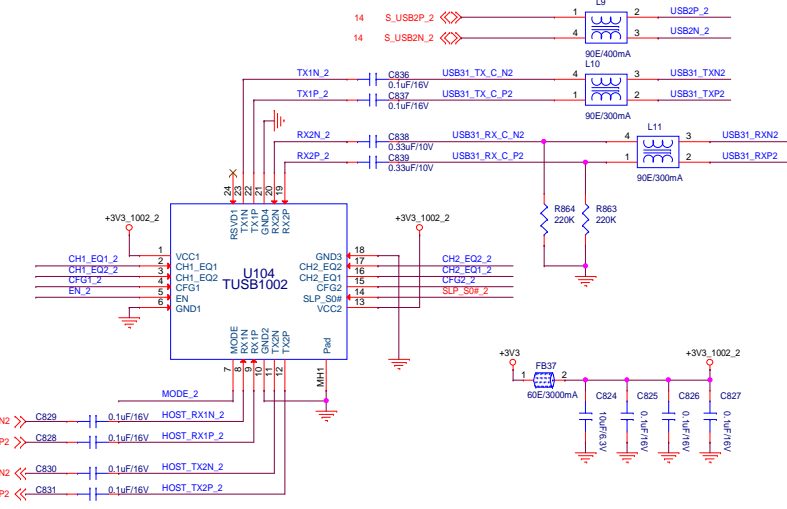
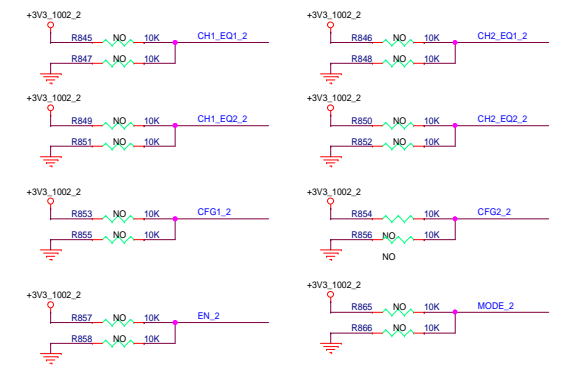
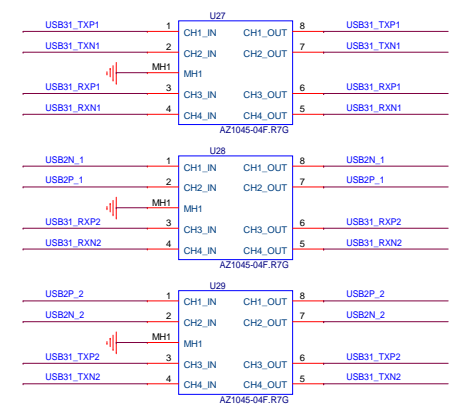
LEVEL	SETTINGS
0	Option 1: Tie 1 KΩ 5% to GND. Option 2: Tie directly to GND.
R	Tie 20 KΩ 5% to GND.
F	Float (leave pin open)
1	Option 1: Tie 1 KΩ 5% to V _{CC} . Option 2: Tie directly to V _{CC} .

Table 2. EQ Configuration Options for 1200mV Linearity 0 dB DC Gain Setting

EQ SETTING #	CHx_EQ2 PIN LEVEL	CHx_EQ1 PIN LEVEL	EQ GAIN at 2.5GHz / 5 GHz (dB)
1	0	0	1.9 / 5.5
2	0	R	2.8 / 7.1
3	0	F	3.5 / 8.2
4	0	1	4.4 / 9.3
5	R	0	5.0 / 10.2
6	R	R	5.8 / 11.1
7	R	F	6.4 / 11.8
8	R	1	7.1 / 12.6
9	F	0	7.6 / 13.1
10	F	R	8.2 / 13.8
11	F	F	8.7 / 14.3
12	F	1	9.2 / 14.8
13	1	0	9.6 / 15.2
14	1	R	10.1 / 15.6
15	1	F	10.4 / 16.0
16	1	1	10.6 / 16.3

Table 3. VOD Linear Range and DC Gain

SETTING #	CFG1 PIN LEVEL	CFG2 PIN LEVEL	CH1 DC GAIN (dB)	CH2 DC GAIN (dB)	CH1 V _{OD} LINEAR RANGE (mVpp)	CH2 V _{OD} LINEAR RANGE (mVpp)
1	0	0	+1	0	900	900
2	0	R	0	+1	900	900
3	0	F	0	0	900	900
4	0	1	+1	+1	900	900
5	R	0	0	0	1000	1000
6	R	R	+1	0	1000	1000
7	R	F	0	-1	1000	1000
8	R	1	+2	+2	1000	1000
9	F	0	-1	-1	1200	1200
10	F	R	0	-2	1200	1200
11	F	F	0	0	1200	1200
12	F	1	+1	+1	1200	1200
13	1	0	-1	0	1200	1200
14	1	R	0	-1	1200	1200
15	1	F	0	+1	1200	1200
16	1	1	+1	0	1200	1200



- 14 S_USB31_TXN2 >> C829 | 0.1uF/16V | HOST_RX1N_2
- 14 S_USB31_TXP2 >> C828 | 0.1uF/16V | HOST_RX1P_2
- 14 S_USB31_RXN2 >> C830 | 0.1uF/16V | HOST_TX2N_2
- 14 S_USB31_RXP2 >> C831 | 0.1uF/16V | HOST_TX2P_2