Schematic Review Form

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Pin #	Name	Info	Violations	*Description*
1, 13	VCC	10uF, 2 0.1uF bypass caps.		3.3 V (±10%) Supply.
2	CH1_EQ1	Floating		CH1_EQ1. Configuration pin used to control Rx EQ level for RX1P/N. The state of this pin is sampled after the rising edge of EN. This pin along with CH1_EQ2 allows for up to 16 equalization settings
3	CH1_EQ2	Floating		CH1_EQ2. Configuration pin used to control Rx EQ level for RX1P/N. The state of this pin is sampled after the rising edge of EN. This pin along with CH1_EQ1 allows for up to 16 equalization settings.
4	CFG1	Floating		This pin along with CFG2 will select VOD linearity range and DC gain for both channels 1 and 2. The state of this pin is sampled after the rising edge of EN.
5	EN	Pulled up with 20K		EN. Places TUSB1002A into shutdown mode when asserted low. Normal operation when pin is asserted high. When in shutdown, TUSB1002A's receiver terminations will be high impedance and tx/rx channels will be disabled.
6, 10, 18, 21	GND	Ground		Ground
7	MODE	Floating, USB3.2x1 Dual channel		MODE. This pin is for selecting different modes of operation. The state of this pin is sampled after the rising edge of EN. Refer to Figure 6-2 for details of timing. 0 = Basic Redriver Mode.

				R = PCIe / Test Mode. PCIe Mode and TI Internal use only F = USB3.2 x1 Dual Channel Operation enabled (TUSB1002A normal mode). 1 = USB3.2 x1 Single-channel operation.
8	RX1N	Connected off page		Differential input for SuperSpeed (SS) and SuperSpeedPlus (SSP) negative signals for Channel 1
9	RX1P	Connected off page		Differential input for SuperSpeed (SS) and SuperSpeedPlus (SSP) positive signals for Channel 1
11	TX2N	Connected off page	Place 100nF AC coupling capacitor near TX side	Differential output for SuperSpeed (SS) and SuperSpeedPlus (SSP) negative signals for Channel 2
12	TX2P	Connected off page	Place 100nF AC coupling capacitor near TX side	Differential output for SuperSpeed (SS) and SuperSpeedPlus (SSP) positive signals for Channel 2
14	DCBOOST#	Floating		DCBOOST#. This pin when asserted low will increase the DC Gain level defined in Table 7-3 by +1 dB unless already at +2dB. If DC Gain level defined in Table 7-3 is already at +2 dB, then asserting this pin low will not change the DC Gain level. This pin can be left unconnected if this function is not needed. 1 = DC Gain defined by Table 7-3. 0 = DC Gain defined by Table 7-3 is increased by +1 dB.
15	CFG2	Floating		This pin along with CFG1 will set VOD linearity range and DC gain for both channels 1 and 2. The state of this pin is sampled after the rising edge of EN.
16	CH2_EQ1	Floating		Configuration pin used to control Rx EQ level for RX2P/N. The state of this pin is sampled after the

				rising edge of EN. This pin along with CH2_EQ2 allows for up to 16 equalization settings.
17	CH2_EQ2	Floating		Configuration pin used to control Rx EQ level for RX2P/N. The state of this pin is sampled after the rising edge of EN. This pin along with CH2_EQ1 allows for up to 16 equalization settings.
19	RX2P	Connected off page through 100nF capacitor	Use 330nF capacitor on receiving side	Differential input for SuperSpeed (SS) and SuperSpeedPlus (SSP) positive signals for Channel 2
20	RX2N	Connected off page through 100nF capacitor	Use 330nF capacitor on receiving side	Differential input for SuperSpeed (SS) and SuperSpeedPlus (SSP) negative signals for Channel 2.
22	TX1P	Connected off page through 100nF capacitor		Differential output for SuperSpeed (SS) and SuperSpeedPlus (SSP) positive signals for Channel 1.
23	TX1N	Connected off page through 100nF capacitor		Differential output for SuperSpeed (SS) and SuperSpeedPlus (SSP) negative signals for Channel 1.
24	RSVD1	NC		RSVD1. Under normal operation, this pin will be driven low by TUSB1002A. Recommend leaving this pin unconnected on PCB.

Comments