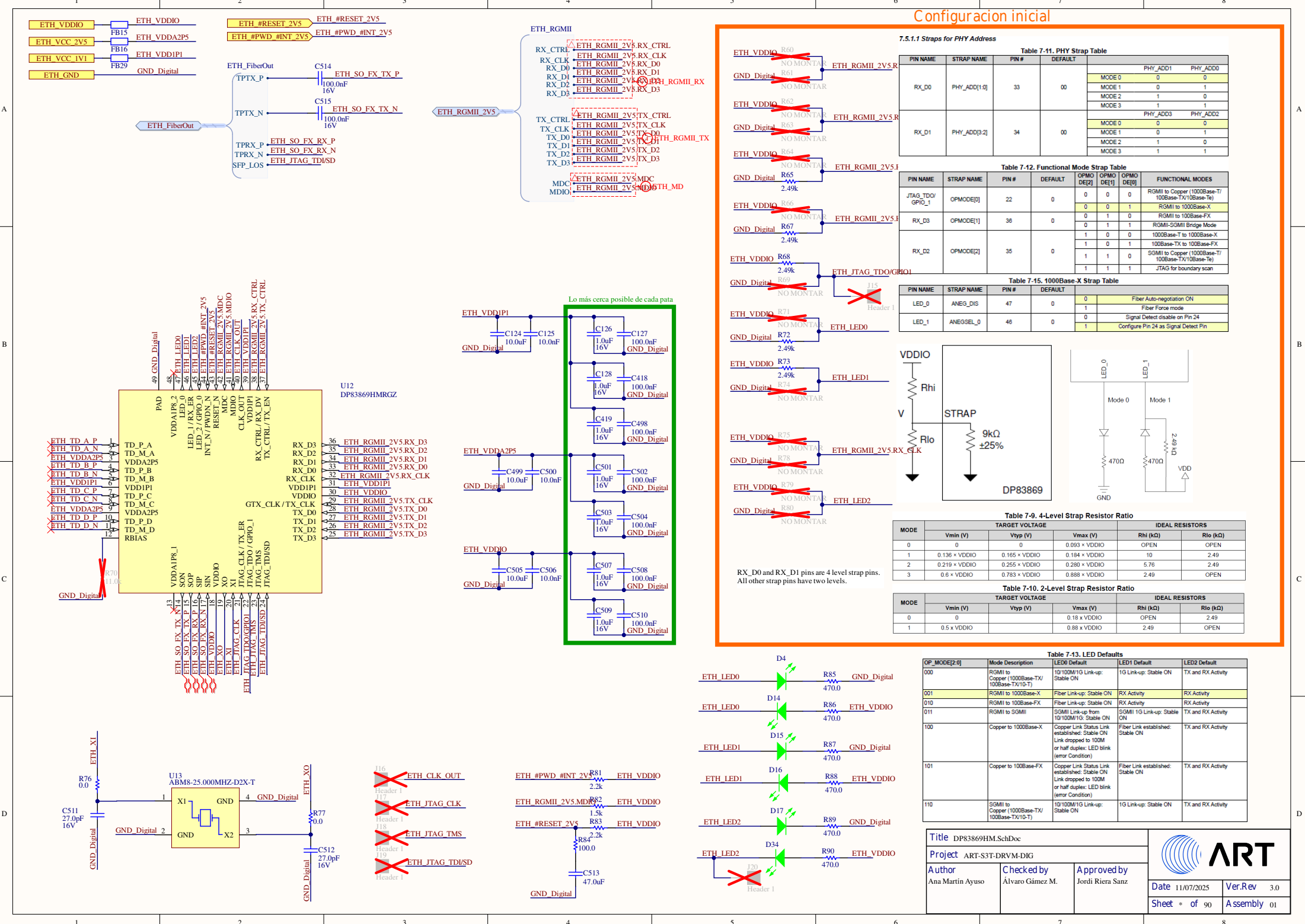




Configuracion inicial

7.5.1.1 Straps for PHY Address

Table 7-11. PHY Strap Table					
PIN NAME	STRAP NAME	PIN #	DEFAULT	PHY_ADD1	PHY_ADD0
RX_D0	PHY_ADD[1:0]	33	00	MODE 0	0
				MODE 1	0
				MODE 2	1
				MODE 3	1
RX_D1	PHY_ADD[3:2]	34	00	PHY_ADD3	PHY_ADD2
				MODE 0	0
				MODE 1	0
				MODE 2	1

Table 7-12. Functional Mode Strap Table					
PIN NAME	STRAP NAME	PIN #	DEFAULT	OPMODE DE[2]	OPMODE DE[1]
JTAG_TDO/GPIO_1	OPMODE[0]	22	0	0	0
RX_D3	OPMODE[1]	36	0	0	1
				0	1
				1	0
				1	0
RX_D2	OPMODE[2]	35	0	1	1
				1	1
				1	1
				1	1

Table 7-15. 1000Base-X Strap Table					
PIN NAME	STRAP NAME	PIN #	DEFAULT	LED_0	LED_1
LED_0	ANEG_DIS	47	0	0	1
LED_1	ANEGSEL_0	46	0	0	1

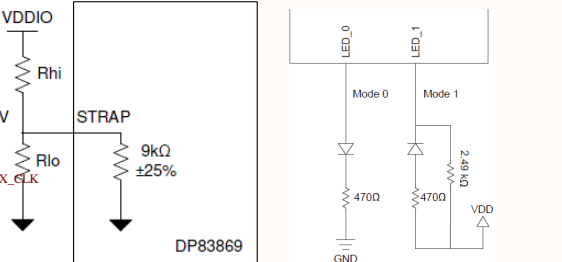


Table 7-9. 4-Level Strap Resistor Ratio					
MODE	Vmin (V)	Vtyp (V)	Vmax (V)	Rhi (kΩ)	Rlo (kΩ)
0	0	0	0.093 × VDDIO	OPEN	OPEN
1	0.136 × VDDIO	0.165 × VDDIO	0.184 × VDDIO	10	2.49
2	0.219 × VDDIO	0.255 × VDDIO	0.280 × VDDIO	5.76	2.49
3	0.6 × VDDIO	0.783 × VDDIO	0.888 × VDDIO	2.49	OPEN

Table 7-10. 2-Level Strap Resistor Ratio					
MODE	Vmin (V)	Vtyp (V)	Vmax (V)	Rhi (kΩ)	Rlo (kΩ)
0	0	0	0.18 × VDDIO	OPEN	2.49
1	0.5 × VDDIO	0.88 × VDDIO	0.88 × VDDIO	2.49	OPEN

Table 7-13. LED Defaults					
OP_MODE[2:0]	Mode Description	LED0 Default	LED1 Default	LED2 Default	
000	RGMII to Copper (1000Base-TX/100Base-TX/10-T)	1G Link-up: Stable ON	1G Link-up: Stable ON	TX and RX Activity	
001	RGMII to 1000Base-X	Fiber Link-up: Stable ON	RX Activity	RX Activity	
010	RGMII to 1000Base-FX	Fiber Link-up: Stable ON	RX Activity	RX Activity	
011	RGMII to SGMII	SGMII 1G Link-up from 10/100M/1G: Stable ON	SGMII 1G Link-up: Stable ON	TX and RX Activity	
100	Copper to 1000Base-X	Copper Link Status Link established: Stable ON Link dropped to 100M or half duplex: LED blink (error Condition)	Fiber Link established: Stable ON	TX and RX Activity	
101	Copper to 100Base-FX	Copper Link Status Link established: Stable ON Link dropped to 100M or half duplex: LED blink (error Condition)	Fiber Link established: Stable ON	TX and RX Activity	
110	SGMII to Copper (1000Base-TX/100Base-TX/10-T)	1G Link-up: Stable ON	1G Link-up: Stable ON	TX and RX Activity	

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Author Ana Martín Ayuso	Checked by Álvaro Gámez M.	Approved by Jordi Riera Sanz	
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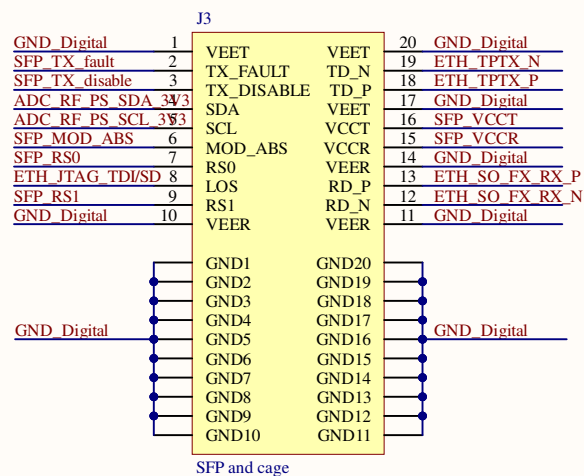
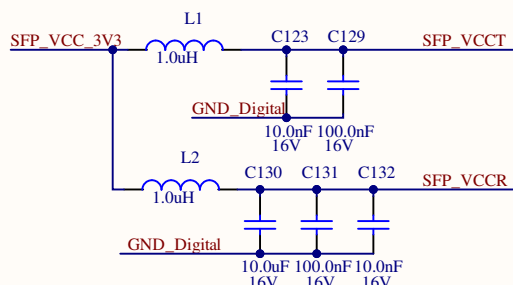
SFP_VCC_3V3 SFP_VCC_3V3
SFP_GND GND_Digital

ETH_FiberOut

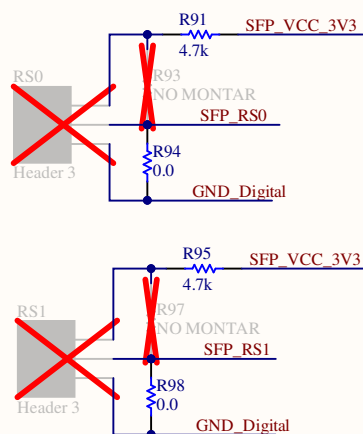
ETH_FiberOut
TPTX_P ETH_TPTX_P
TPTX_N ETH_TPTX_N
TPRX_P ETH_SO_FX_RX_P
TPRX_N ETH_SO_FX_RX_N
SFP_LOS ETH_JTAG_TDI/SD

SFP_I2C_3V3

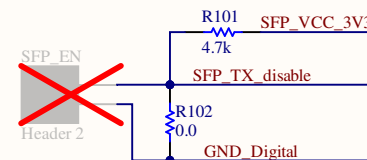
I2C_3V3
SCL_3V3 ADC_RF_PS_SCL_3V3
SDA_3V3 ADC_RF_PS_SDA_3V3



SFP and cage

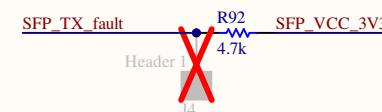


RS0: GND -> Low BW RX
VCC -> Full BW RX
RS1: GND -> Low BW TX
VCC -> Full BW TX



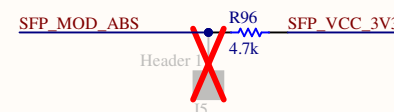
SFP_TX_DISABLE:

GND -> Transmitter on
VCC -> Transmitter off

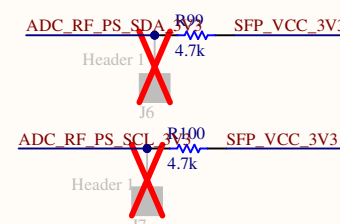


SFP_TX_FAULT indicates:

GND -> NORMAL OPERATION
HIGH -> FAULT



SFP_MOD_ABS: grounded by the module to indicate that the module is present



SFP_SDA: data line of two wire serial interface for serial ID
SFP_SCL: clock line of two wire serial interface for serial ID



SFP_LOS indicates:

GND -> NORMAL OPERATION
HIGH -> received optical power is below the worst-case receiver sensitivity

Title Eth_SFP.SchDoc

Project ART-S3T-DRVM-DIG

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Date 11/07/2025

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