HD3SS3220 USB Type-C DRP Port Controller with SuperSpeed 2:1 MUX

1 Features

- USB Type-C Port Controller with Integrated 2:1 SuperSpeed Mux
- Compatible to USB Type-C™ Specifications
- Supports USB 3.1 G1 and G2 up to 10 Gbps
- Supports up to 15 W of Power Delivery with 3-A Current Advertisement and Detection
- Mode Configuration
  - Host Only – DFP/Source
  - Device Only – UFP/Sink
  - Dual Role Port - DRP
- Channel Configuration (CC)
  - Attach of USB Port Detection
  - Cable Orientation Detection
  - Role Detection
  - Type-C Current Mode (Default, Mid, High)
- $V_{(BUS)}$ Detection and VCONN Support for Active Cables
- Audio and Debug Accessory Support
- Supports for Try.SRC and Try.SNK DRP Modes
- Configuration Control through GPIO and I^2C
- Low Active and Standby Current Consumptions
- Industrial Temperature Range of –40 to 85°C

2 Applications

- USB Host, Device, Hub
- Mobile Phones, Tablets and Notebooks
- USB Peripherals such as Thumb Drives, Portable Hard Disks, Set Top Box

3 Description

HD3SS3220 is a USB SuperSpeed (SS) 2:1 mux with DRP port controller. The device provides Channel Configuration (CC) logic and 5V VCONN sourcing for ecosystems implementing USB Type-C. The HD3SS3220 can be configured as a Downstream Facing Port (DFP), Upstream Facing Port (UFP) or a Dual Role Port (DRP) making it ideal for any application.

The HD3SS3220, in DRP mode, alternates presenting itself as a DFP or UFP according to the Type-C specifications. The CC logic block monitors the CC1 and CC2 pins for pull-up or pull-down resistances to determine when a USB port has been attached and its port role. Once a USB port has been attached, the CC logic also determines the orientation of the cable and configures the USB SS mux accordingly. Finally, CC logic advertises or detects Type-C current mode – Default, Mid, or High in DFP and UFP modes respectively.

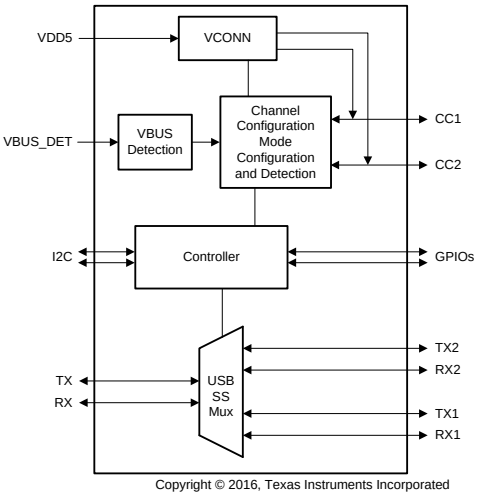
Excellent dynamic characteristics of the integrated mux allow switching with minimum attenuation to the SS signal eye diagram and very little added jitter. The device's switch paths deploy adaptive common mode voltage tracking resulting identical channel despite different common mode voltage for RX and TX channels.

Device Information(1)

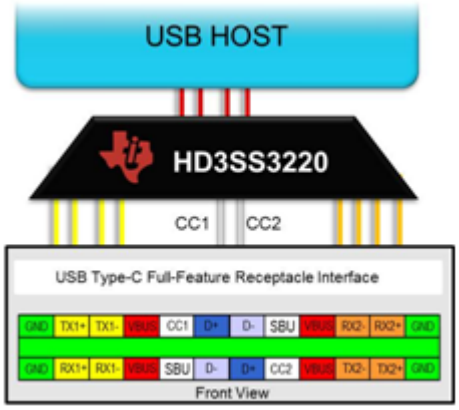
PART NUMBER	PACKAGE	BODY SIZE (NOM)
HD3SS3220	VQFN RNH (30)	2.50 mm x 4.50 mm
HD3SS3220I		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



Typical Application



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4 Revision History

Changes from Revision B (September 2016) to Revision C **Page**

- Added R_{VBUS} values: MIN = 855, TYP = 887, MAX = 920 KΩ ... 7

Changes from Revision A (August 2016) to Revision B **Page**

- Changed pins CC1 and CC2 values From: MIN = –0.3 MAX = VDD5 +0.3 To: MIN –0.3 MAX = 6 in the *Absolute Maximum Ratings* ... 5

Changes from Original (December 2016) to Revision A **Page**

- *Absolute Maximum Ratings*, Deleted "ENn_MUX" from the Control Pins ... 5
- *ESD Ratings*, Deleted text "Pins listed as ±XXX V may actually have higher performance." from Note 1 ... 5
- *Recommended Operating Conditions*, Added "VDD5 supply ramp time" ... 5
- *Recommended Operating Conditions*, Changed "External resistor on VBUS_DET pin" MIN value From: 890 KΩ To: 880 KΩ ... 5
- Switch the position of CC1 and CC2 in Figure 10 ... 24
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- Switch the position of CC1 and CC2 in Figure 12 ... 28

7.6.4 General Control Register (offset = 0x0A) [reset = 0x00]

Figure 8. General Control Register

7	6	5	4	3	2	1	0
DEBOUNCE		MODE_SELECT		I2C_SOFT _RESET	SOURCE_PREF		DISABLE _TERM
R/W		R/W		R/U	R/W		R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. General Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	DEBOUNCE	R/W	2'b00	The nominal amount of time the HD3SS3220 debounces the voltages on the CC pins. 00 – 168 ms (Default) 01 – 118 ms 10 – 134 ms 11 – 152 ms
5:4	MODE_SELECT	R/W	2'b00	This register can be written to set the HD3SS3220 mode operation. The ADDR pin must be set to I^2C mode. If the default is maintained, HD3SS3220 shall operate according to the PORT pin levels and modes. The MODE_SELECT can only be changed when in the unattached state. 00 – DRP mode (start from unattached.SNK) (default) 01 – UFP mode (unattached.SNK) 10 – DFP mode (unattached.SRC) 11 – DRP mode (start from unattached.SNK)
3	I2C_SOFT _RESET	R/U	1'b0	This register resets the digital logic. The bit is self-clearing. A write of 1 starts the reset. The following registers can be affected after setting this bit: CURRENT_MODE_DETECT ACTIVE_CABLE_DETECTION ACCESSORY_CONNECTED ATTACHED_STATE CABLE_DIR
2:1	SOURCE_PREF	R/W	2'b00	This field controls the TUSB322I behavior when configured as a DRP. 00 – Standard DRP (default) 01 – DRP performs Try.SNK 10 – Reserved 11 – DRP performs Try.SRC
0	DISABLE _TERM	R/W	1'b0	This field disables the termination on CC pins and transition the CC state machine to the disabled state. 0 – Termination enabled according TUSB322I mode of operation (default) 1 – Termination disabled and state machine held in disable state

7.6.5 Device Revision Register (offset = 0xA0) [reset = 0x02]

Figure 9. Device Revision Register

7	6	5	4	3	2	1	0
REVISION							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. Device Revision Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REVISION	R	'h02	Revision of HD3SS3220. Defaults to 0x02