

VCC_2V5 VCC_2V5
VCC_3V3 VCC_3V3

Power

C10_MUX0_I2C_3V3_SCK C10_MUX0_I2C_3V3_SCK
C10_MUX0_I2C_3V3_SDA C10_MUX0_I2C_3V3_SDA

MUX0 I2C

C10_MUX1_I2C_3V3_SCK C10_MUX1_I2C_3V3_SCK
C10_MUX1_I2C_3V3_SDA C10_MUX1_I2C_3V3_SDA

MUX1 I2C

SFP28_MUX0_ECPRI[3:0]_RX_P SFP28_MUX0_ECPRI[3:0]_RX_P
SFP28_MUX0_ECPRI[3:0]_RX_N SFP28_MUX0_ECPRI[3:0]_RX_N

CN6_MUX0_ECPRI[3:0]_RX_P CN6_MUX0_ECPRI[3:0]_RX_P
CN6_MUX0_ECPRI[3:0]_RX_N CN6_MUX0_ECPRI[3:0]_RX_N

QSFP28_MUX0_ECPRI[3:0]_RX_P QSFP28_MUX0_ECPRI[3:0]_RX_P
QSFP28_MUX0_ECPRI[3:0]_RX_N QSFP28_MUX0_ECPRI[3:0]_RX_N

CN6_MUX0_ECPRI[3:0]_TX_P CN6_MUX0_ECPRI[3:0]_TX_P
CN6_MUX0_ECPRI[3:0]_TX_N CN6_MUX0_ECPRI[3:0]_TX_N

SFP28_MUX0_ECPRI[3:0]_TX_P SFP28_MUX0_ECPRI[3:0]_TX_P
SFP28_MUX0_ECPRI[3:0]_TX_N SFP28_MUX0_ECPRI[3:0]_TX_N

QSFP28_MUX0_ECPRI[3:0]_TX_P QSFP28_MUX0_ECPRI[3:0]_TX_P
QSFP28_MUX0_ECPRI[3:0]_TX_N QSFP28_MUX0_ECPRI[3:0]_TX_N

SFP28_MUX1_ECPRI[5:0]_RX_P SFP28_MUX1_ECPRI[5:0]_RX_P
SFP28_MUX1_ECPRI[5:0]_RX_N SFP28_MUX1_ECPRI[5:0]_RX_N

PROC_MUX1_ECPRI[5:0]_RX_P PROC_MUX1_ECPRI[5:0]_RX_P
PROC_MUX1_ECPRI[5:0]_RX_N PROC_MUX1_ECPRI[5:0]_RX_N

QSFP28_MUX1_ECPRI[5:0]_RX_P QSFP28_MUX1_ECPRI[5:0]_RX_P
QSFP28_MUX1_ECPRI[5:0]_RX_N QSFP28_MUX1_ECPRI[5:0]_RX_N

PROC_MUX1_ECPRI[5:0]_TX_P PROC_MUX1_ECPRI[5:0]_TX_P
PROC_MUX1_ECPRI[5:0]_TX_N PROC_MUX1_ECPRI[5:0]_TX_N

SFP28_MUX1_ECPRI[5:0]_TX_P SFP28_MUX1_ECPRI[5:0]_TX_P
SFP28_MUX1_ECPRI[5:0]_TX_N SFP28_MUX1_ECPRI[5:0]_TX_N

QSFP28_MUX1_ECPRI[5:0]_TX_P QSFP28_MUX1_ECPRI[5:0]_TX_P
QSFP28_MUX1_ECPRI[5:0]_TX_N QSFP28_MUX1_ECPRI[5:0]_TX_N

PROC_MUX2_10G_L[1:0]_RX_P PROC_MUX2_10G_L[1:0]_RX_P
PROC_MUX2_10G_L[1:0]_RX_N PROC_MUX2_10G_L[1:0]_RX_N

CN6_MUX2_ECPRI[9:8]_10G_RX_P CN6_MUX2_ECPRI[9:8]_10G_RX_P
CN6_MUX2_ECPRI[9:8]_10G_RX_N CN6_MUX2_ECPRI[9:8]_10G_RX_N

A10_MUX2_ECPRI[9:8]_RX_P A10_MUX2_ECPRI[9:8]_RX_P
A10_MUX2_ECPRI[9:8]_RX_N A10_MUX2_ECPRI[9:8]_RX_N

U?

CN6_MUX2_ECPRI[9:8]_10G_TX_P CN6_MUX2_ECPRI[9:8]_10G_TX_P
CN6_MUX2_ECPRI[9:8]_10G_TX_N CN6_MUX2_ECPRI[9:8]_10G_TX_N

PROC_MUX2_10G_L[1:0]_TX_P PROC_MUX2_10G_L[1:0]_TX_P
PROC_MUX2_10G_L[1:0]_TX_N PROC_MUX2_10G_L[1:0]_TX_N

A10_MUX2_ECPRI[9:8]_TX_P A10_MUX2_ECPRI[9:8]_TX_P
A10_MUX2_ECPRI[9:8]_TX_N A10_MUX2_ECPRI[9:8]_TX_N

TBD
Pending

CAL_CLK_BUF_OUT[5:0]_2V5_25M CAL_CLK_BUF_OUT[5:0]_2V5_25M

C10_MUX0_[1:0]_3V3_INT_N C10_MUX0_[1:0]_3V3_INT_N

C10_MUX1_[2:0]_3V3_INT_N C10_MUX1_[2:0]_3V3_INT_N

C10_MUX2_3V3_INT_N C10_MUX2_3V3_INT_N

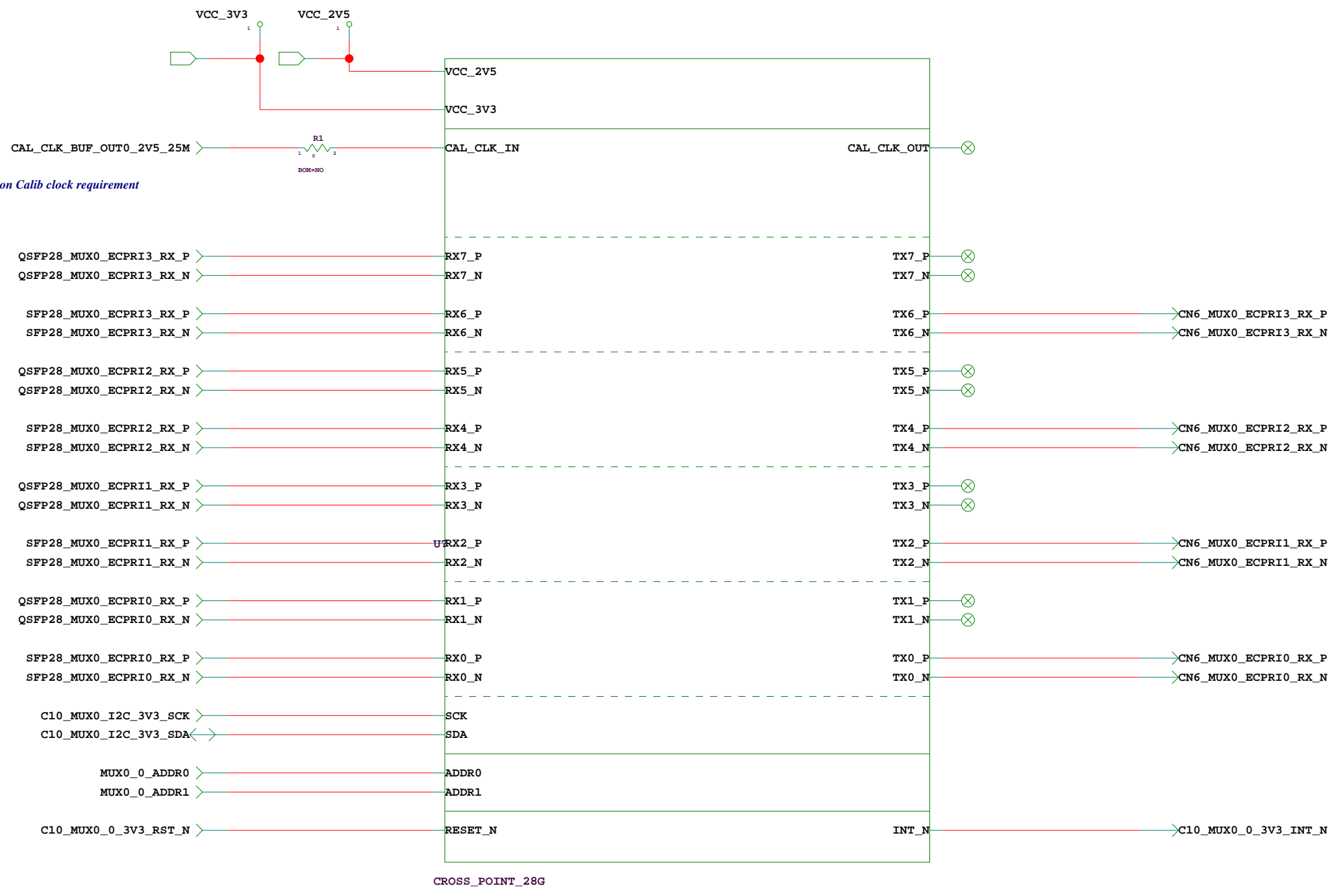
C10_MUX0_[1:0]_3V3_RST_N C10_MUX0_[1:0]_3V3_RST_N

C10_MUX1_[2:0]_3V3_RST_N C10_MUX1_[2:0]_3V3_RST_N

C10_MUX2_3V3_RST_N C10_MUX2_3V3_RST_N

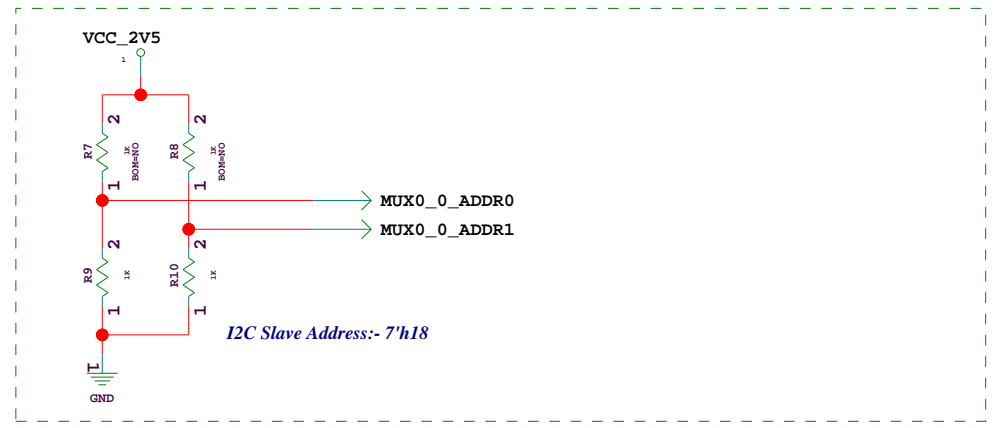
MUX_TOP

Description:		Tejas Networks	
DESCRIPTION			
Sheet 1 of 1			
Project:	PROJECT NAME	Drawn By:	DESIGNER(S)
Date:	10-7-2024_15:57	Rev:	REV
Reviewed By:		REVIEWER(S)	
PART NUMBER:		PART_NUMBER	

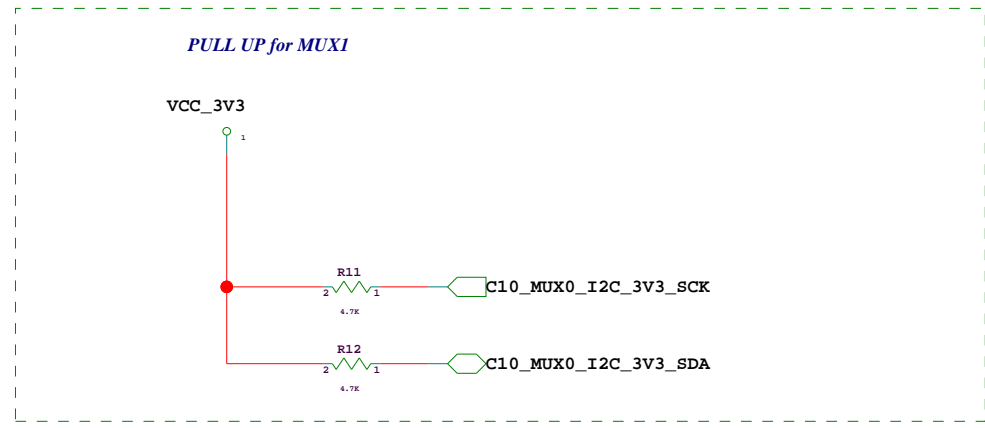


Note:- Need to Finalize on Calib clock requirement

CROSS_POINT_28G

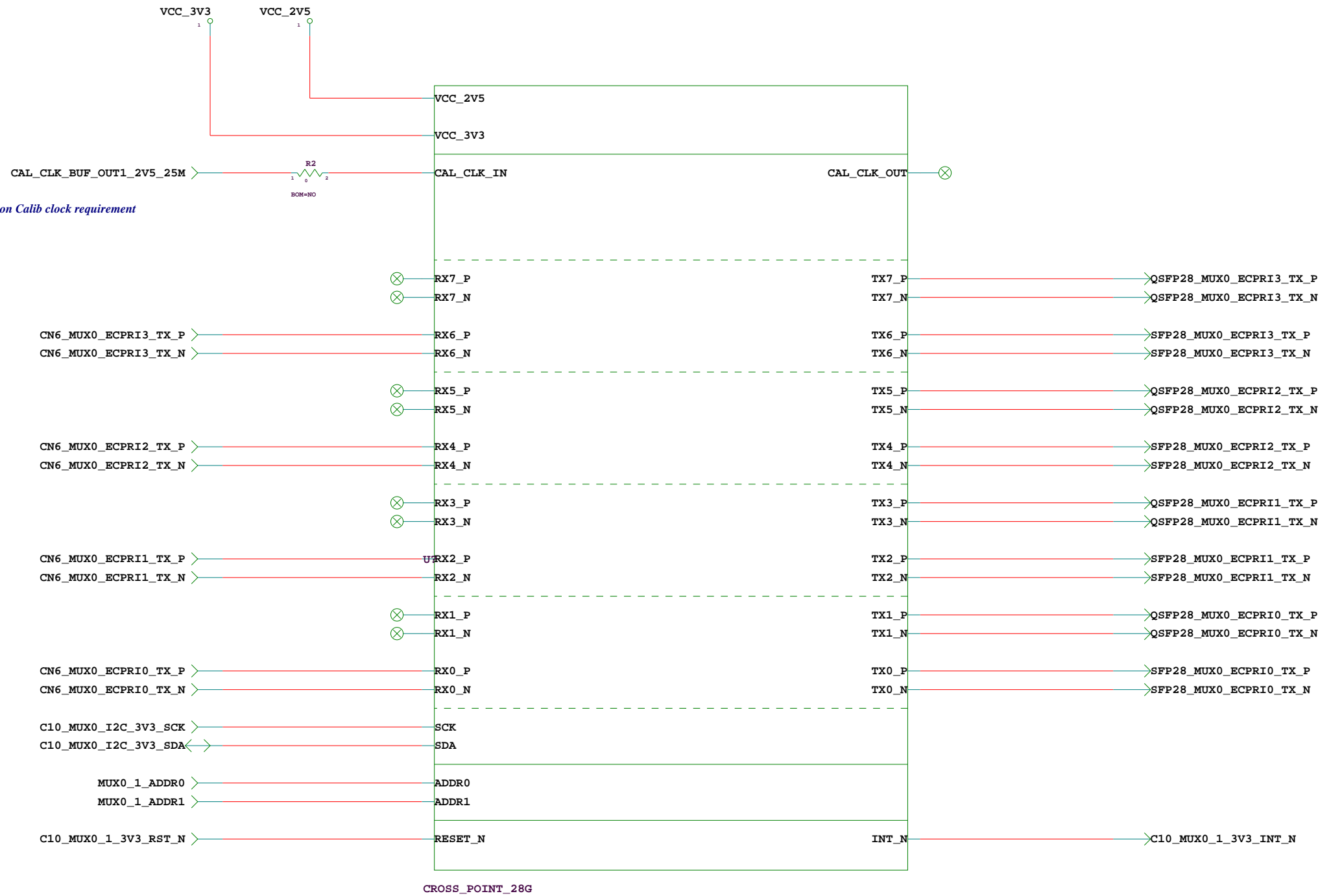


I2C Slave Address:- 7'h18

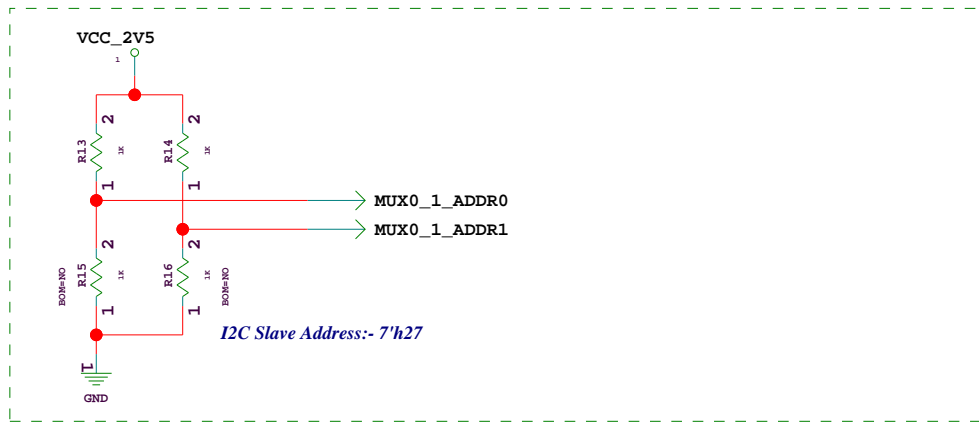


PULL UP for MUX1

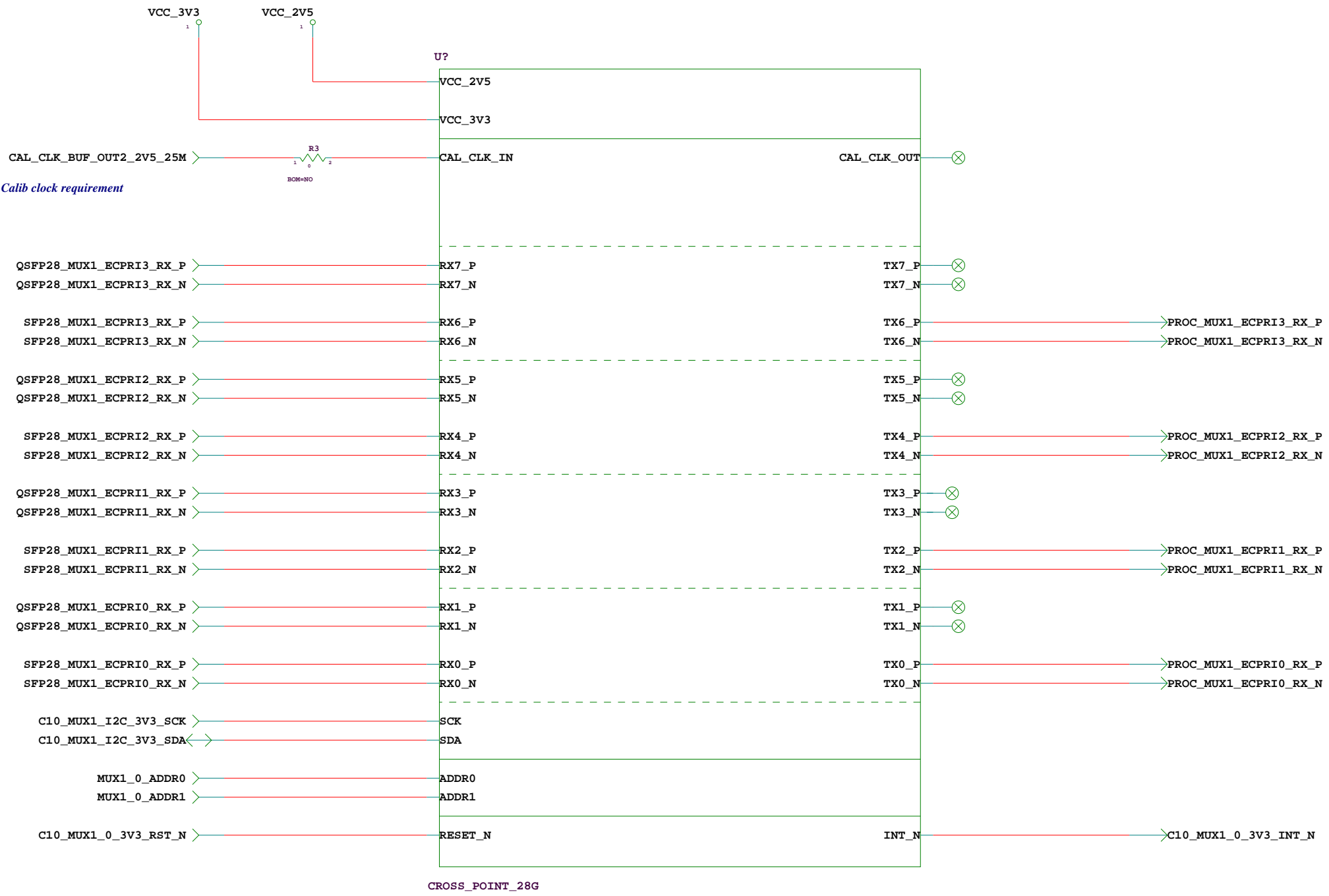
Description:		Tejas Networks	
DESCRIPTION			
Sheet 1 of 10			
Project:	PROJECT NAME	Drawn By:	DESIGNER(S)
Date:	10-7-2024_12:41	Rev:	REV
		Reviewed By:	REVIEWER(S)



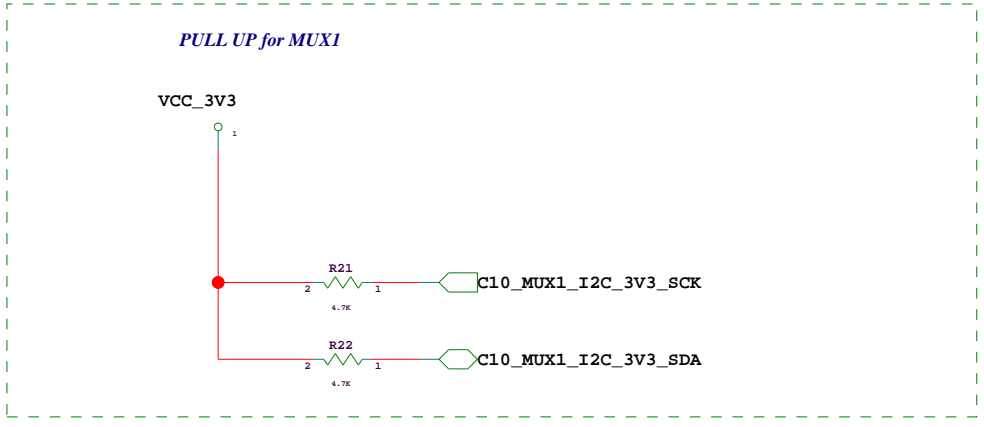
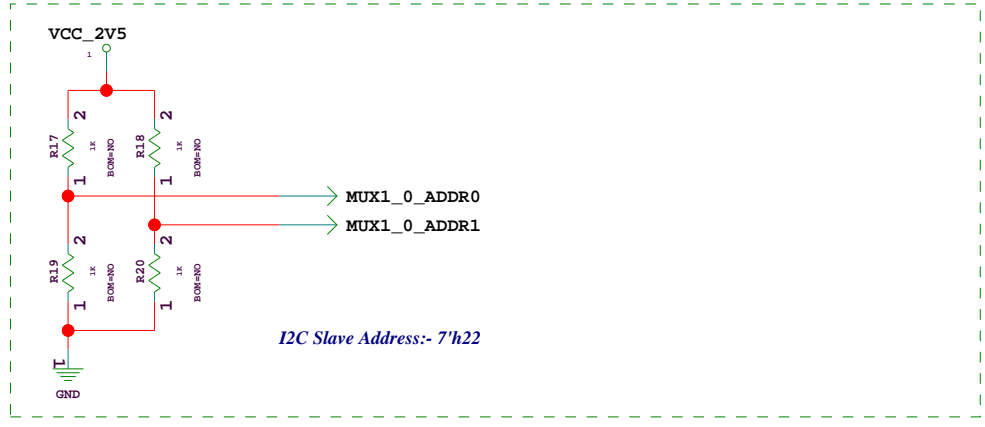
Note:- Need to Finalize on Calib clock requirement



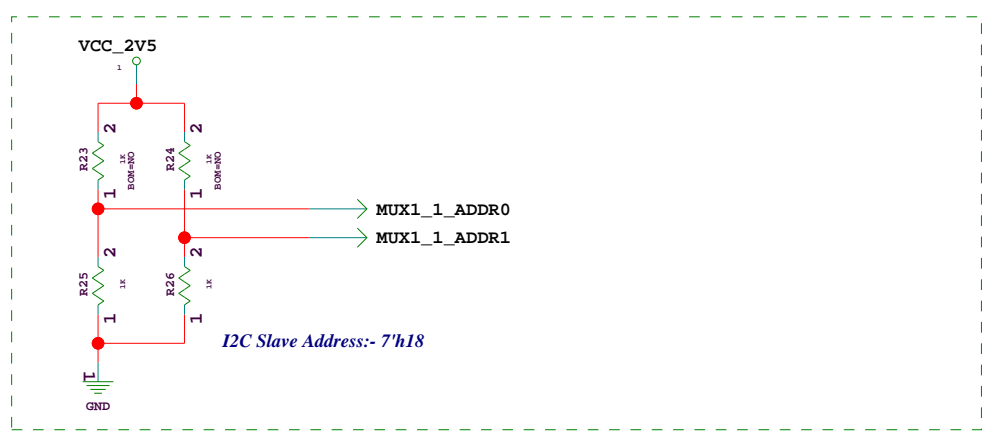
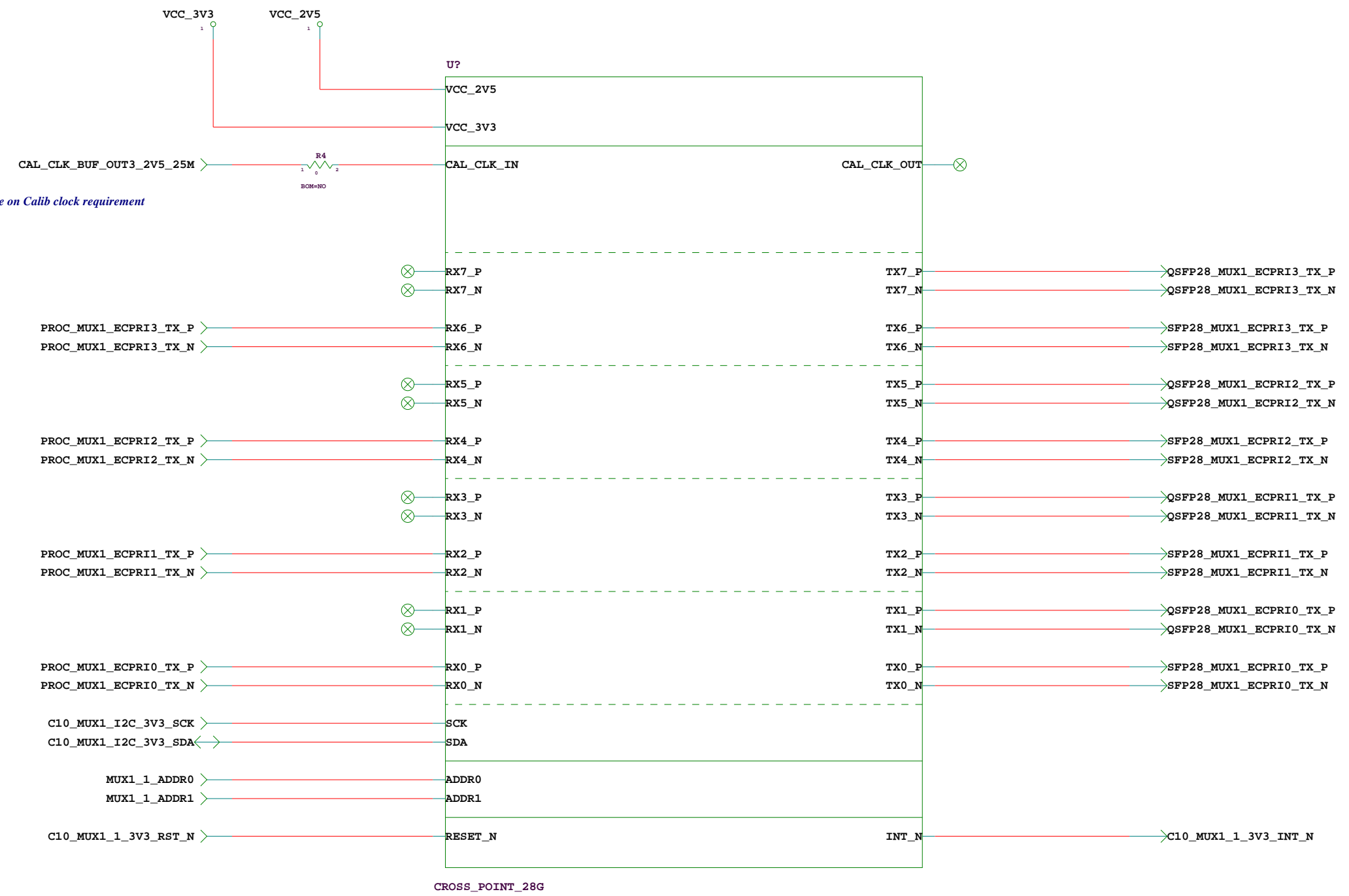
Description:		Tejas Networks	
DESCRIPTION			
		Sheet 2 of 10	
Project:	PROJECT NAME	Drawn By:	DESIGNER(S)
Date:	10-7-2024_12:41	Rev:	REV
		Reviewed By:	REVIEWER(S)



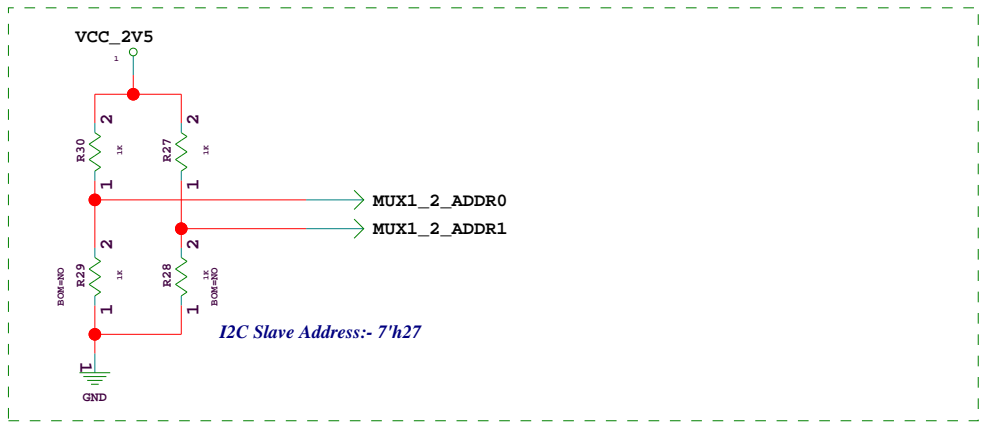
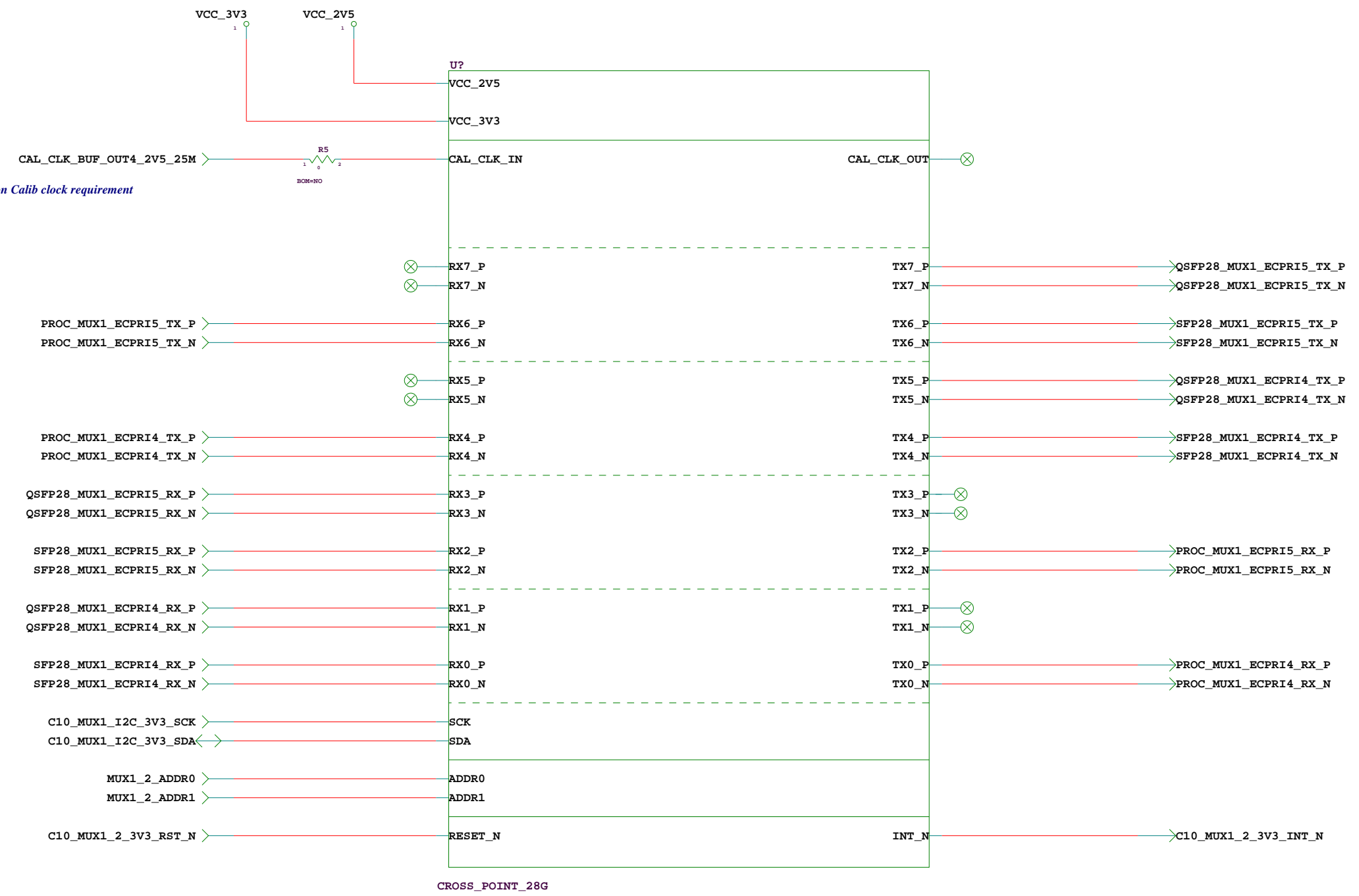
Note:- Need to Finalize on Calib clock requirement



Description:		Tejas Networks	
DESCRIPTION			
		Sheet 3 of 10	
Project:	PROJECT NAME	Drawn By:	DESIGNER(S)
Date:	10-7-2024_12:41	Rev:	REV
		Reviewed By:	REVIEWER(S)

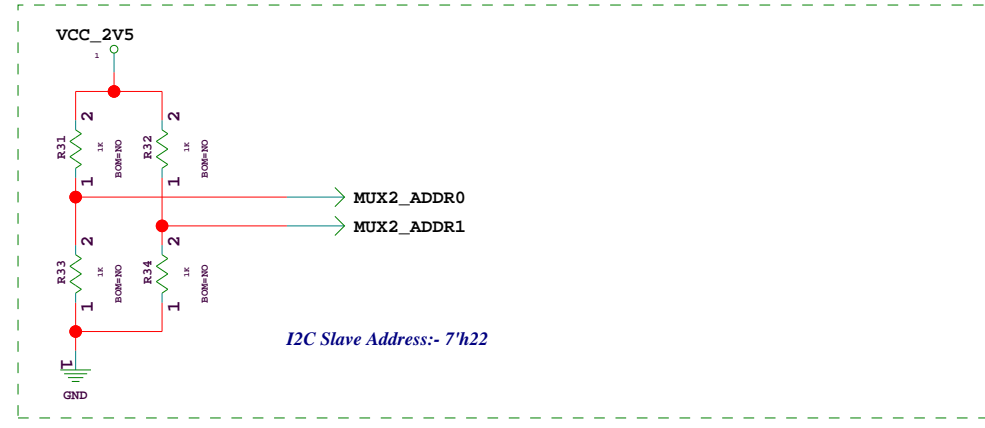


Description:		Tejas Networks	
DESCRIPTION			
		Sheet 4 of 10	
Project:	PROJECT NAME	Drawn By:	DESIGNER(S)
Date:	10-7-2024_12:41	Rev:	REV
		Reviewed By:	REVIEWER(S)
PART NUMBER:		PART_NUMBER	

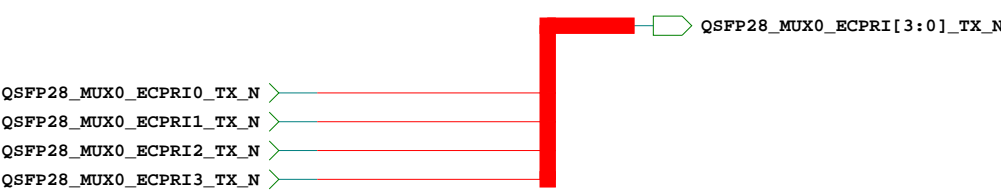
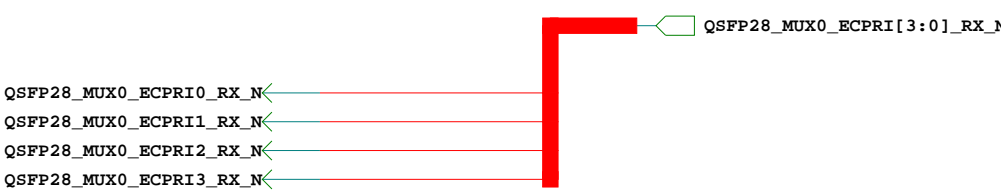
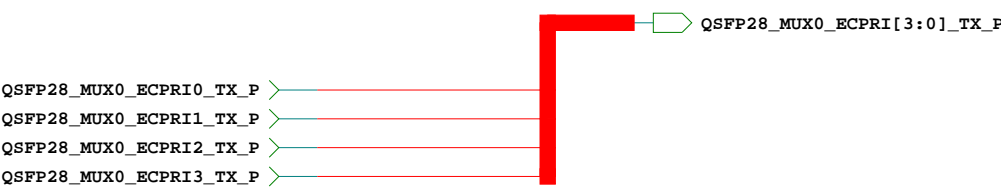
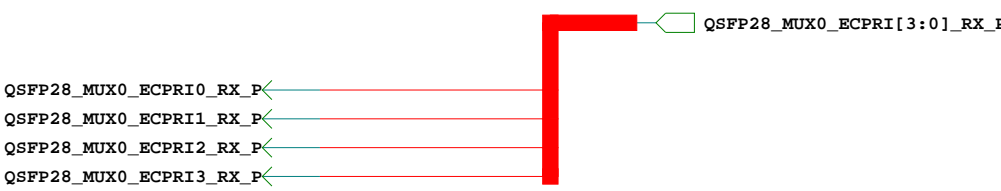
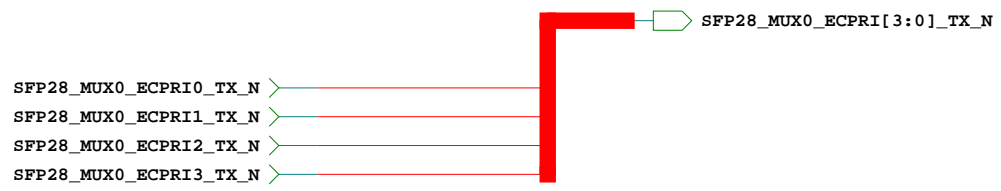
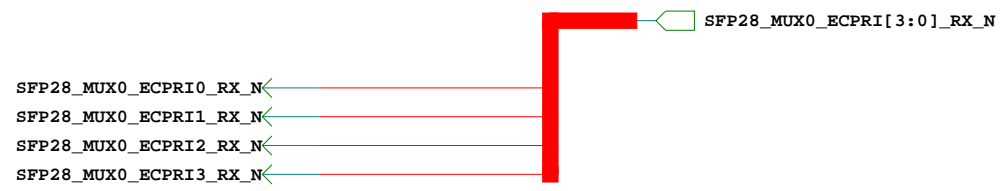
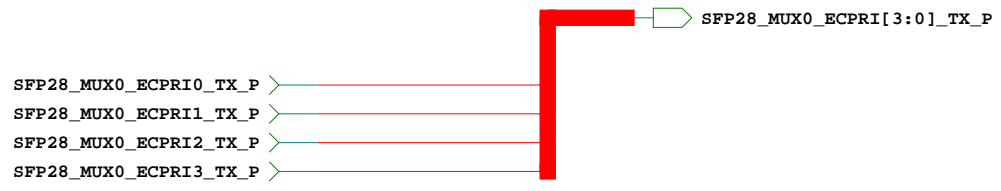
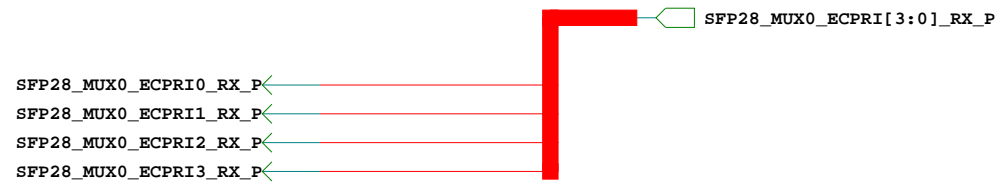


Description:		Tejas Networks	
DESCRIPTION			
Project: PROJECT NAME		Sheet 5 of 10	
Date: 10-7-2024_12:41		Rev: REV	
Drawn By: DESIGNER(S)		Reviewed By: REVIEWER(S)	
PART NUMBER:		PART_NUMBER	

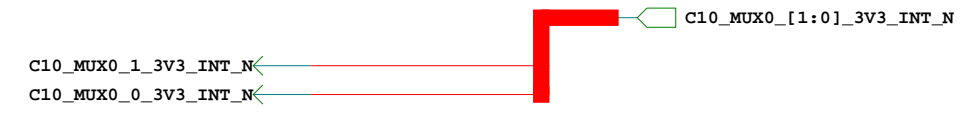
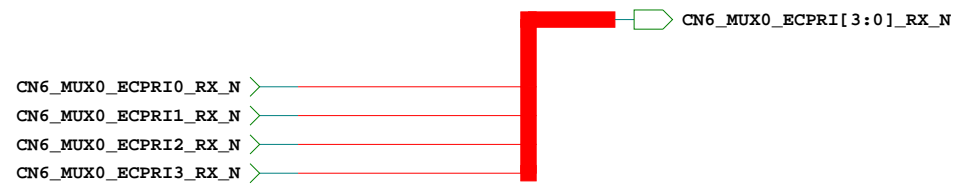
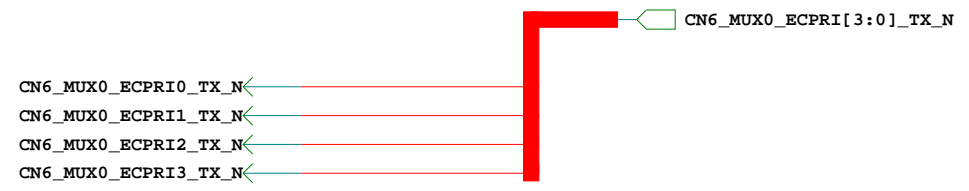
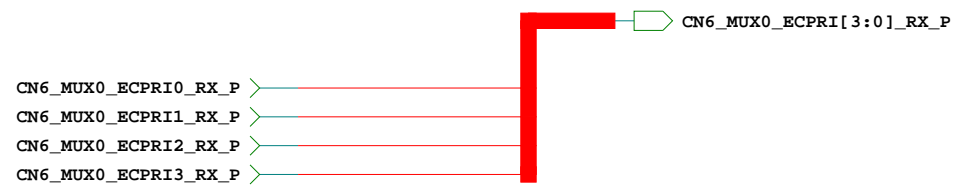
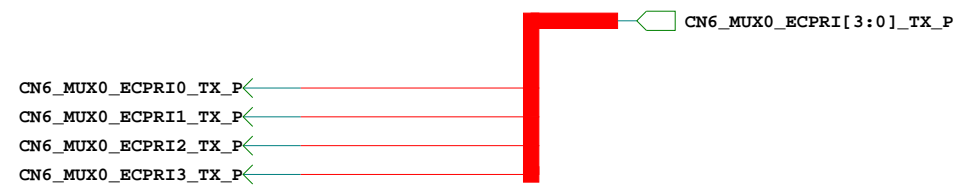
Note:- Need to Finalize on Calib clock requirement



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DESCRIPTION			
		Sheet 6 of 12	
Project:	PROJECT NAME	Drawn By:	DESIGNER(S)
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		Reviewed By:	REVIEWER(S)

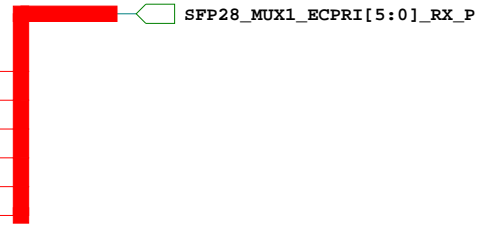


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DESCRIPTION		Sheet 6 of 8	
Project:	PROJECT NAME	Drawn By:	DESIGNER(S)
Date:	7-19-2024_1:52	Rev:	REV
		Reviewed By:	REVIEWER(S)

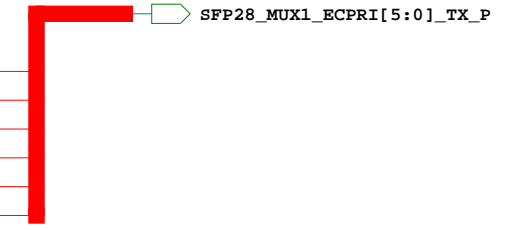


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DESCRIPTION		Sheet 8 of 12	
Project:	PROJECT NAME	Drawn By:	DESIGNER(S)
Date:	9-18-2024_13:11	Rev:	REV
		Reviewed By:	REVIEWER(S)

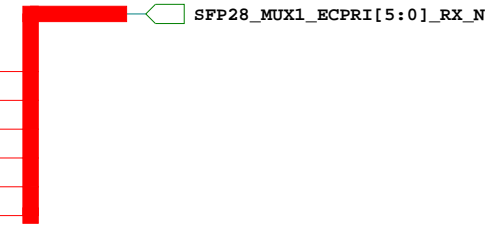
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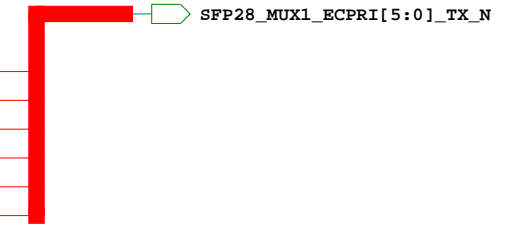
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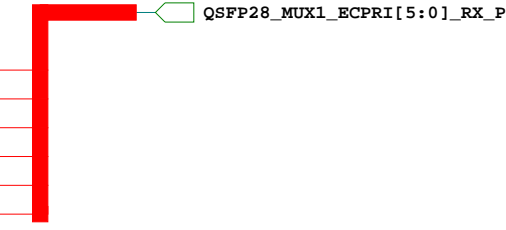
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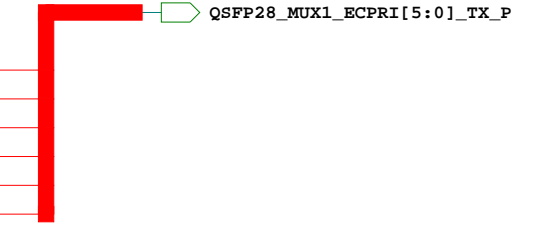
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QSFP28_MUX1_ECPRI5_RX_P
 QSFP28_MUX1_ECPRI4_RX_P
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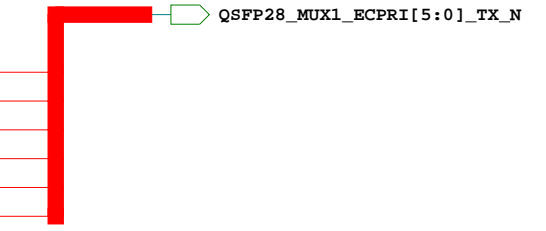
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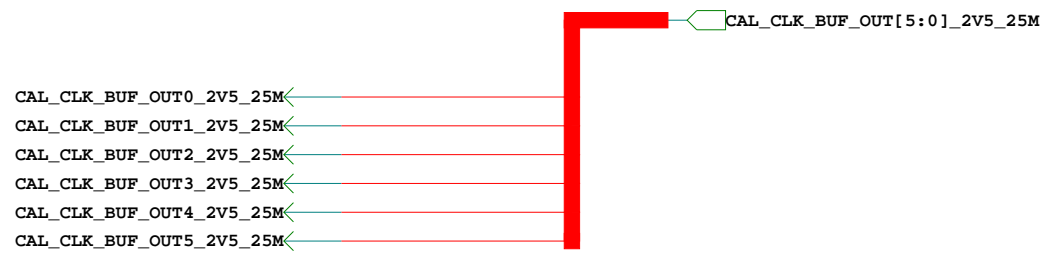
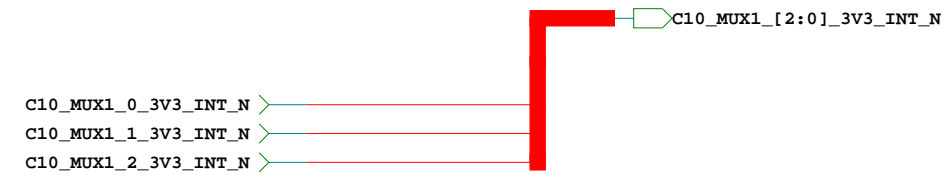
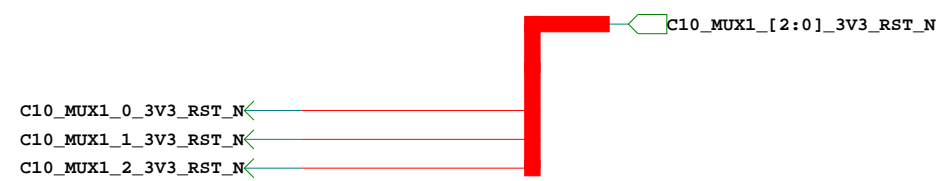
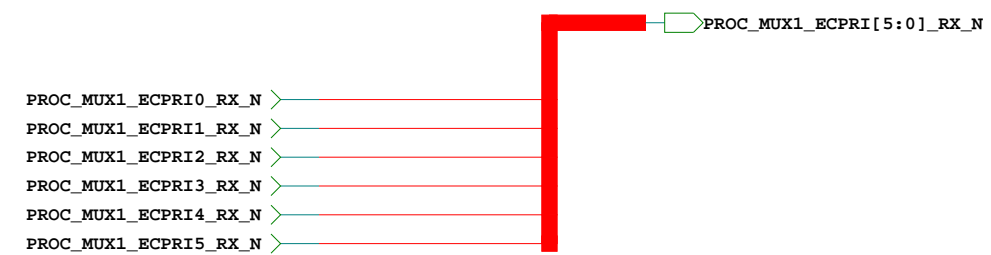
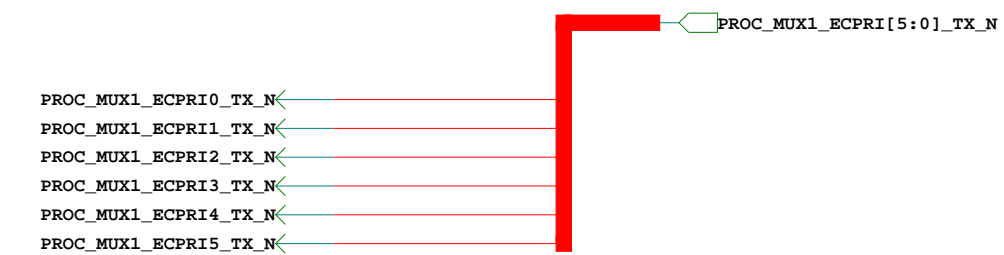
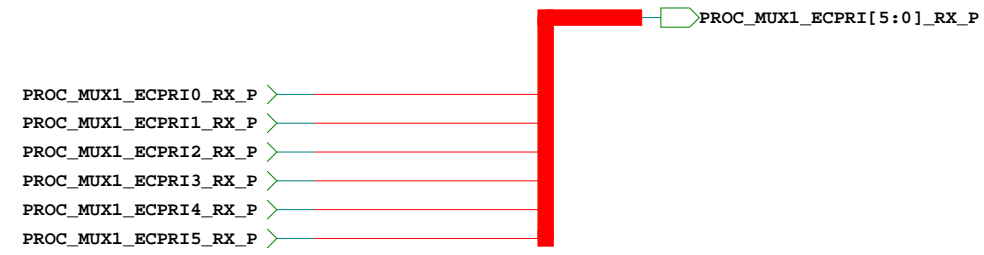
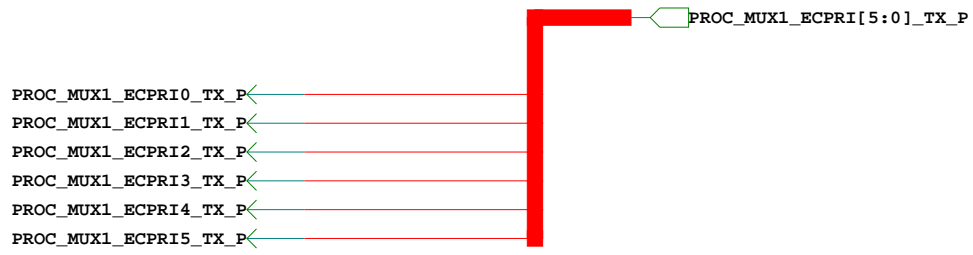
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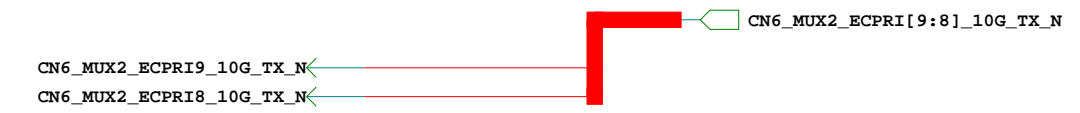
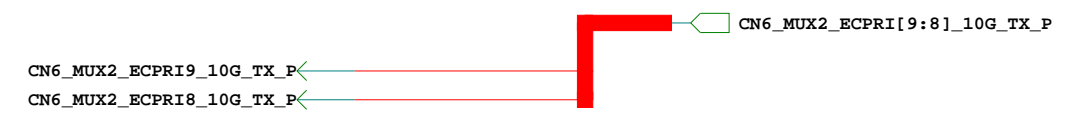
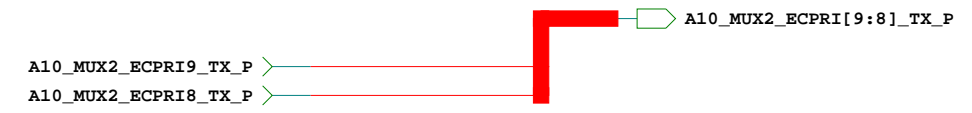
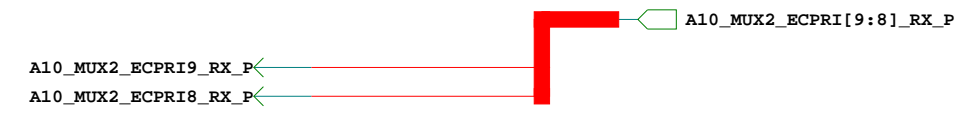
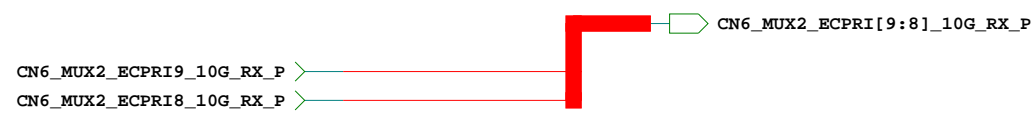
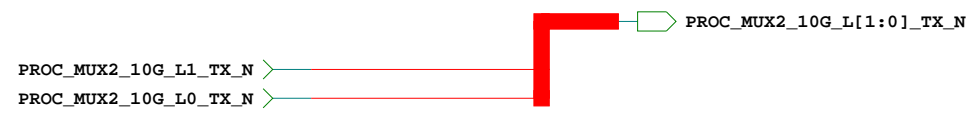
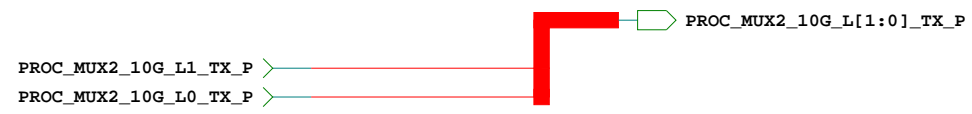
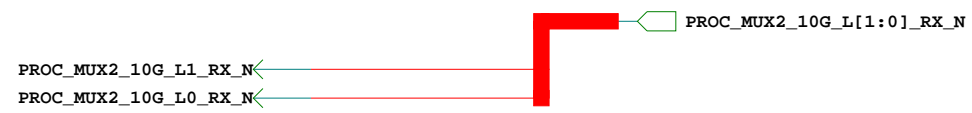
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 QSFP28_MUX1_ECPRI1_TX_N
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Date:	7-19-2024_1:52	Rev:	REV
		Reviewed By:	REVIEWER(S)



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DESCRIPTION			
		Sheet 10 of 12	
Project:	PROJECT NAME	Drawn By:	DESIGNER(S)
Date:	9-18-2024_14:08	Rev:	REV
		Reviewed By:	REVIEWER(S)



Description:		Tejas Networks	
DESCRIPTION			
Sheet 11 of 12			
Project:	PROJECT NAME	Drawn By:	DESIGNER(S)
Date:	9-18-2024_14:37	Rev:	REV
		Reviewed By:	REVIEWER(S)

PART NUMBER: PART_NUMBER

A

B

C

D

1

1

2

2

3

3

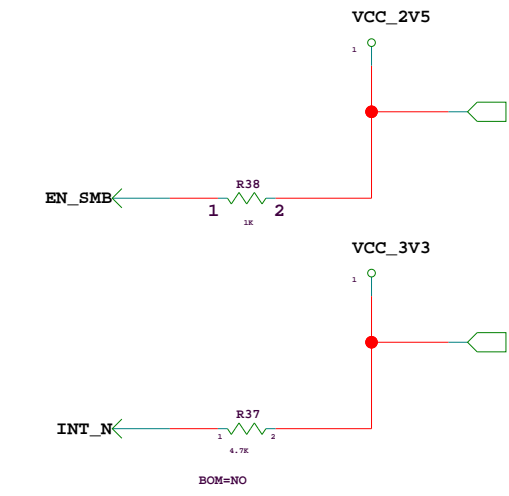
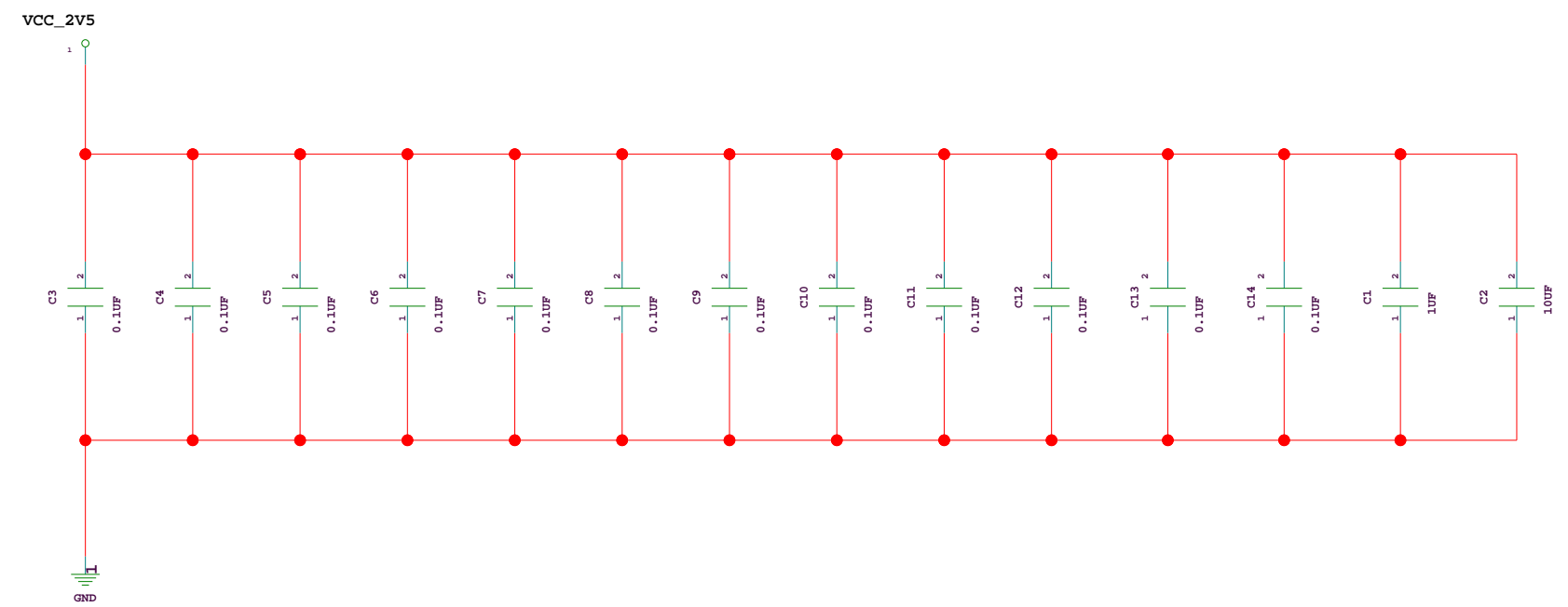
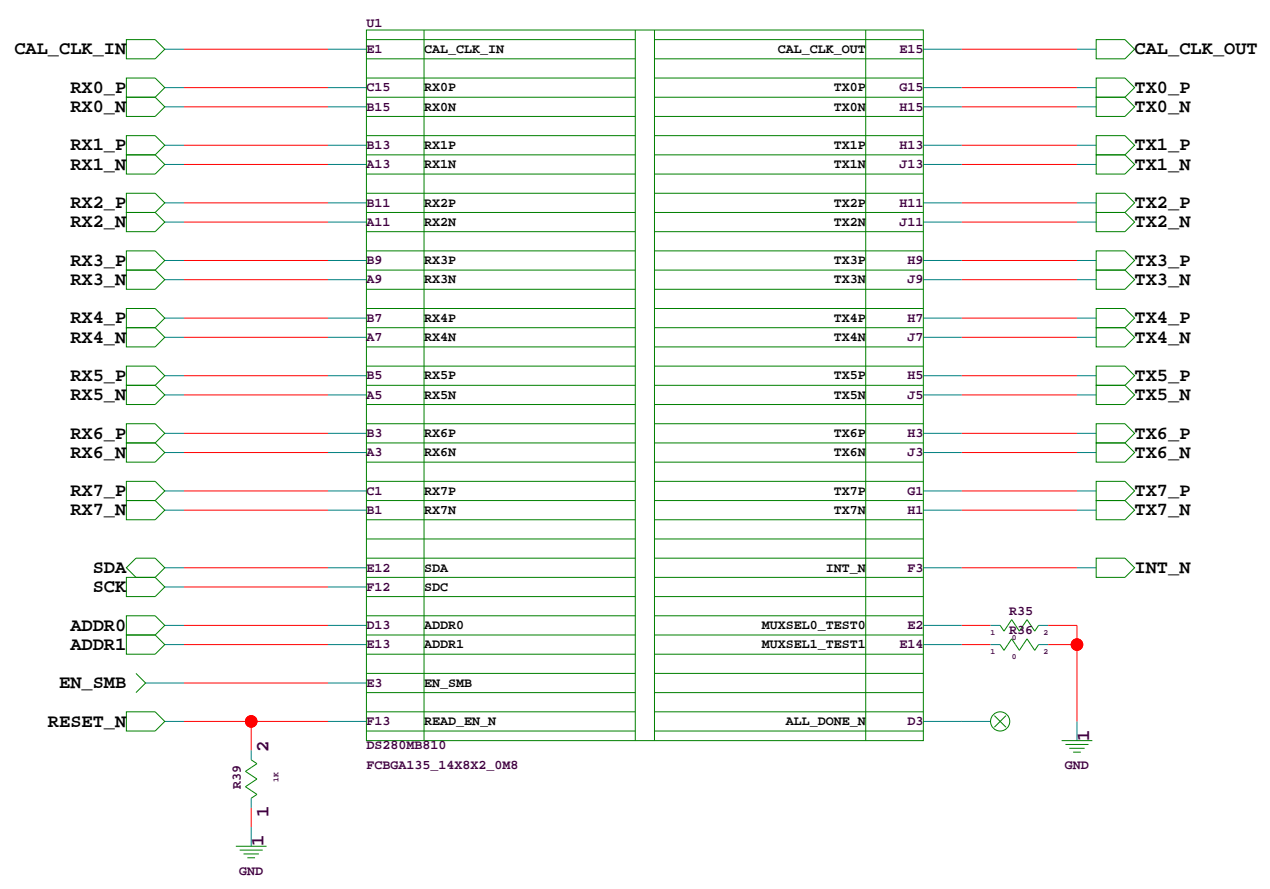
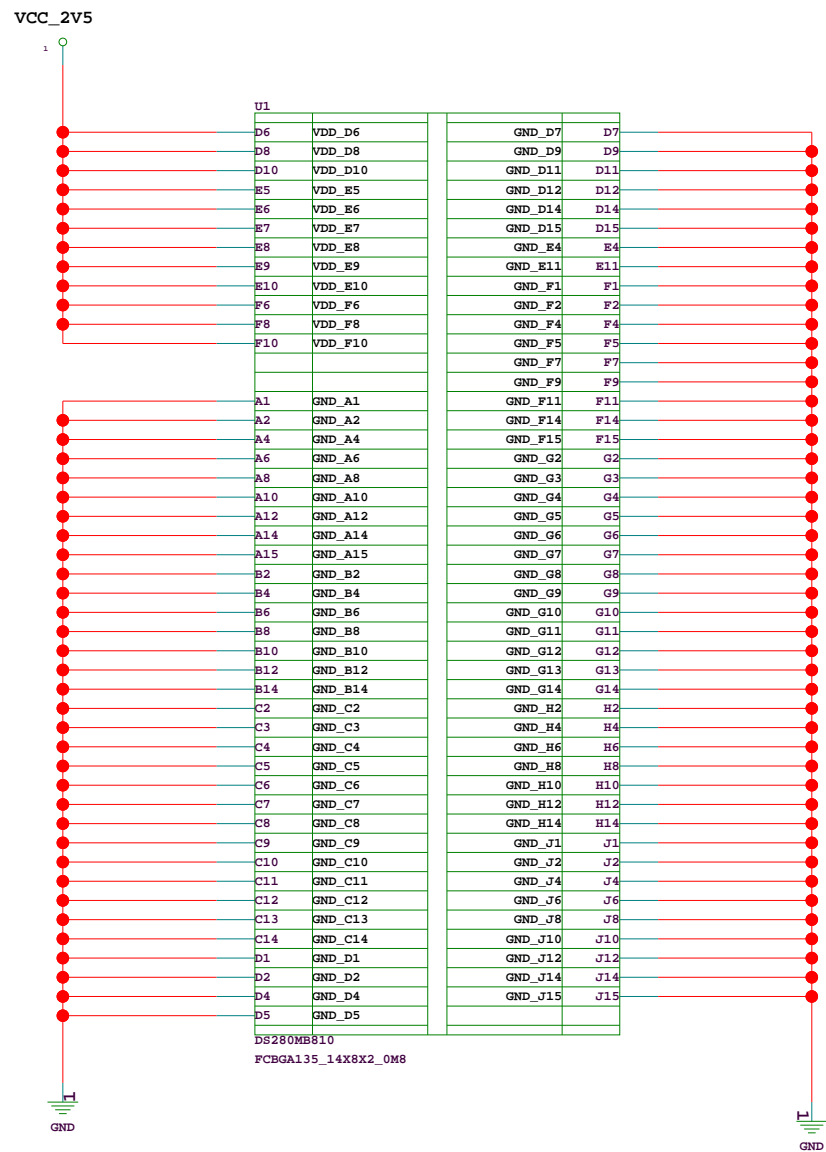
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DESCRIPTION		Sheet 12 of 12	
Project:	PROJECT NAME	Drawn By:	DESIGNER(S)
Date:	9-18-2024_13:04	Rev:	REV
		Reviewed By:	REVIEWER(S)

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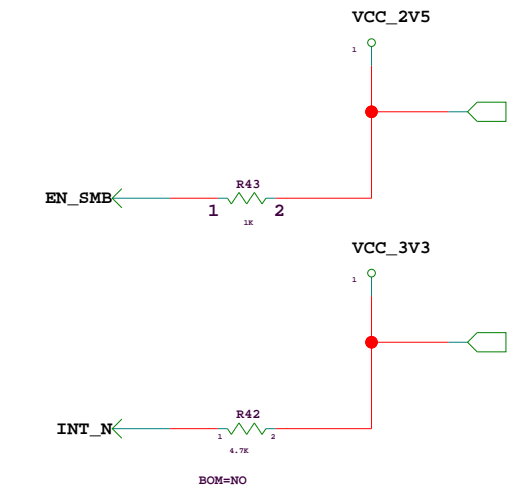
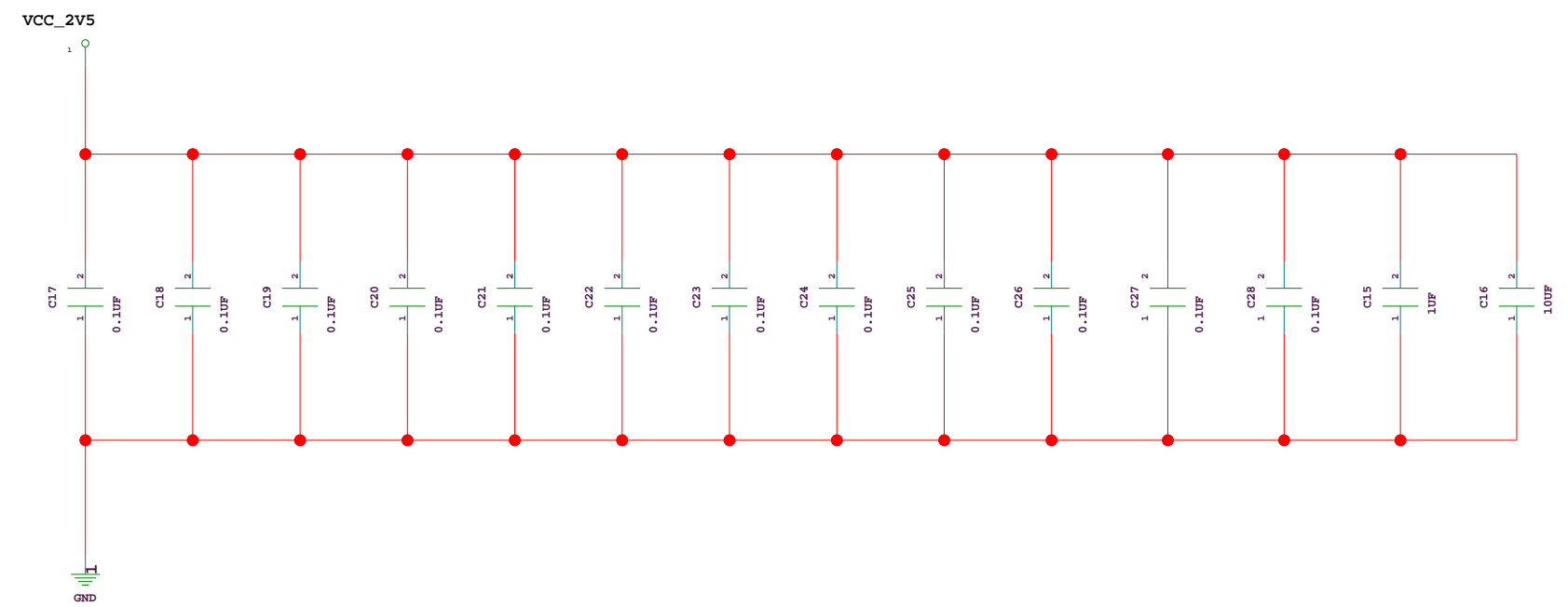
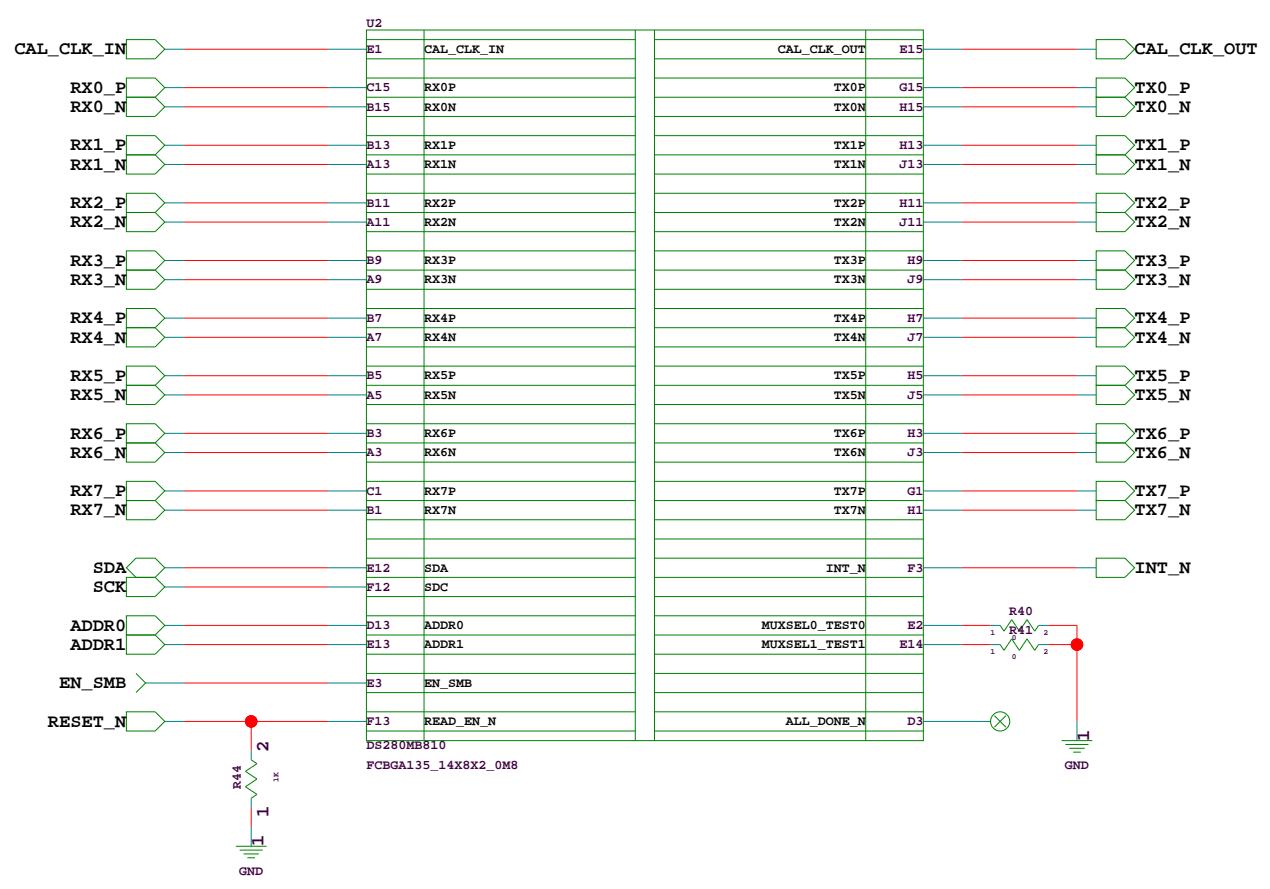
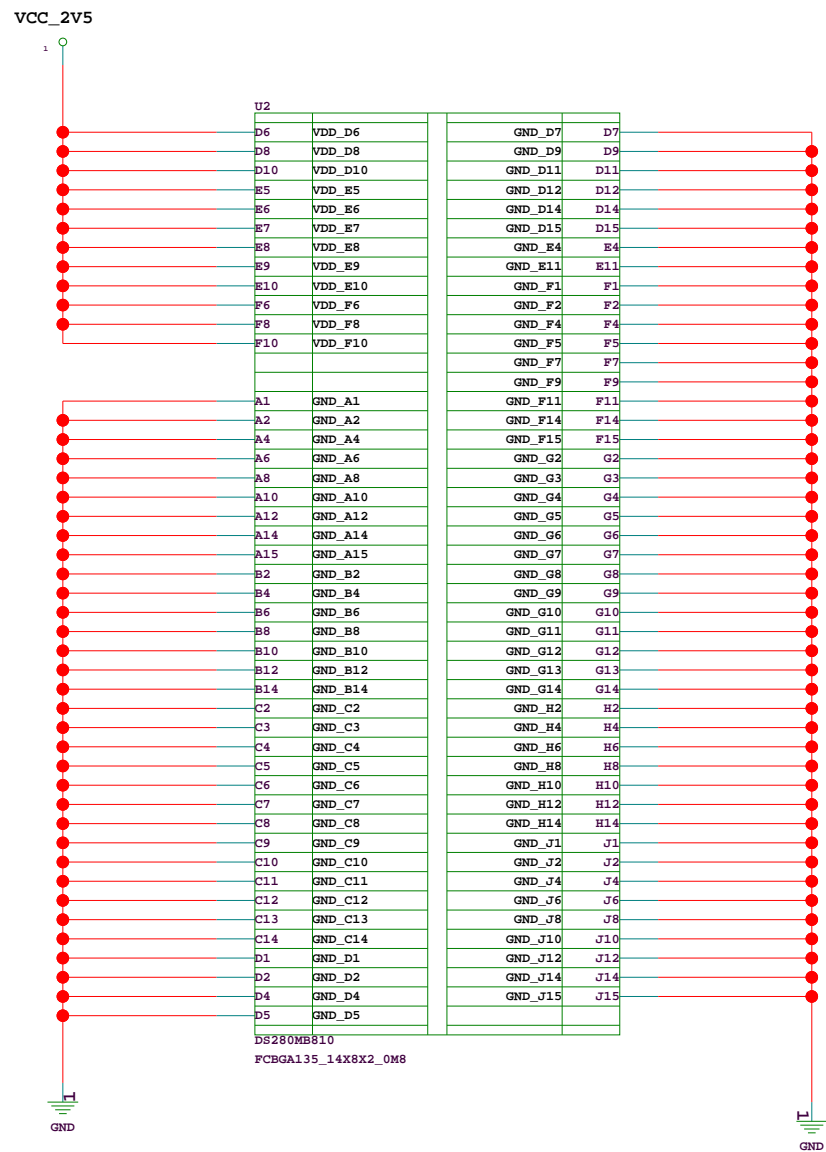
TJ1400-NR 5GAC100 1U PLATFORM

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Project: TJ1400-NR Drawn By: DESIGNER(S)

Date: 10-7-2024_12:41 Rev: 1 Reviewed By: RIJAS

PART NUMBER: TBD



Description:

TJ1400-NR 5GAC100 1U PLATFORM

Project: TJ1400-NR

Date: 10-7-2024_12:41

Rev: 1

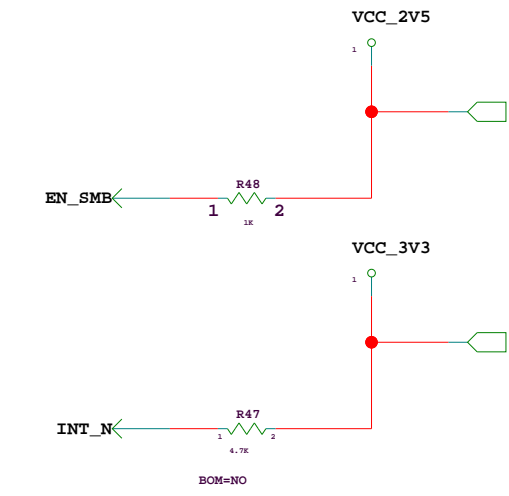
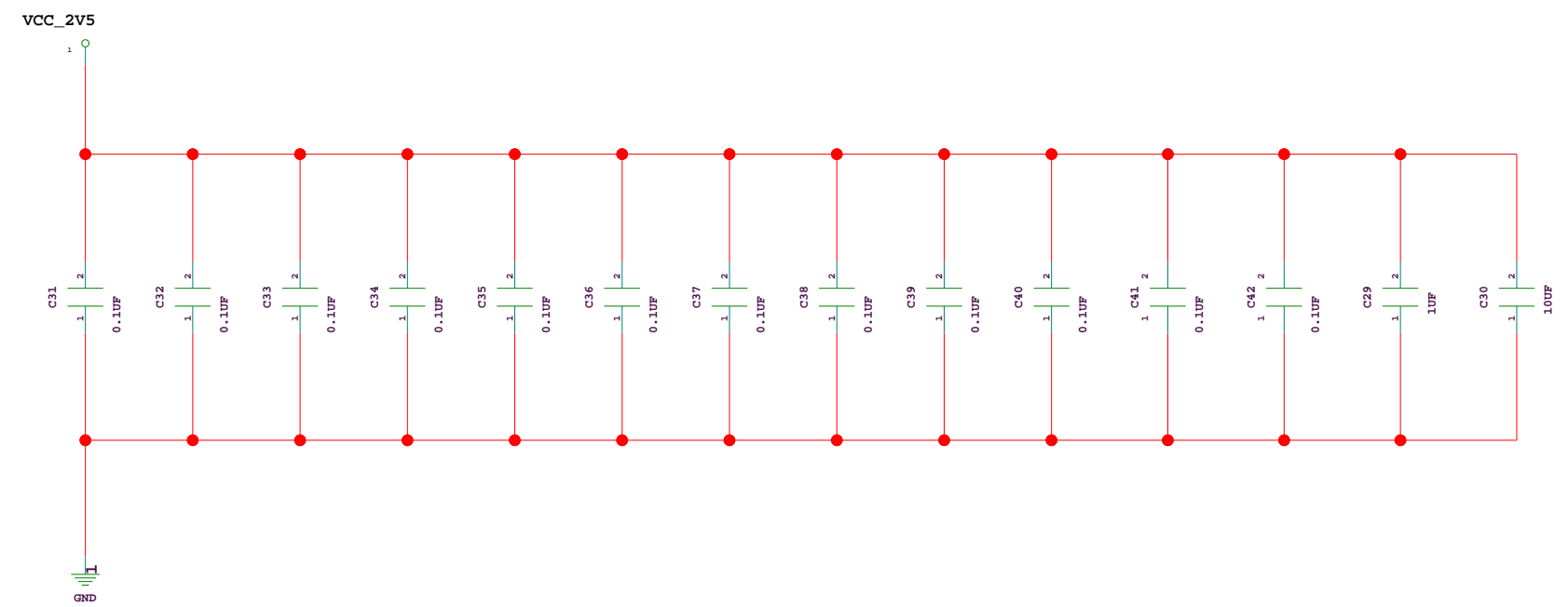
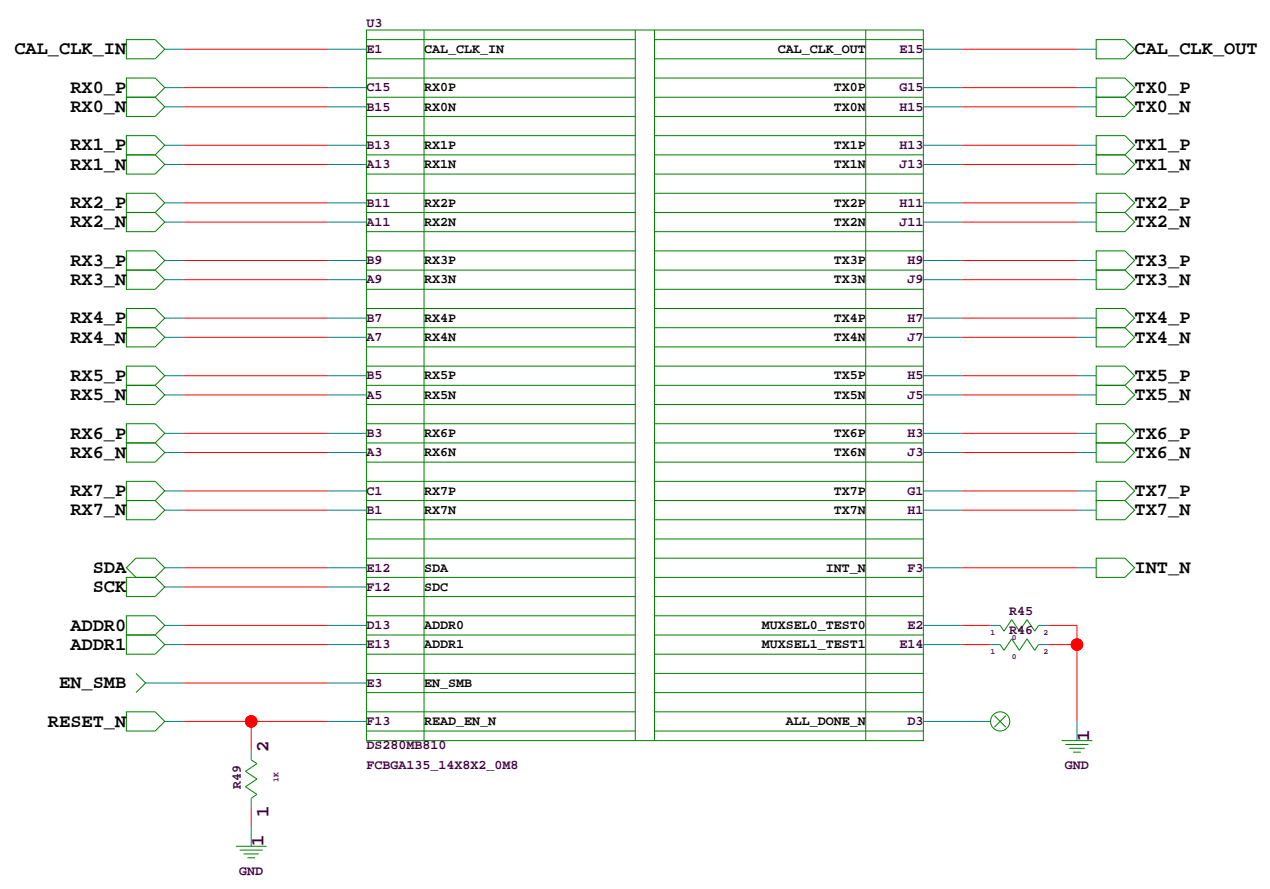
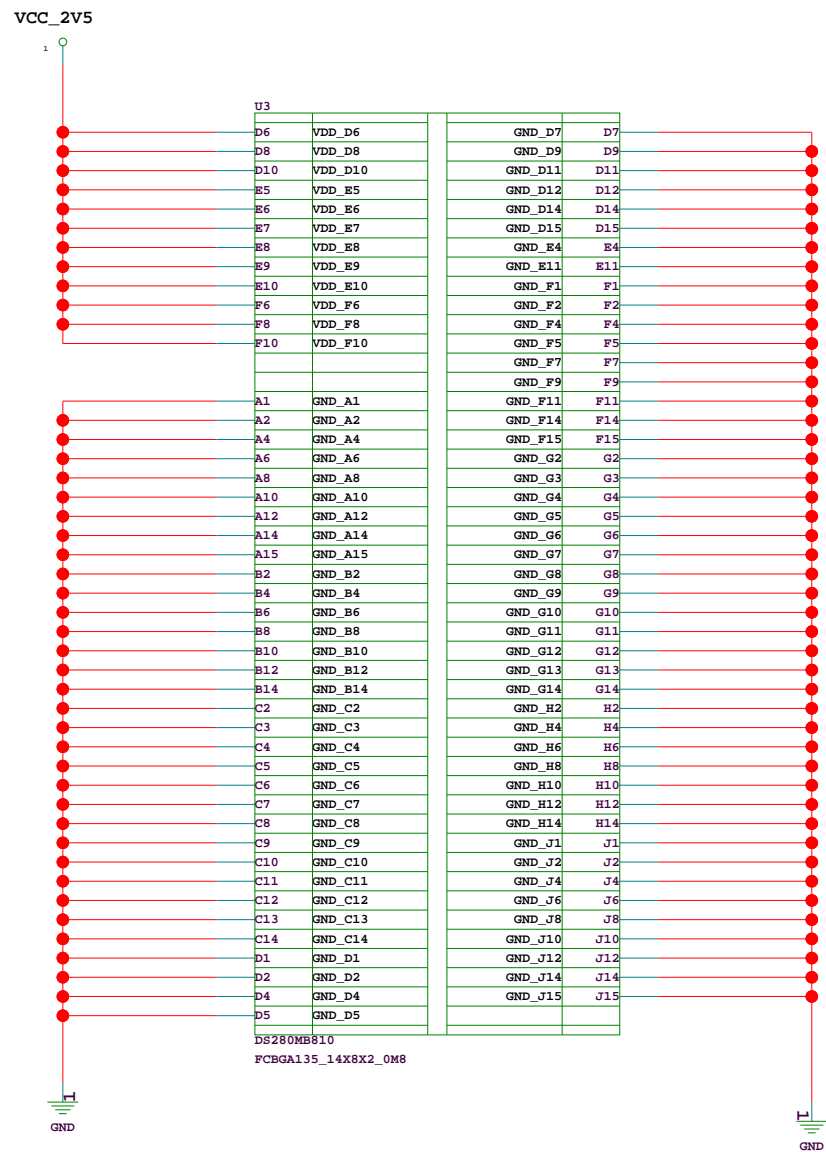
Sheet 1 of 1

Drawn By: DESIGNER(S)

Reviewed By: RIJAS

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Description:

TJ1400-NR 5GAC100 1U PLATFORM

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Project: TJ1400-NR

Drawn By: DESIGNER(S)

Date: 10-7-2024_12:41

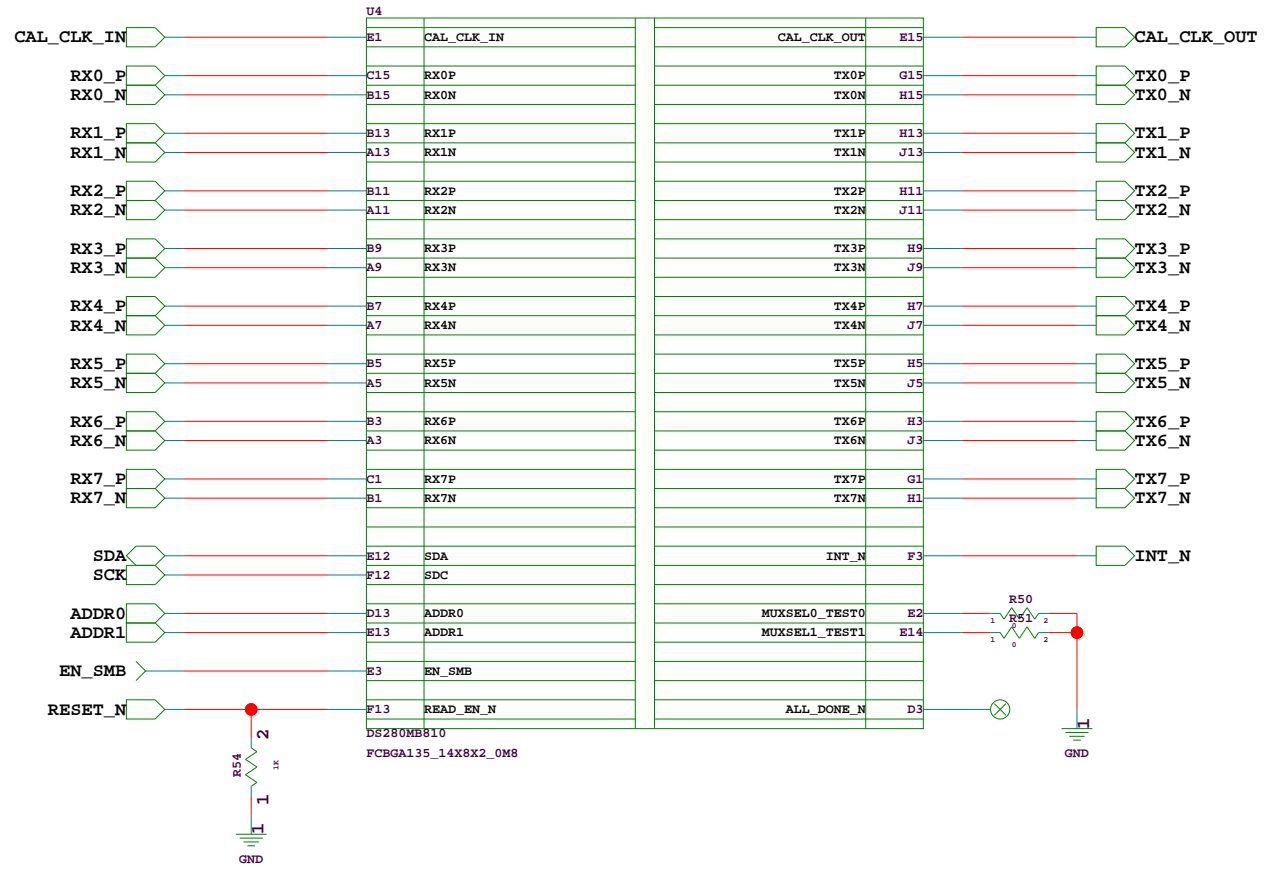
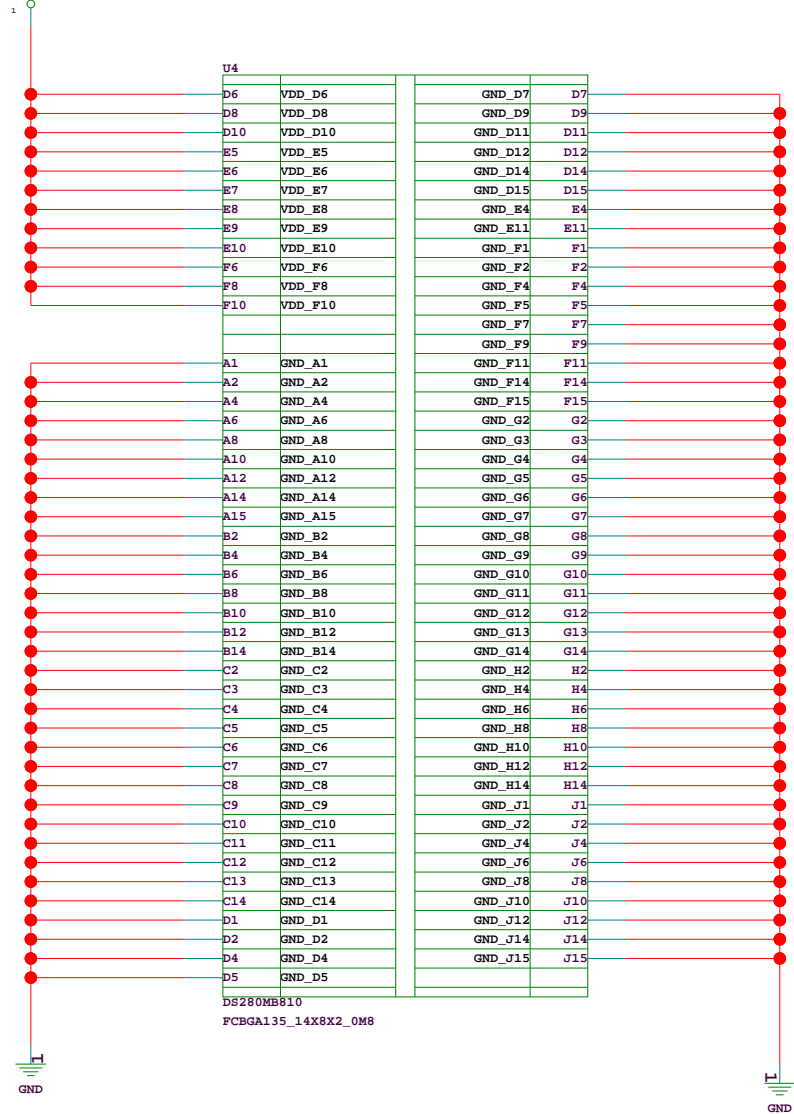
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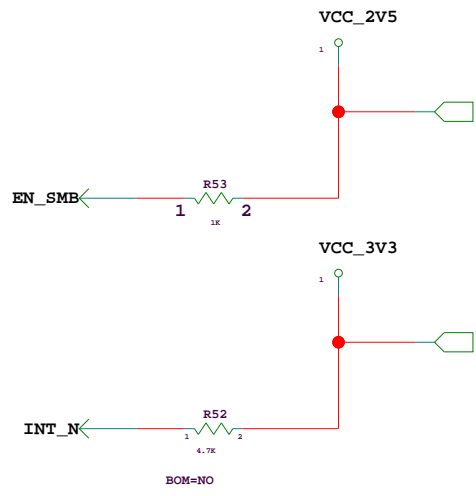
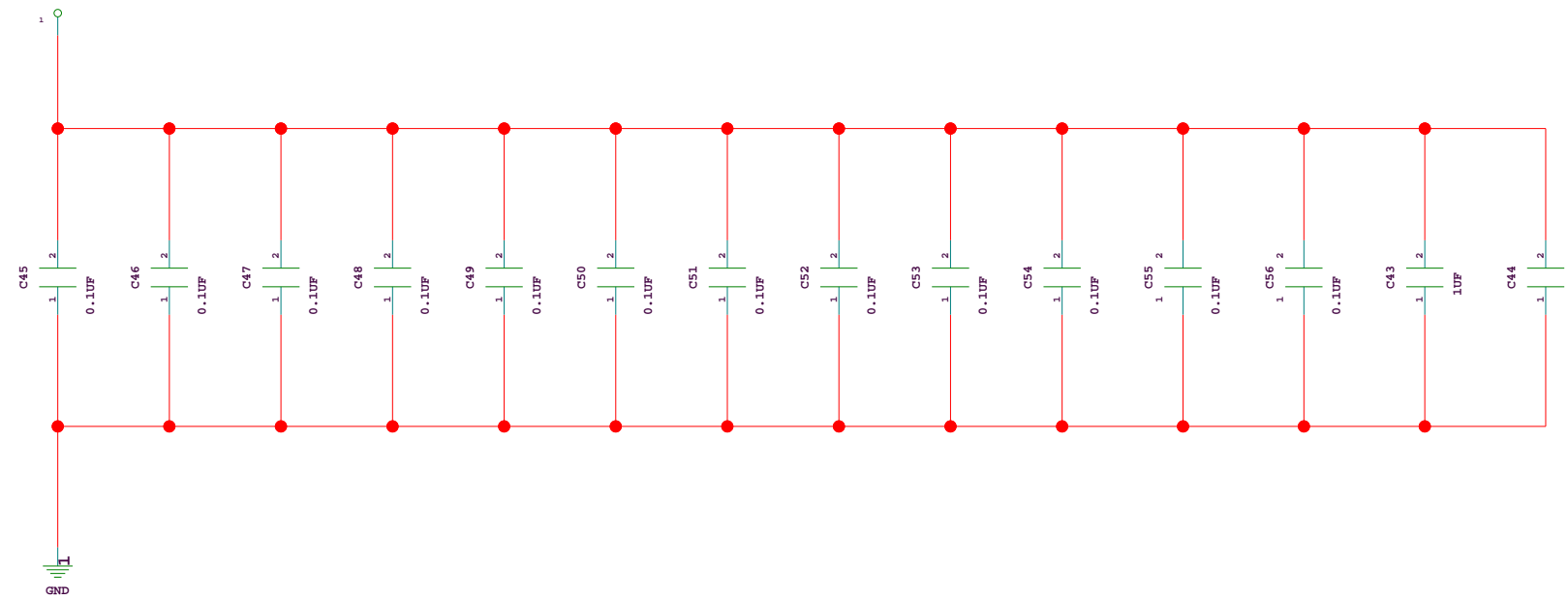
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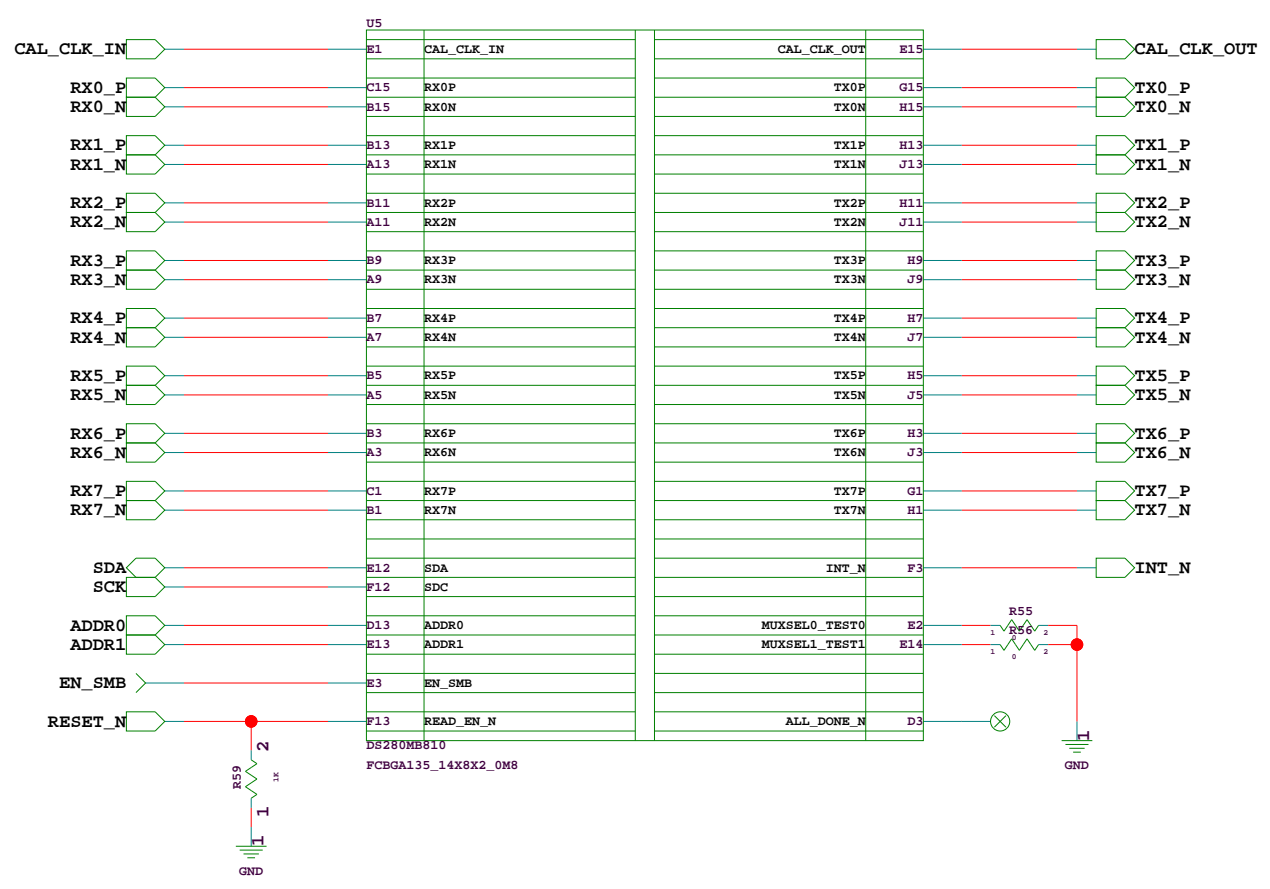
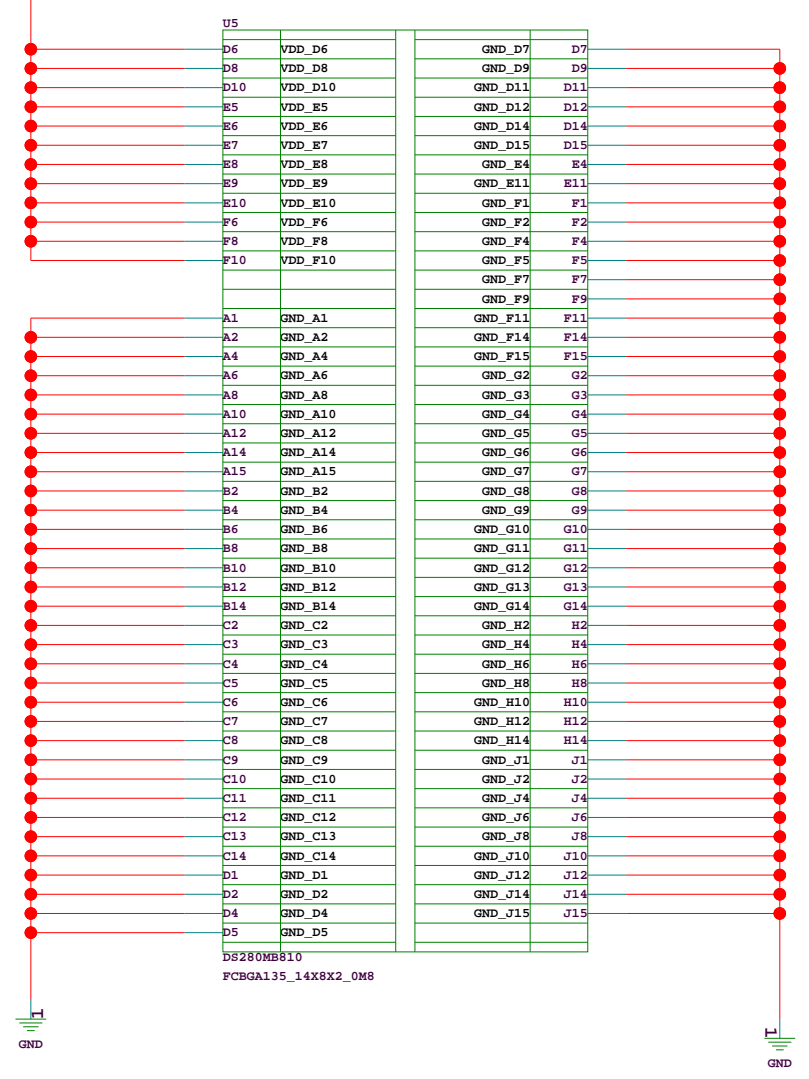
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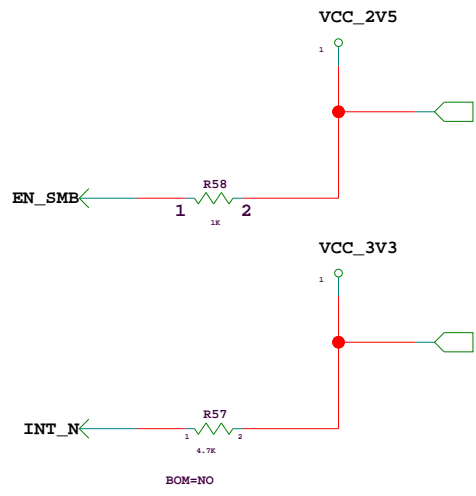
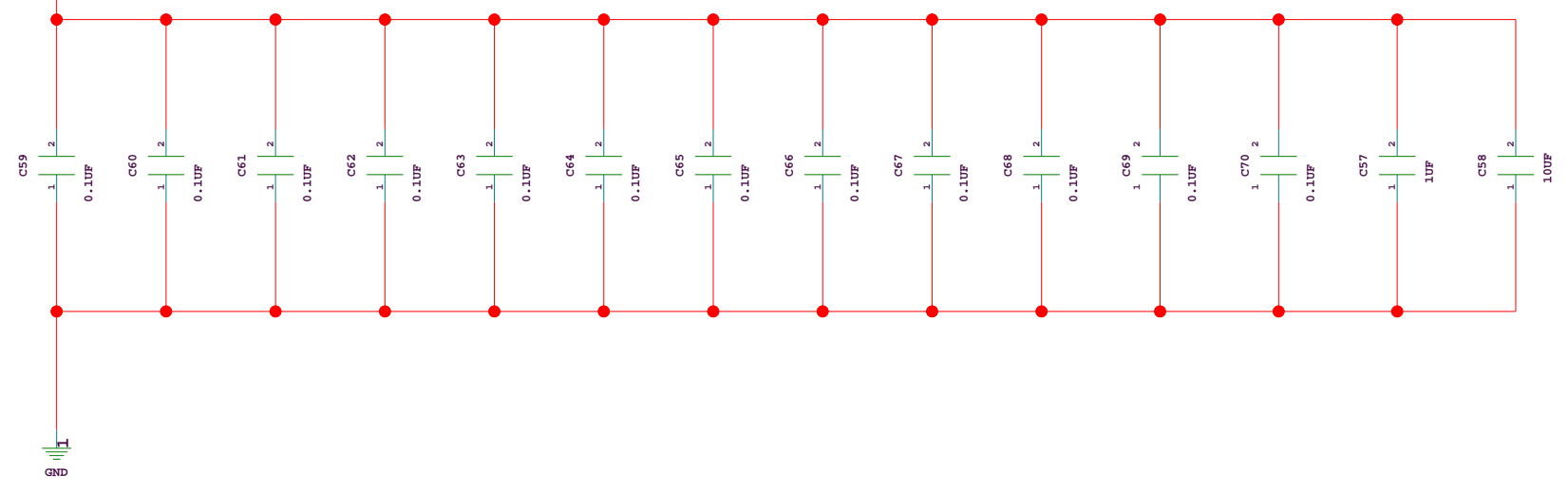
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Date: 10-7-2024_12:41	Rev: 1
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Description:
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Date: 10-7-2024_12:41

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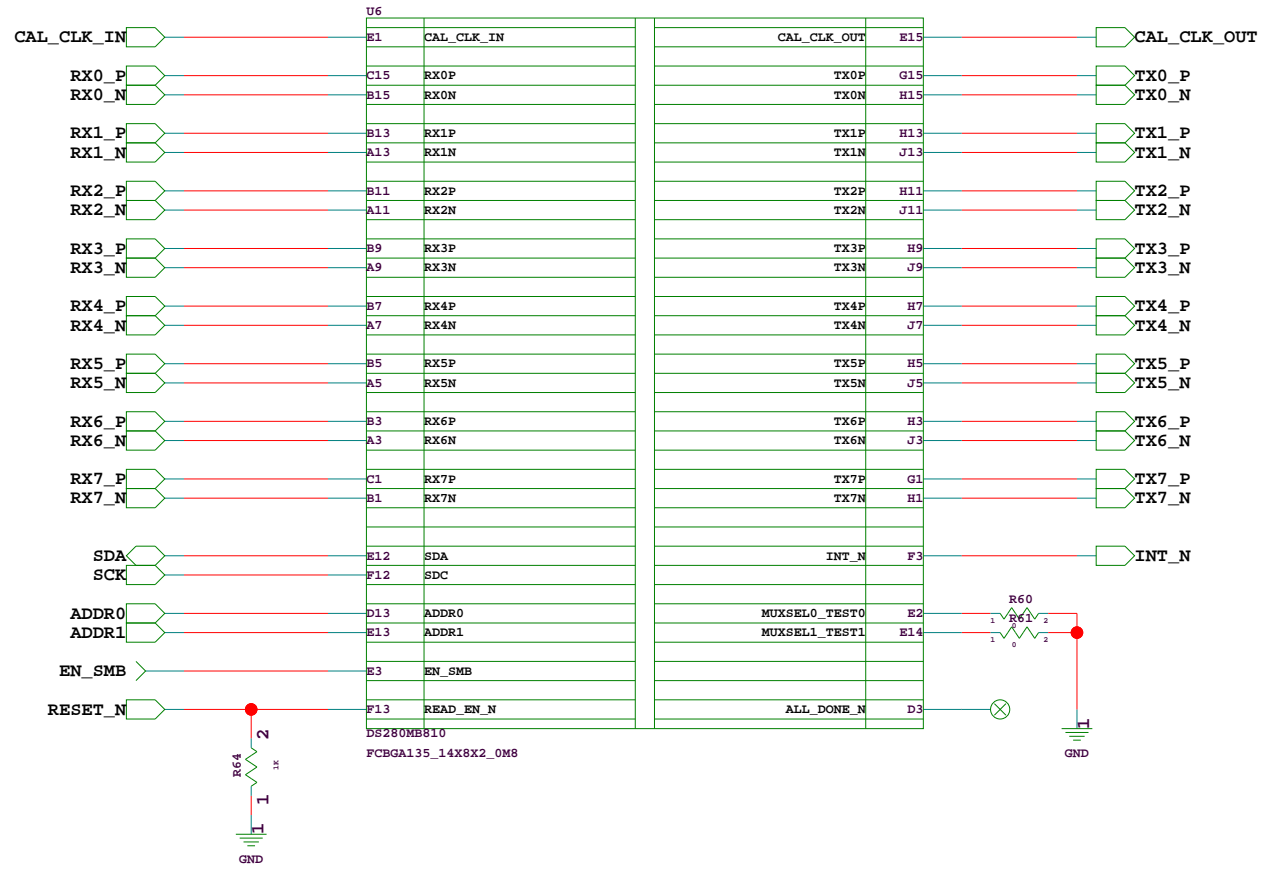
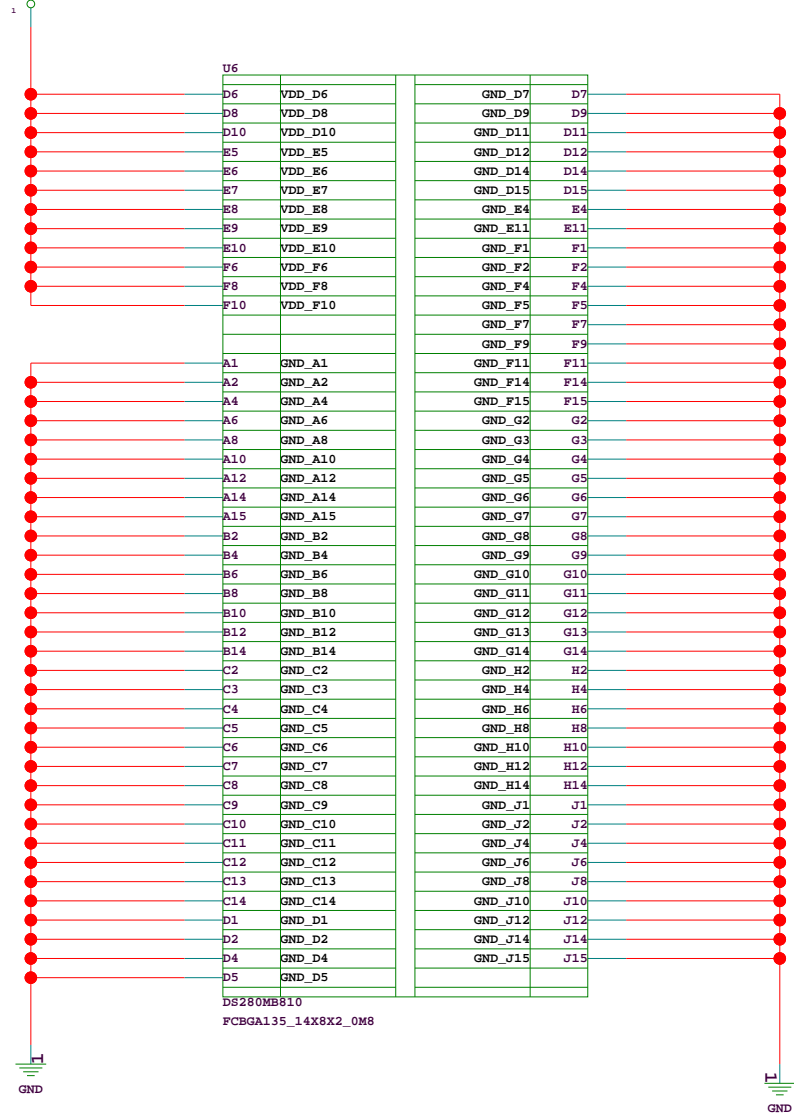
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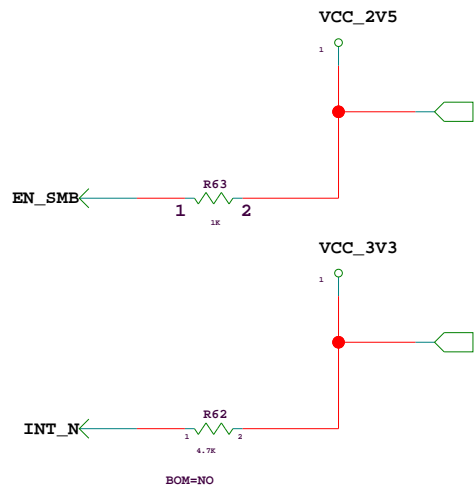
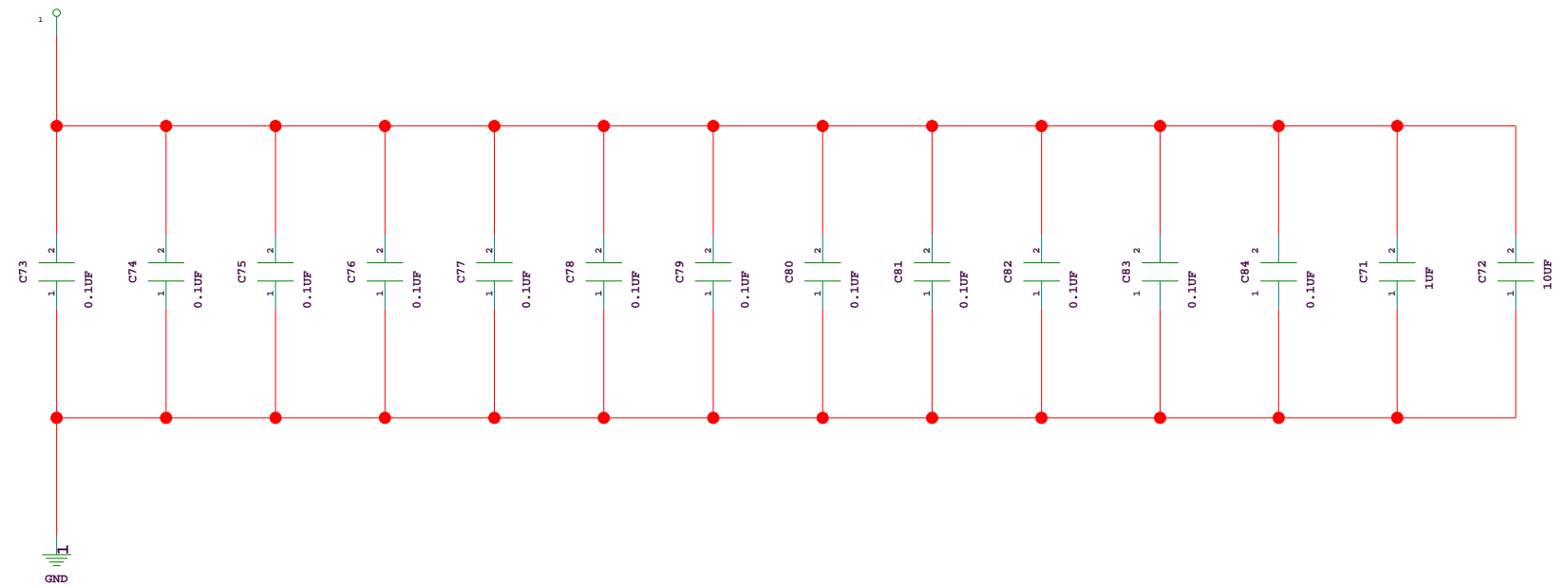
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Description:

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