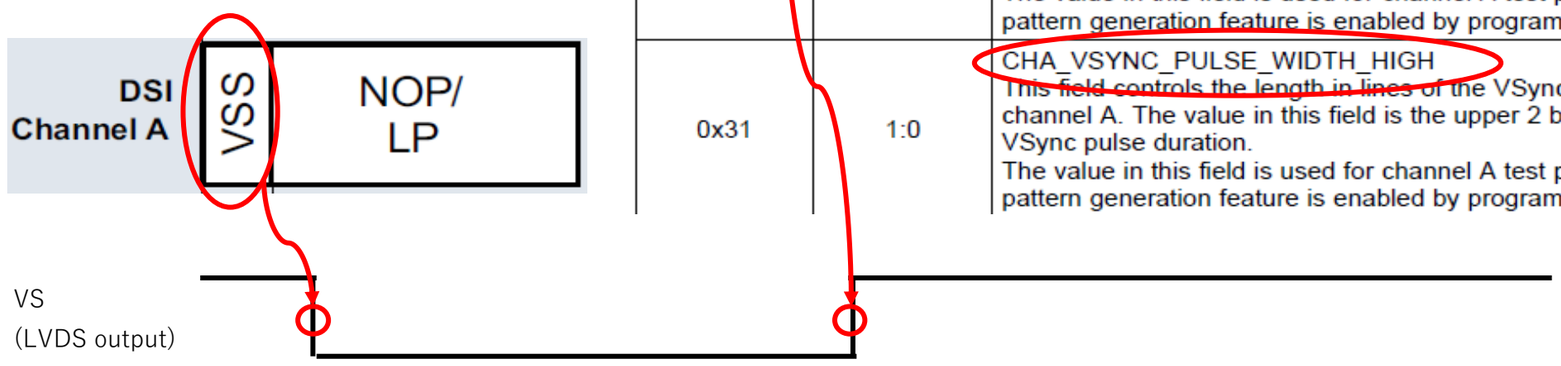
VSYNC_PULSE_WIDTH

0x30	7:0	CHA_VSYNC_PULSE_WIDTH_LOW This field controls the length in lines of the VSync pulse duration for LVDS channel A. The value in this field is the lower 8 bits of the 10-bit value for the VSync pulse duration. The value in this field is used for channel A test pattern generation when test pattern generation feature is enabled by programming bit 4 at 0x3C.
0x31	1:0	CHA_VSYNC_PULSE_WIDTH_HIGH This field controls the length in lines of the VSync pulse duration for LVDS channel A. The value in this field is the upper 2 bits of the 10-bit value for the VSync pulse duration. The value in this field is used for channel A test pattern generation when test pattern generation feature is enabled by programming bit 4 at 0x3C.

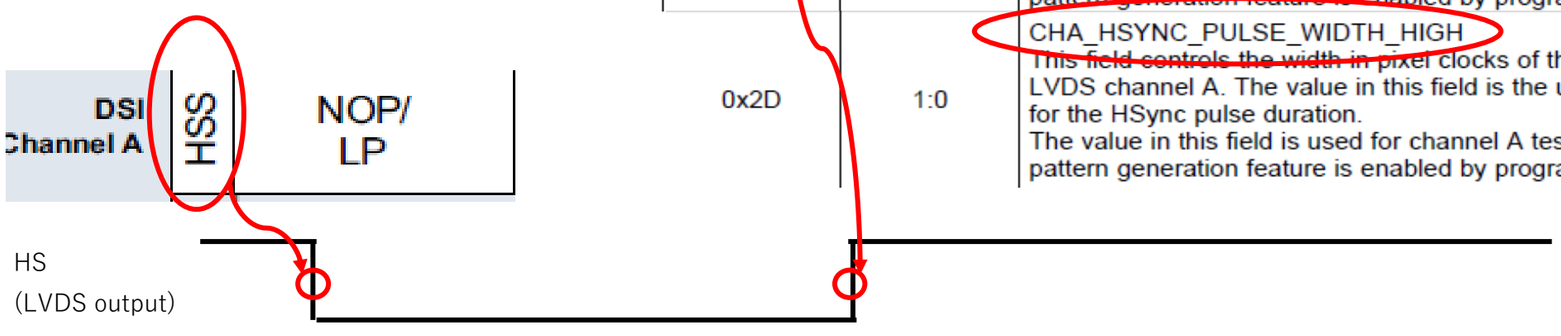


Asserted from HI to LOW by finding VSS

Deasserted from LOW to HI by the setting value of VSYNC_PULSE_WIDTH register

HSYNC_PULSE_WIDTH

0x2C	7:0	CHA_HSYNC_PULSE_WIDTH_LOW This field controls the width in pixel clocks of the HSync pulse duration for LVDS channel A. The value in this field is the lower 8 bits of the 10-bit value for the HSync pulse duration. The value in this field is used for channel A test pattern generation when test pattern generation feature is enabled by programming bit 4 at 0x3C.
0x2D	1:0	CHA_HSYNC_PULSE_WIDTH_HIGH This field controls the width in pixel clocks of the HSync pulse duration for LVDS channel A. The value in this field is the upper 2 bits of the 10-bit value for the HSync pulse duration. The value in this field is used for channel A test pattern generation when test pattern generation feature is enabled by programming bit 4 at 0x3C.



Asserted from HI to LOW by finding HSS

Deasserted from LOW to HI by the setting value of HSYNC_PULSE_WIDTH register