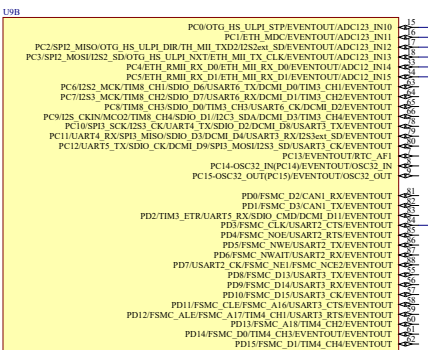
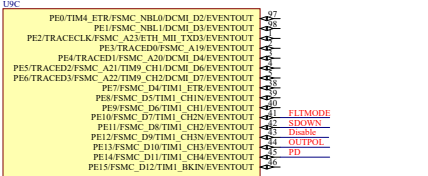


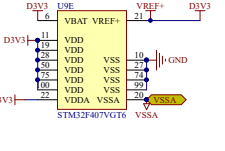
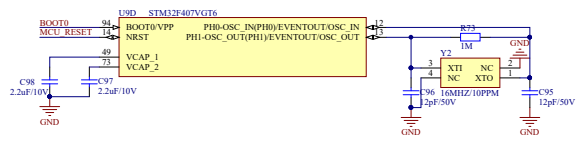
STM32F407VGT6



STM32F407VGT6



STM32F407VGT6

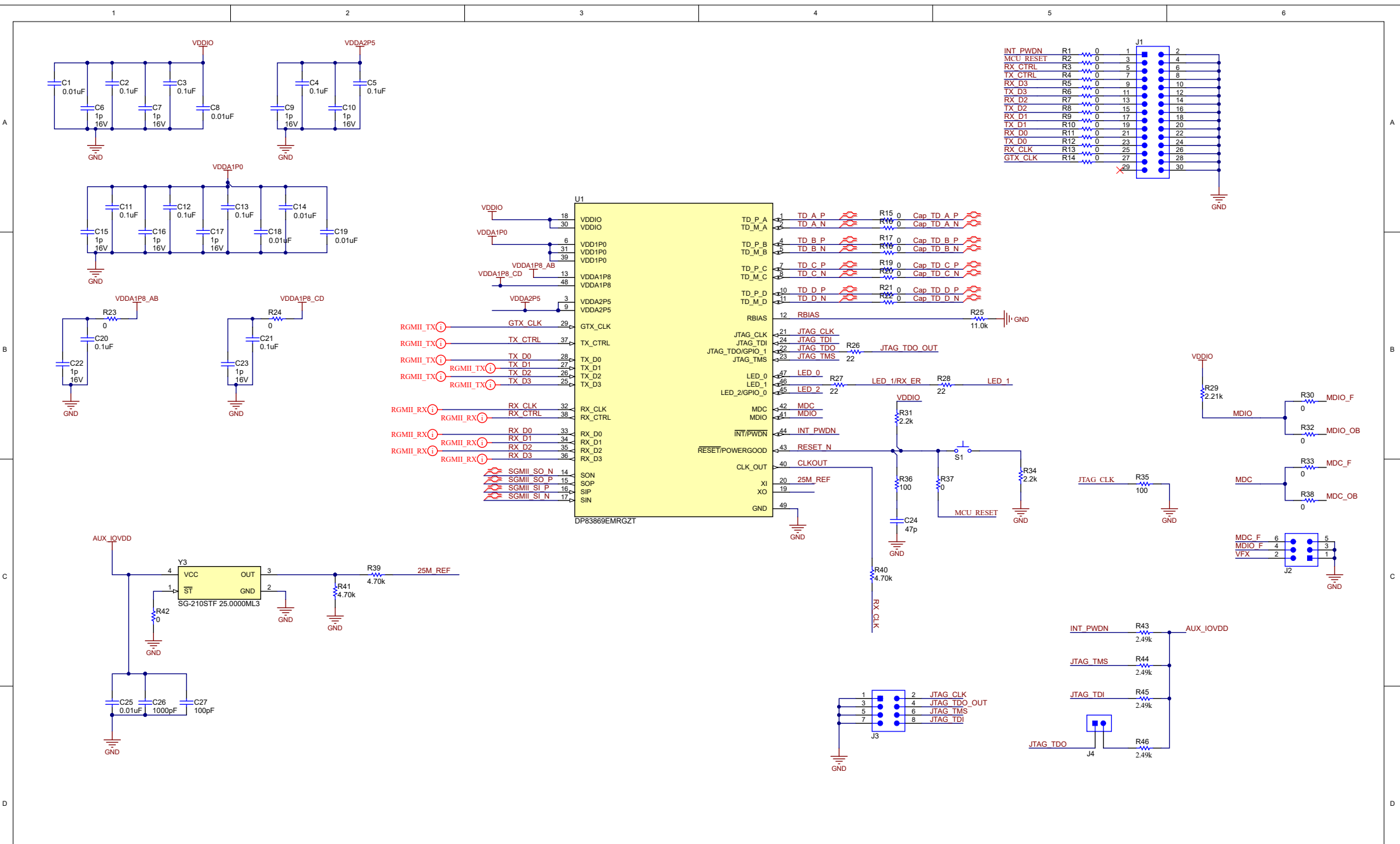


### MCU复位



- 1: MONP
- 2: SDOWN
- 3: JTAGMODE
- 4: DnAKE
- 5: OUTPOL
- 6: PD
- 7: PD
- 8: SGM1\_S0\_T
- 9: SGM1\_S0\_T
- 10: SGM1\_S0\_T

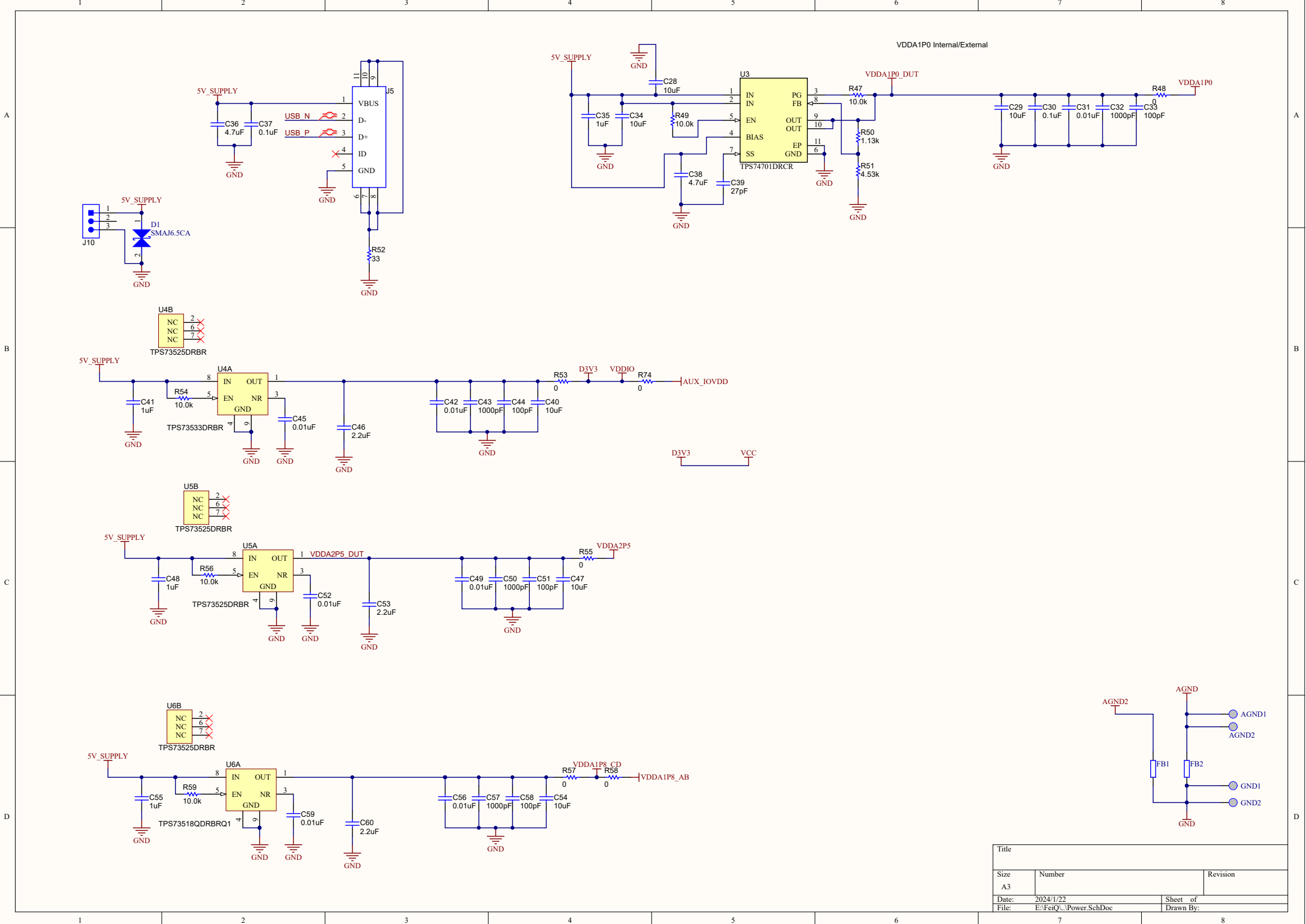
J111的PINS和PIN0尽量靠近DPS1869



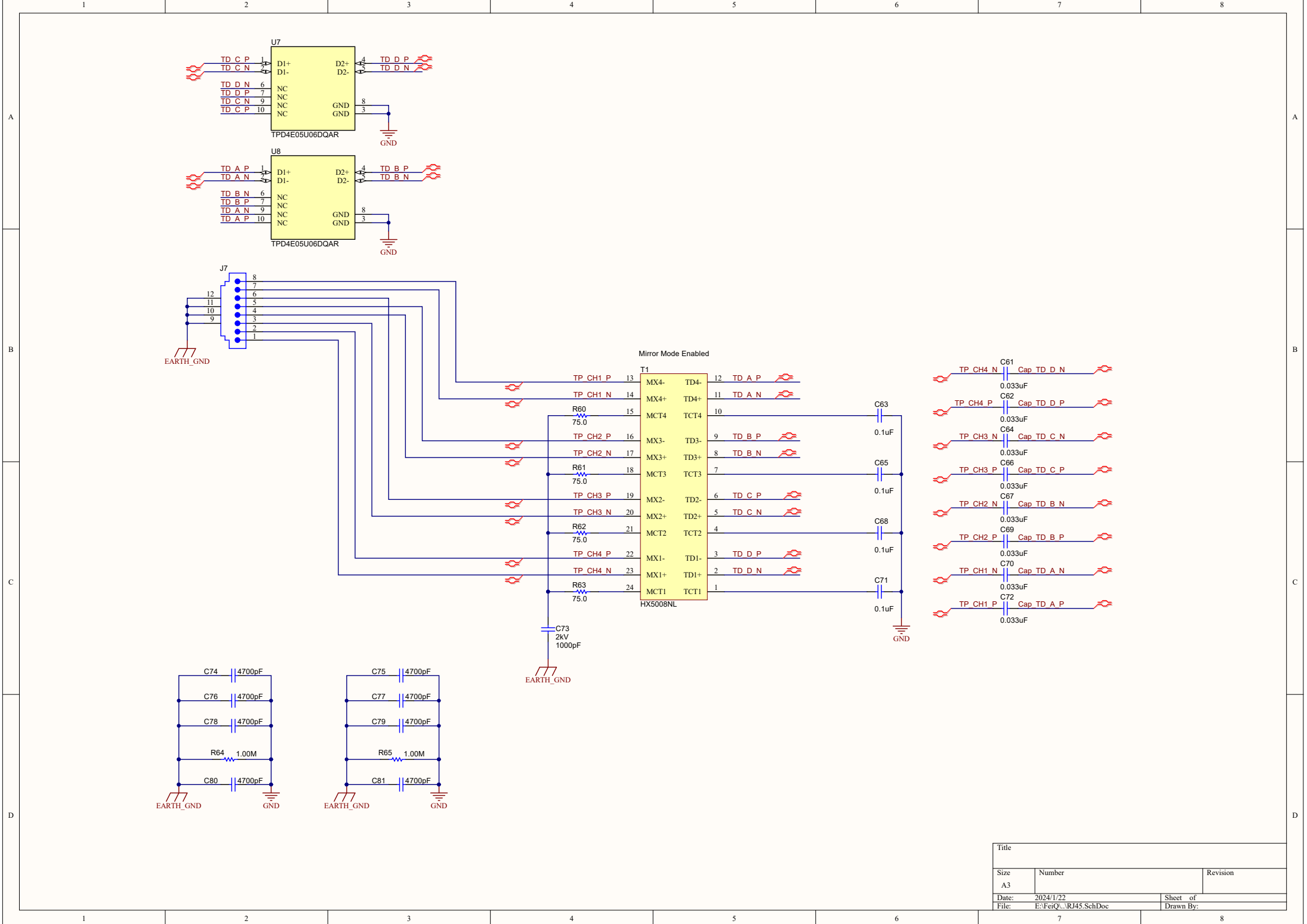
INT_PWDN	R1	0	1	2
MCU_RESET	R2	0	3	4
RX_CTRL	R3	0	5	6
TX_CTRL	R4	0	7	8
RX_D3	R5	0	9	10
TX_D3	R6	0	11	12
RX_D2	R7	0	13	14
TX_D2	R8	0	15	16
RX_D1	R9	0	17	18
TX_D1	R10	0	19	20
RX_D0	R11	0	21	22
TX_D0	R12	0	23	24
RX_CLK	R13	0	25	26
GTX_CLK	R14	0	27	28
			29	30

Orderable:	EVM orderable	Designed for:	PRJ Customer	Mod. Date:	2023/4/25
TID #:	TID	Project Title:	PRJ Title		
Number:	PRJ Number	Rev:	SCH	Sheet Title:	
SVN Rev:	Not in version control	Assembly Variant:	[No Variations]	Sheet:	2 of 7
Drawn By:		File:	DP83869_SchDoc	Size:	B
Engineer:	PRJ Engineer	Contact:	TechSupport		

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Title		
Size	Number	Revision
A3		
Date:	2024/1/22	Sheet of
File:	E:\FeiQ...\Power.SchDoc	Drawn By:



Title		
Size A3	Number	Revision
Date: 2024/1/22	Sheet of	
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