Schematic Review Form

Customer/Project

Pin #	Name	Info	Violations	*Description*
7,8	OUTA+/-	AC coupling present		Inverting and non-inverting CML-compatible differential outputs. Outputs require AC coupling
20,19	OUTB+/-	AC coupling present		Inverting and non-inverting CML-compatible differential outputs. Outputs require AC coupling
24,23	INA+/-	AC coupling present		Inverting and non-inverting CML-compatible differential inputs. An on-chip 100 Ω terminating resistor connects INA+ to INA-. Inputs require AC coupling. TI recommends 100 nF capacitors. Note that for SFP+ applications, AC coupling is included as part of the SFP+ module.
11,12	INB+/-	AC coupling present		Inverting and non-inverting CML-compatible differential inputs. An on-chip 100 Ω terminating resistor connects INB+ to INB-. Inputs require AC coupling. TI recommends 100 nF capacitors. Note that for SFP+ applications, AC coupling is included as part of the SFP+ module.
2,1	LPF_CP_A, LPF_REF_A	Good		Loop filter connection, place a 22 nF ± 10% capacitor in series between LPF_CP_A and LPF_REF_A
17,18	LPF_CP_B, LPF_REF_B	Good		Loop filter connection, place a 22 nF ± 10% capacitor in series between LPF_CP_B and LPF_REF_B
14	REFCLK_IN		Schematic shows 50 MHz clock	25 MHz ± 100 ppm clock from external Oscillator
16	LOCK	Good		LOCK VOH is referenced to VIN voltage level. Note that this pin is shared with strap input functions read at startup. The Address value loaded into pin 16 (ADDR0) at startup changes the definition of the LOCK pin output. See the

				Shared Register Definition in Table 7 for more details.
13	LOS/INT#		Open drain outputs should use a pullup resistor.	Output is driven LOW when a valid signal is present on INA. Output is released when signal on INA is lost (LOS). This output can be redefined as an INT# signal which will be driven LOW for any of the following conditions. 1. The EOM check returns a value below the HEO/VEO interrupt threshold. 2. CDR check returns lock/loss status. 3. Signal Detector returns detect/loss status. The LOS/INT# pin is an open drain output which requires external pull-up resistor typically connected to 2.5 V or 3.3 V for system logic compatibility) to achieve a HIGH level.
3	ENSMB		Schematic seems to show ENSMB is LOW, which selects pin control mode. However, SCL/SDA are populated like SMBus target (slave) mode will be used. Will review schematic assuming SMBus target mode is intended.	System Management Bus (SMBus) enable pin HIGH = Register Access, SMBus Slave mode FLOAT = SMBus Master read from External EEPROM 20 K to GND = Reserved LOW = External Pin Control Mode. See section on Pin Mode Limitation
4	SDA	2k PU, good		Data Input / Open Drain Output External pull-up resistor is required. Pin is 3.3 V LVCMOS tolerant
5	SCL	2k PU, good		Clock input in SMBus slave mode. Can also be an open drain output in SMBus master mode Pin is 3.3 V LVCMOS Tolerant
6	TX_DIS	1k PD, good. Selects output enabled.		Disable the OUTB transmitter HIGH = OUTA Enabled/OUTB Disabled FLOAT = Reserved

				20 K to GND = Reserved LOW = OUTA/OUTB Enabled (normal operation)
16	ADDR0	1k PD		This pin sets the SMBus address for the retimer. This pin is a strap input. The state is read on power-up to set the SMBus address in SMBus control mode. The latched value of ADDR0 read at startup will change the LOCK output definition. See the Shared Register Definition in Table 7 for more details.
10	ADDR1/DONE#	1k PD, selects SMBus address 0x30		This pin sets the SMBus address for the retimer in SMBus Slave Mode. DONE#. VOH is referenced to VIN voltage level. DONE# goes low to indicate that the SMBus master EEPROM read has been completed in SMBus Master Mode
9	READEN#	1k PD, good for SMBus target mode.		Initiates SMBus master EEPROM read. When multiple DS125DF111 are connected to a single EEPROM, the READEN# input can be daisy chained to the DONE# output. In SMBus Slave Mode this pin should be tied to Logic 0.
4	DEMA	N/A, using SMBus target mode		Set CHA output de-emphasis level in pin control mode
5	DEMB	N/A, using SMBus target mode		Set CHB output de-emphasis level in pin control mode
6	LPBK	N/A, using SMBus target mode		HIGH = INA goes to OUTA, INB goes to OUTB FLOAT = INB goes to OUTA and OUTB 20 K to GND = INA goes to OUTA and OUTB LOW = INA goes to OUTB, INB goes to OUTA
9	VODA	N/A, using SMBus target mode		Set CHA output launch amplitude in pin control mode
10	VODB	N/A, using SMBus target mode		Set CHB output launch amplitude in pin control mode
21,22	VDD	Bypass caps good		VDD = 2.5 V ± 5%. See Figure 12. 3.3-V supply mode: VDD = 2.5 V is supplied the internal output regulator. Pins only require de-

				coupling caps; no external supply is needed. 2.5-V supply mode: VDD input = 2.5 V ± 5%.
15	VIN	Bypass caps good		Regulator Input with Integrated Supply Mode Control. See Figure 12. 3.3-V supply mode: VIN input = 3.3 V ± 10%. 2.5-V Mode Operation: VIN Supply Input = 2.5 V ± 5%. Connect directly to VDD supply pins.
PAD	DAP	GND, good		GND reference The exposed pad at the center of the package must be connected to ground plane of the board with at least 4 vias to lower the ground impedance and improve the thermal performance of the package

Comments