**1920x720 Display Bringup**

1. We are using ti-ds90ub941as-q1.c driver for serialiser, ti-ds90ub948-q1.c for deserialiser and ti-fpdlink.c as a bridge driver. ti-fpdlink will act as a bridge in between processor and serialiser/Deserilaiser
2. Following are the device tree changes added for IC Display.

&i2c0\_mipi0 {

#address-cells = <1>;

#size-cells = <0>;

pinctrl-names = "default";

pinctrl-0 = <&pinctrl\_mipi0\_lpi2c0>;

clock-frequency = <100000>;

status = "okay";

fpdlink\_serializer\_i2c0: serializer@0e {

compatible = "ti,ds90ub941as\_q1";

reg = <0x0e>;

reg\_config = <0x01 0x08 0x1E 0x01 0x03 0x9A 0x1E 0x01 0x40 0x05 0x41 0x21 0x42 0x60 0x1E 0x01 0x5B 0x03 0x4F 0x8C 0x1E 0x01 0x40 0x04 0x41 0x05 0x42 0x0E 0x03 0x9A 0x01 0x08 0x17 0x9E 0x01 0x00>;

status = "okay";

};

fpdlink\_deserializer\_i2c0: deserializer@2c {

compatible = "ti,ds90ub948\_q1";

reg = <0x2c>;

reg\_config = <0x49 0x62 0x20 0x90 0x1F 0x09 0x1D 0x19 0x1E 0x90>;

status = "okay";

fpdlink\_lvds\_dic: fpdlink\_bridge@100 {

compatible = "ti,fpdlink";

ti,dsi-lanes = <4>;

ti,lvds-format = <1>;

ti,lvds-bpp = <24>;

ti,width-mm = <508>;

ti,height-mm = <190>;

fpdlink-serializer-i2c-handle = <&fpdlink\_serializer\_i2c0>;

fpdlink-deserializer-i2c-handle = <&fpdlink\_deserializer\_i2c0>;

status = "okay";

display-timings {

native-mode = <&timing0>;

timing0: 1920X720\_50HZ {

clock-frequency = <75193600>;

hactive = <1920>;

vactive = <720>;

hfront-porch = <40>;

vfront-porch = <31>;

hback-porch = <16>;

vback-porch = <5>;

hsync-len = <8>;

vsync-len = <2>;

};

};

port@0 {

reg = <0>;

bridge\_in: endpoint {

remote-endpoint = <&mipi0\_host\_out>;

};

};

};

};

};

&mipi0\_dphy {

status = "okay";

};

&mipi0\_dsi\_host {

status = "okay";

ports {

port@1 {

reg = <1>;

mipi0\_host\_out: endpoint {

remote-endpoint = <&bridge\_in>;

};

};

};

};

1. We are able to detect serialiser and deserialiser in the mipi0 i2c bus with address 0x0e and 0x2c respectively. And the backlight is turning ON.

Text

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1. MODE\_SEL0, MODE\_SEL1 and IDX hardware configuration of serialiser daughter is as shown below.

Graphical user interface, application

Description automatically generated

IDX address is configured to be 0x0C [ hardware side ] but we are getting 0x0E in i2cdetect

Command.

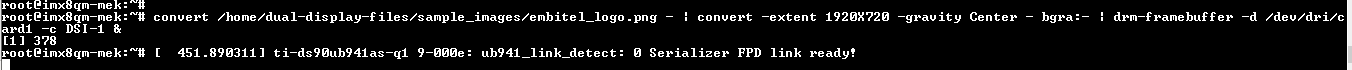
1. MODE\_SEL0 and MODE\_SEL1 hardware configurations are set for single OLDI with MAPSEL=H and STP cable with 5Mbps Back channel respectively as shown below.(same configurations for both IVI and IC display)

Table

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1. On the deserialiser side LOCK Pin and PDB are shown as HIGH.
2. Run drm-framebuffer command as shown below.

*convert /home/dual-display-files/sample\_images/embitel\_logo.png - | convert -extent 1920X720 -gravity Center - bgra:- | drm-framebuffer -d /dev/dri/card1 -c DSI-1 &*



1. Run Modetest commands

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1. Test pattern generation using pattern generation registers. We are able to generate pattern using internal pattern generation register configuration

#Serializer configuration for pattern generation:

i2cset -y -f 9 0x0e 0x01 0x08

i2cset -y -f 9 0x0e 0x1E 0x01

i2cset -y -f 9 0x0e 0x66 0x0F

i2cset -y -f 9 0x0e 0x67 0x1E

i2cset -y -f 9 0x0e 0x66 0x10

i2cset -y -f 9 0x0e 0x67 0x03

i2cset -y -f 9 0x0e 0x66 0x11

i2cset -y -f 9 0x0e 0x67 0x43

i2cset -y -f 9 0x0e 0x66 0x12

i2cset -y -f 9 0x0e 0x67 0x05

i2cset -y -f 9 0x0e 0x66 0x03

i2cset -y -f 9 0x0e 0x67 0x03

i2cset -y -f 9 0x0e 0x66 0x07

i2cset -y -f 9 0x0e 0x67 0x80

i2cset -y -f 9 0x0e 0x66 0x08

i2cset -y -f 9 0x0e 0x67 0x07

i2cset -y -f 9 0x0e 0x66 0x09

i2cset -y -f 9 0x0e 0x67 0x2D

i2cset -y -f 9 0x0e 0x66 0x04

i2cset -y -f 9 0x0e 0x67 0xD0

i2cset -y -f 9 0x0e 0x66 0x05

i2cset -y -f 9 0x0e 0x67 0xD7

i2cset -y -f 9 0x0e 0x66 0x06

i2cset -y -f 9 0x0e 0x67 0x2D

i2cset -y -f 9 0x0e 0x66 0x0C

i2cset -y -f 9 0x0e 0x67 0x20

i2cset -y -f 9 0x0e 0x66 0x0D

i2cset -y -f 9 0x0e 0x67 0x05

i2cset -y -f 9 0x0e 0x66 0x0A

i2cset -y -f 9 0x0e 0x67 0x10

i2cset -y -f 9 0x0e 0x66 0x0B

i2cset -y -f 9 0x0e 0x67 0x02

i2cset -y -f 9 0x0e 0x66 0x0E

i2cset -y -f 9 0x0e 0x67 0x03

i2cset -y -f 9 0x0e 0x65 0x05

i2cset -y -f 9 0x0e 0x64 0x11

i2cset -y -f 9 0x0e 0x01 0x00

A picture containing indoor

Description automatically generatedA picture containing text

Description automatically generated

1. We also tried multiple clock frequencies and timing values as per the typical value given in the below table.

Table

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1. Also tried with following clock frequency (207Mhz)and timing parameters.

clock-frequency = <207000000>;

hactive = <1920>;

vactive = <720>;

hfront-porch = <40>;

vfront-porch = <31>;

hback-porch = <16>;

vback-porch = <5>;

hsync-len = <8>;

vsync-len = <2>;

1. After Bootup is completed IC display will be as shown below. Only backlight is turned ON.



1. Then, After doing DSI reset using i2c commands as given below, we are getting images like as shown below.

i2cset -y -f 9 0x0e 0x01 0x08 🡪 Disable DSI

i2cset -y -f 9 0x0e 0x01 0x00 🡪 Enable DSI

A picture containing text, oven

Description automatically generated

1. Then after running modetest command, we are getting images as shown below.

Text

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A picture containing text

Description automatically generated

NOTE:

These Images are all getting for clock-frequency 207Mhz (frequencies in the range 200Mhz-217Mh also). For frequencies in the range 60-100 Mhz we only getting blank screen with backlight turned ON as shown in the image in step 10a), for every scenarios (after bootup, after DSI reset, after modetest).

1. For 1280x720 display we used the following timing parameters and clock frequency, and It is working fine in the bootup itself(without any DSI reset). We used the same drivers for both IC and IVI displays, only changes are the timing parameters and clock frequency.

timing1: 1280X720\_60HZ {

clock-frequency = <69676800>;

hactive = <1280>;

vactive = <720>;

hfront-porch = <80>;

vfront-porch = <16>;

hback-porch = <80>;

vback-porch = <14>;

hsync-len = <80>;

vsync-len = <14>;

de-active = <1>;

};

A close-up of a computer screen

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