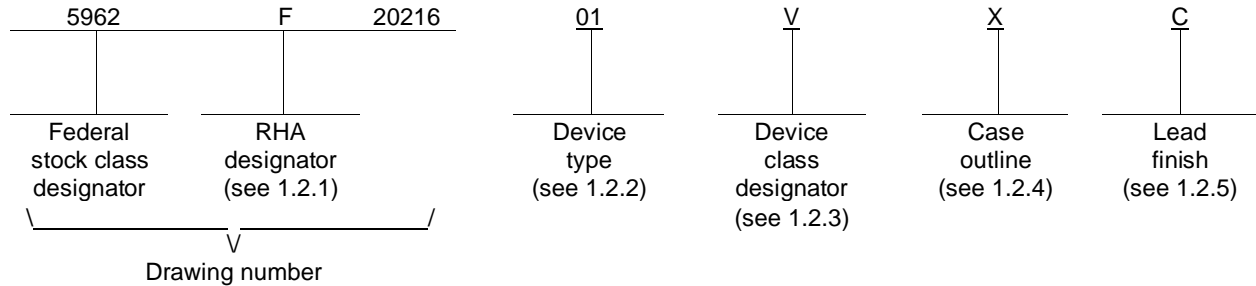| REVISIONS				
LTR	DESCRIPTION		DATE (YR-MO-DA)	APPROVED
A	Remove parameters with typical values from Table 1A. - TTM		22-05-20	Muhammad A. Akbar

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

Revision Status of Sheets

REV	A	A	A																			
SHEET	23	24	25																			
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

PMIC N/A

STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	PREPARED BY Taysa Markus	**DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/LandandMaritime**		
	CHECKED BY Taysa Markus			
	APPROVED BY Muhammad Akbar	MICROCIRCUIT, RADIATION HARDENED, HIGH IMMUNITY, 10/100/1000 MB/S ETHERNET PHYSICAL LAYER TRANCEIVER, MONOLITHIC SILICON		
	DRAWING APPROVAL DATE 21-11-10			
	REVISION LEVEL A	SIZE A	CAGE CODE **67268**	**5962-20216**
		SHEET 1 OF 25		

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5962-E216-22

1. SCOPE

1.1 <u>Scope</u>. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 <u>PIN</u>. The PIN is as shown in the following example:

```
   5962          F        20216          01              V              X              C
     |           |          |             |              |              |              |
  Federal       RHA                     Device         Device         Case          Lead
 stock class  designator               type           class          outline       finish
 designator   (see 1.2.1)              (see 1.2.2)    designator      (see 1.2.4)    (see 1.2.5)
                                                      (see 1.2.3)
     _____/
                    V
              Drawing number
```

1.2.1 <u>RHA designator</u>. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 <u>Device type(s)</u>. The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	DP83561-SP	High immunity 10/100/1000 Mbps Ethernet physical layer transceiver.

1.2.3 <u>Device class designator</u>. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 <u>Case outline(s)</u>. The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	64	Ceramic quad flat pack (CQFP)

1.2.5 <u>Lead finish</u>. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

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1.3 Absolute maximum ratings. 1/ 2/ 3/ 4/

    Power supply voltage (AVDD 2.5 V) .... -0.3 to 3.0 V
    Power supply voltage (AVDD 1.8 V) .... -0.3 to 2.16 V
    Power supply voltage (AVDD 1.1 V) .... -0.3 to 1.4 V
    Power supply voltage (VDDIO 3.3 V option) .... -0.3 to 3.8 V
    Power supply voltage (VDDIO 2.5 V option) .... -0.3 to 3.0 V
    Power supply voltage (VDDIO 1.8 V option) .... -0.3 to 2.1 V
    Maximum junction temperature (T_J) .... 150°C
    Storage temperature range (T_{STG}) .... -65°C to 150°C
    PINS media dependent interface (MDI) .... -0.3 to 6.5 V
    PINS (MAC interface, MDIO, MDC, GPIO) .... -0.3 to VDDIO+0.3 V
    PINS (EN, RESET_N) .... -0.3 to VDDIO+0.3 V
    Electrostatic discharge (ESD) rating: 5/ 6/
        Human-body model (HBM), All Pins except MDI Pins 2/ .... ±2500 V
        Human-body model (HBM), MDI Pins   .... ±8000 V
        IEC 61000-4-2 contact discharge, MDI Pins .... ±8000 V
    Thermal characteristics: 7/
    Thermal resistance, junction-to-ambient ($R_{\theta JA}$) .... 22.5°C/W
    Thermal resistance, junction-to-case, top ($R_{\theta JC(top)}$) .... 7.4°C/W
    Thermal resistance, junction-to-case, bottom ($R_{\theta JC(bot)}$) .... 1.1°C/W
    Thermal resistance, junction-to-board($R_{\theta JB}$) .... 8.1°C/W
    Junction-to-top characterization parameter, (Ψ_{JT}) .... 2°C/W
    Junction-to-board characterization parameter (Ψ_{JB}) .... 7.8°C/W

1.4 Recommended operating conditions.

    Power supply voltage (2.5 V analog supply)... +2.375 V to +2.625 V
    Power supply voltage (1.8 V analog supply)... +1.710 V to +1.890 V
    Power supply voltage (1.1 V digital supply).. +1.045 V to +1.155 V
    Power supply voltage (VDDIO 3.3 V option).. +3.145 V to +3.465 V
    Power supply voltage (VDDIO 2.5 V option).. +2.375 V to +2.625 V
    Power supply voltage (VDDIO 1.8 V option).. +1.710 V to +1.890 V
    Operating free air temperature range (T_A) .... -55°C to +125°C

_____

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the
    maximum levels may degrade performance and affect reliability.
2/ All voltages are measured with respect to ground terminal.
3/ Short-circuits can cause excessive heating. Destructive dissipation can result from short-circuits on outputs.
4/ Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant
    to imply that the device should be operated at these limits.
5/ JEDEC document JEP155 states that 500-V HBM allow s safe manufacturing with a standard ESD control process.
    Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±8 V and/or ±2 V may
    actually have higher performance.
6/ JEDEC document JEP157 states that 250-V CDM allow s safe manufacturing with a standard ESD control process.
    Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±500 V may actually have
    higher performance.
7/ For more information about traditional and new thermal metrics, see Texas Instruments *IC Package Thermal Metrics*
    application report, SPRA953.

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1.5 <u>Radiation features</u>.

Maximum total dose available (high dose rate = 50 – 300 rad(Si)/s) .... 300 krads(Si)   <u>1</u>/

Heavy ion single event phenomenon (SEP):
No Single event latch-up (SEL) occurs at effective LET (see 4.4.5.3) $\leq$ 121 MeV·cm^2/mg   <u>2</u>/

—————

<u>1</u>/ The manufacturer supplying device type 01 has performed characterization testing in accordance with MIL-STD-883 method 1019, condition A to a maximum total dose of 300 krads(Si). The radiation end points limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 300 krads(Si).

<u>2</u>/ Heavy ion single event effects (SEE) test was performed at the TAMU Cyclotron Radiation Effects facility using a superconducting cyclotron and an advanced electron cyclotron resonance (ECR) ion source. No single event latch-up (SEL) was observed under ^{197}Au ions at angle 43° at Vmax supply voltages and operating temperature 125°C corresponding to an effective LET of 121 MeV·cm^2/mg. For more information on SEP test results, customers are requested to contact the manufacturer.

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2. APPLICABLE DOCUMENTS

2.1 <u>Government specification, standards, and handbooks</u>. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

   DEPARTMENT OF DEFENSE SPECIFICATION

      MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

   DEPARTMENT OF DEFENSE STANDARDS

      MIL-STD-883 - Test Method Standard Microcircuits.
      MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

   DEPARTMENT OF DEFENSE HANDBOOKS

      MIL-HDBK-103 - List of Standard Microcircuit Drawings.
      MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

2.2 <u>Non-Government publications</u>. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

   ASTM INTERNATIONAL (ASTM)

      ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP, SEU) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

   JEDEC Solid State Technology Association

      JEDEC PUB 95 - Registered and Standard Outlines for Semiconductor Devices
      JEDEC JEP 163 - Selection of burn-in/life test conditions and critical parameters for QML microcircuits

(Copies of these documents are available online at https://www.jedec.org/.)

   ANSI/ESDA/JEDEC JOINT STANDARD

      ANSI/ESDA/JEDEC JS-001 - For Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM)
                             - Component Level.
      ANSI/ESDA/JEDEC JS-002 - For Electrostatic Discharge Sensitivity Testing – Charged Device Model (CDM)
                             - Device Level.

(Non-Government standards and other publications are normally available from the organizations that prepare of distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 <u>Order of precedence</u>. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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3. REQUIREMENTS

3.1 <u>Item requirements</u>. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 <u>Design, construction, and physical dimensions</u>. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 <u>Case outline</u>. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 <u>Terminal connections</u>. The terminal connections shall be as specified on figure 2.

3.2.3 <u>Block diagram</u>. The block diagram shall be as specified on figure 3.

3.2.4 <u>Power up timing</u>. The power up timing shall be as specified on figure 4.

3.2.5 <u>Reset timing.</u> The reset timing shall be as specified on figure 5.

3.2.6 <u>100-Mbps MII transmit timing.</u> The 100-Mbps MII transmit timing shall be as specified on figure 6.

3.2.7 <u>100-Mbps MII receive timing.</u> The 100-Mbps MII receive timing shall be as specified on figure 7.

3.2.8 <u>RGMII transmit multiplexing and timing diagram.</u> The RGMII transmit multiplexing and timing diagram shall be as specified on figure 8.

3.2.9 <u>RGMII receive multiplexing and timing diagram.</u> The RGMII receive multiplexing and timing diagram shall be as specified on figure 9.

3.2.10 <u>Serial management interface timing.</u> The serial management interface timing shall be as specified on figure 10.

3.2.11 <u>Radiation exposure circuit</u>. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 <u>Electrical performance characteristics and postirradiation parameter limits</u>. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 <u>Electrical test requirements</u>. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 <u>Marking</u>. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 <u>Certification/compliance mark</u>. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 <u>Certificate of compliance</u>. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 <u>Certificate of conformance</u>. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

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TABLE IA. <u>Electrical performance characteristics</u>.

Test	Symbol	Conditions 1/ 3/ -55°C ≤ T_A ≤ +125°C 1.1V ≤ AVDD ≤ +2.5V unless otherwise specified	Group A subgroups	Limits		Test
				Min	Max	
IEEE Tx conformance (1000BaseT)						
Output differential voltage		Normal mode, all channels	1,2,3	0.67	0.82	V
IEEE Tx conformance (100BaseTx)						
Output differential voltage 2/		Normal mode, channels A and B	1,2,3	0.95	1.05	V
Bootstrap DC characteristics (4 level) (PHY address pins)						
Mode 0 strap voltage range	V_{MODE0}		1,2,3	0	0.093xVDDIO	V
Mode 1 strap voltage range	V_{MODE1}		1,2,3	0.136x VDDIO	0.184x VDDIO	V
Mode 2 strap voltage range	V_{MODE2}		1,2,3	0.219x VDDIO	0.280x VDDIO	V
Mode 3 strap voltage range	V_{MODE3}		1,2,3	0.600x VDDIO	0.888x VDDIO	V
Bootstrap DC characteristics (2 level)						
Mode 0 strap voltage range	V_{MODE0}		1,2,3	0	0.18x VDDIO	V
Mode 1 strap voltage range	V_{MODE1}		1,2,3	0.50x VDDIO	0.88x VDDIO	V
IO characteristics						
High level input voltage	V_{IH}	VDDIO = 3.3V ±5%	1,2,3	2		V
Low level input voltage	V_{IL}	VDDIO = 3.3V ±5%	1,2,3		0.8	V
high level output voltage	V_{OH}	I_{OH} = -2mA, VDDIO = 3.3V ±5%	1,2,3	2.4		V
Low level output voltage	V_{OL}	I_{OL} = 2mA, VDDIO = 3.3V ±5%	1,2,3		0.4	V
High level input voltage	V_{IH}	VDDIO = 2.5V ±5%	1,2,3	1.7		V
Low level input voltage	V_{IL}	VDDIO = 2.5V ±5%	1,2,3		0.7	V
high level output voltage	V_{OH}	I_{OH} = -2mA, VDDIO = 2.5V ±5%	1,2,3	2		V
Low level output voltage	V_{OL}	I_{OL} = 2mA, VDDIO = 2.5V ±5%	1,2,3		0.4	V
High level input voltage	V_{IH}	VDDIO = 1.8V ±5%	1,2,3	0.65* VDDIO		V
Low level input voltage	V_{IL}	VDDIO = 1.8V ±5%	1,2,3		0.35* VDDIO	V
high level output voltage	V_{OH}	I_{OH} = -2mA, VDDIO = 1.8V ±5%	1,2,3	VDDIO-0.45		V
Low level output voltage	V_{OL}	I_{OL} = 2mA, VDDIO = 1.8V ±5%	1,2,3		0.45	V

See footnotes at end of table.

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TABLE IA. <u>Electrical performance characteristics</u> – Continued.

Test	Symbol	Conditions 1/ 3/ -55°C ≤ T$_A$ ≤ +125°C 1.1V ≤ AVDD ≤ +2.5V unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
IO characteristics – Continued						
Input high current	I$_{IH}$	Input high current	1,2,3	-55	55	µA
Input low current	I$_{IL}$	T$_A$ = -55°C to 125°C, V$_{IN}$ = GND	1,2,3	-35	35	µA
Tri-state output high current	I$_{OZH}$	T$_A$ = -55°C to 125°C, V$_{OUT}$=GND	1,2,3	-55	55	µA
Tri-state output low current	I$_{OZL}$	T$_A$ = -55°C to 125°C, V$_{OUT}$=GND	1,2,3	-35	35	µA
Internal pull down resistor	R$_{PULLDN}$		1,2,3	6.75	11.25	kΩ
High level input voltage	XI V$_{IH}$		1,2,3	1.2	VDDIO	V
Low level input voltage	XI V$_{IL}$		1,2,3		0.6	V
Power-up timing (2, 3 supply mode)						
Supply ramp rate: For all supplies			9,10,11	0.5	100	ms
Supply ramp delay offset: For all supplies			9,10,11	0	50	ms
Last supply power rail ramp to RESET_N	T1		9,10,11	200		ms
Reset timing						
Reset to SMI ready: Post reset stabilization time prior to MDC preamble for register access	T1		9,10,11	30		µs
RESET PULSE width: minimum reset pulse width to be able to reset	T3		9,10,11	720		ns
MII 100M timing						
TX_CLK high/low time	T1		9,10,11	16	24	ns
TX_D[3:0], TX_ER, TX_EN setup to TX_CLK	T2		9,10,11	10		ns
TX_D[3:0], TX_ER, TX_EN hold from TX_CLK	T3		9,10,11	0		ns
RX_CLK high/low time	T1		9,10,11	16	24	ns
RX_D[3:0], RX_DV delay from RX_CLK rising	T2		9,10,11	10	30	ns

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 3/ -55°C ≤ TA ≤ +125°C 1.1V ≤ AVDD ≤ +2.5V unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
RGMII output timing (1G)						
Data to clock output skew (non-delay mode)	T_{skewT}		9,10,11	-600	625	ps
Data to clock output setup (delay mode: 2 ns default)	T_{skewT} (delay)		9,10,11	1.5	2.5	ns
Data to clock output setup (delay mode)	T_{setupT}		9,10,11	1.2		ns
Data to clock output hold (delay mode)	T_{holdT}		9,10,11	1.2		ns
Clock cycle duration	T_{cyc}		9,10,11	7.2	8.8	ns
Duty cycle			9,10,11	45	58	%
Rise / Fall time (20% to 80%)			9,10,11		0.85	ns
RGMII input timing (1G)						
TX data to clock input setup	T_{setupR}		9,10,11	1		ns
TX clock to data input hold	T_{holdR}		9,10,11	1		ns
SMI timing						
MDC to MDIO (Output) delay time (25 pF load)	T1		9,10,11	0	20	ns
MDIO (Input) to MDC setup time	T2		9,10,11	10		ns
MDIO (Input) to MDC hold time	T3		9,10,11	10		ns
MDC frequency (25 pF load)	T4		9,10,11		24	MHz
Output clock timing (25 MHz clkout)						
Frequency (PPM)			9,10,11	-100	100	-
Duty cycle			9,10,11	40	60	%
25 MHz input clock tolerance						
Frequency tolerance			9,10,11	-100	+100	ppm
Rise / fall time (10% - 90%)			9,10,11		8	ns
Duty cycle			9,10,11	40	60	%

1/ Power dissipation measurements: Traffic: 100%, packet size: 1512, random content, temperature: -55 to 125°C, voltage range: ±5%.

2/ In mirror mode, channel D & C are used for Tx and Rx. Please refer to mirror mode selection for additional configuration, for output differential voltage.

3/ For RGMII interface, please refer to RGMII timing and IBIS mode based signal integrity simulation (add reference to section).

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TABLE IB. SEP test limits. 1/ 2/ 3/

Device type	Bias VDDIO = 3.465 V for SEL test 4/ No SEL occurs at effective LET
All	LET $\leq$ 121 MeV·cm^2/mg

1/ For single event phenomena (SEP) test conditions, see 4.4.5.3 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by TRB and qualifying activity.
3/ Heavy ion single event effects (SEE) test was performed at the TAMU Cyclotron Radiation Effects facility using a superconducting cyclotron and an advanced electron cyclotron resonance (ECR) ion source. No single event latch-up (SEL) was observed under ^{197}Au ions at angle 43° at Vmax supply voltages and operating temperature 125°C corresponding to an effective LET of 121 MeV·cm^2/mg. For more information on SEP test results, customers are requested to contact the manufacturer.
4/ Tested for latch-up at worst case temperature, TA = +125°C ± 10°C.

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		REVISION LEVEL **A**	SHEET **10**
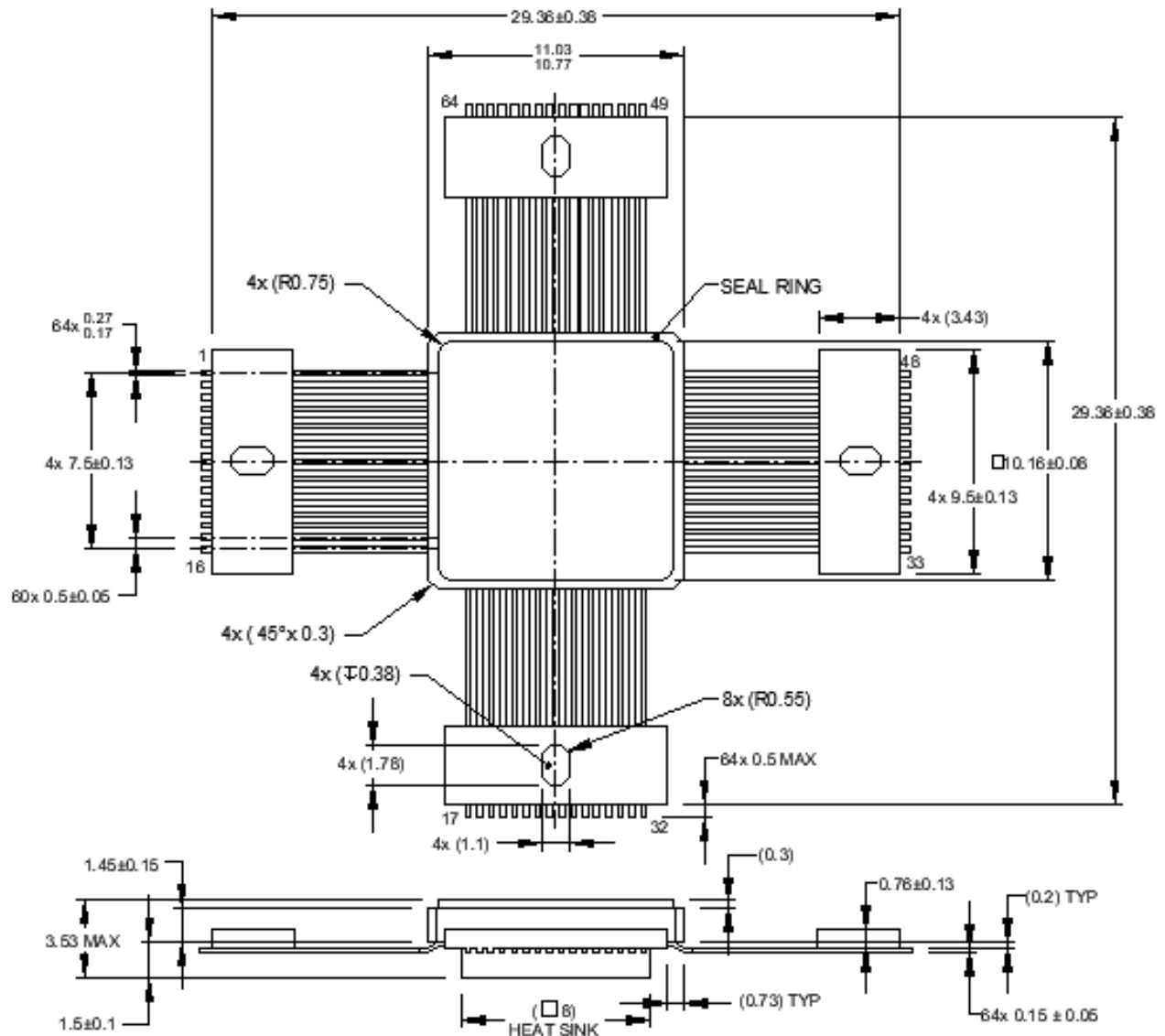
DSCC FORM 2234
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FIGURE 1. Case outline X.

8 ±0.13
HEAT SINK

PIN 1 ID

BOTTOM VIEW

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only.
   Dimensioning and tolerancing per ASME Y14.5M.
2. This package is hermetically sealed with a metal lid.
3. Ground pad to be electronic connected to heat sink and seal ring.
4. The leads are gold plated and can be solder dipped.

FIGURE 1. Case outline X – Continued.
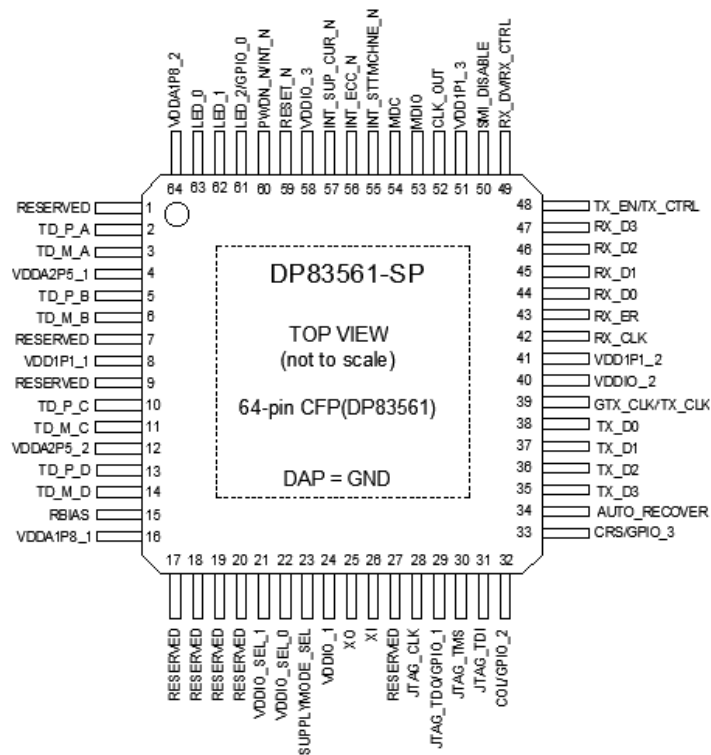
FIGURE 2. Terminal connections.

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PIN		I/O	TYPE	DESCRIPTION
NO.	NAME			
1	Reserved	I/O		Reserved. Keep it NC.
2	TD_P_A	I/O	A	Differential transmit and receive signals.
3	TD_M_A	I/O	A	Differential transmit and receive signals.
4	VDDA2P5_1	I	A	2.5-V analog supply (±5%). Each pin requires a 1-µF and 0.1-µF capacitor to GND.
5	TD_P_B	I/O	A	Differential transmit and receive signals.
6	TD_M_B	I/O	A	Differential transmit and receive signals.
7	Reserved	I	A	Reserved. Keep it NC.
8	VDD1P1_1	I	A	1.1-V digital supply (±5%). Each pin requires a 1-µF and 0.1-µF capacitor to GND.
9	Reserved	I	A	Reserved. Keep it NC.
10	TD_P_C	I/O	A	Differential transmit and receive signals.
11	TD_M_C	I/O	A	Differential transmit and receive signals.
12	VDDA2P5_2	I	A	2.5-V analog supply (±5%). Each pin requires a 1-µF and 0.1-µF capacitor to GND.
13	TD_P_D	I/O	A	Differential transmit and receive signals.
14	TD_M_D	I/O	A	Differential transmit and receive signals.
15	RBIAS	I	A	Bias resistor connection. An 10-kΩ ±1% resistor should be connected from RBIAS to GND. A 90-pF ±10% capacitor should be connected in parallel with the bias resistor.
16	VDDA1P8_1	I	A	In three-supply mode, an external 1.8-V (±5%) supply can be connected to these pins. When using an external supply, each pin requires a 1-µF and 0.1-µF capacitor to GND. In two supply mode, no external supply is required for this pin. When unused, no connections should be made to these pins.
17	Reserved	—	A	Reserved. Keep it NC.
18	Reserved	—	A	Reserved. Keep it NC.
19	Reserved	—	A	Reserved. Keep it NC.
20	Reserved	—	A	Reserved. Keep it NC.
21	VDDIO_SEL_1	I	A, S	VDDIO_SEL1/VDDIO_SEL0: 00 (default): VDDIO 3V3 01: Reserve
22	VDDIO_SEL_0	I	A, S	10: VDDIO 2V5 11: VDDIO 1V8
23	SUPPLYMODE_SEL		S	0 = Dual supply mode (VDDA1P8 left floating) (Default) 1 = Triple supply mode (VDDA1P8 supplied by system)
24	VDDIO_1	I	A	I/O power: 1.8V (±5%), 2.5V (±5%) or 3.3V (±5%). Each pin requires a 1-µF and 0.1-µF capacitor to GND
25	XO	O	A	CRYSTAL OSCILLATOR OUTPUT: Second terminal for 25-MHz crystal. Must be left floating if a clock oscillator is used.

FIGURE 2. Terminal connections – Continued.

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PIN		I/O	TYPE	DESCRIPTION
NO.	NAME			
26	XI	I	A	CRYSTAL OSCILLATOR INPUT: 25-MHz oscillator or crystal input.
27	Reserved	—	A	Reserved. Keep it NC.
28	JTAG_CLK	I	PU	JTAG TEST CLOCK: IEEE 1149.1 test clock input, primary clock source for all test logic input and output controlled by the testing entity.
29	JTAG_TDO/GPIO_1	O	PD	JTAG TEST DATA OUTPUT: IEEE 1149.1 test data output pin, the most recent test results are scanned out of the device via TDO. General Purpose I/O: This signal provides a multi-function configurable I/O. Please refer to the GPIO_MUX_CTRL register for details. This pin should be pulled down by a 2.49-kΩ resistor.
30	JTAG_TMS	I	PU	JTAG TEST MODE SELECT: IEEE 1149.1 test mode select pin, the TMS pin sequences the tap controller (16-state FSM) to select the desired test instruction. Recommend the user apply 3 clock cycles with JTAG_TMS high to reset the JTAG.
31	JTAG_TDI	I	PU	JTAG TEST DATA INPUT: IEEE 1149.1 Test Data Input pin, test data is scanned into the device through the TDI.
32	COL/GPIO_2	I/O	PD	COLLISION DETECT: Asserted high to indicate detection of a collision condition (assertion of CRS due to simultaneous transmit and receive activity) in half-duplex modes. This signal is not synchronous to either MII clock (GTX_CLK, TX_CLK or RX_CLK). (Default) general purpose I/O: This signal provides a multi-function configurable I/O. Refer to the GPIO_MUX_CTRL register for details.
33	COL/GPIO_3	I/O	PD, S	CARRIER SENSE: CRS is asserted high to indicate the presence of a carrier due to receive or transmit activity in Half-Duplex mode. (Default) General Purpose I/O: This signal provides a multi-function configurable I/O. Please refer to the GPIO_MUX_CTRL register for details.
34	AUTO_RECOVER	I	PD, S	0 = DP8356-SP will take no automatic action based on SEFI. SEFI event interrupts will be generated normally. (Default) 1 = Configures the DP8356-SP to automatically apply RESET signal to PHY logic when a SEFI is detected by one of the monitors configured (STATE_MACHINE, temperature monitor, PLL lock, ECC registers). Default register values will be reloaded and pin options. SEFI event interrupts will be generated normally.
35	TX_D3	I	PD	TRANSMIT DATA: Signal TX_D [3:0] carries data from the MAC to the
36	TX_D2	I	PD	PHY in RGMII mode and MII mode. Data is synchronous to the transmit
37	TX_D1	I	PD	clock.
38	TX_D0	I	PD	
39	GTX_CLK/TX_CLK	I/O	PD/O	RGMII TRANSMIT CLOCK: This continuous clock signal is sourced from the MAC layer to the PHY. Nominal frequency is 125 MHz in 1000-Mbps mode. This pin will be input in RGMII mode. MII TRANSMIT CLOCK: In MII mode, this pin provides a 25-MHz reference clock for 100-Mbps speed and a 2.5-MHz reference clock for 10-Mbps speed. This pin will be output in MII mode. This pin will be GTX_CLK by default and can be changed to TX_CLK by register configurations. Selection of the MII MAC interface also changes the GTX_CLK/TX_CLK selection without any additional register writes needed.

FIGURE 2. Terminal connections - Continued.

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PIN		I/O	TYPE	DESCRIPTION
NO.	NAME			
40	VDDIO_2	I	A	I/O power: 1.8V (±5%), 2.5V (±5%) or 3.3V (±5%). Each pin requires a 1-µF and 0.1-µF capacitor to GND.
41	VDD1P1_2	I	A	1.1-V digital supply (±5%). Each pin requires a 1-µF and 0.1-µF capacitor to GND.
42	RX_CLK	O	PD	RECEIVE CLOCK: Provides the recovered receive clocks for different modes of operation: 125 MHz in 1000-Mbps RGMII mode. 25 MHz in 100-Mbps RGMII/MII mode. 2.5 MHz in 10-Mbps RGMII/MII mode. When PHY is not linked, this pin provides 2.5 MHz clock for both RGMII/MII mode.
43	RX_ER	O	PD	MII Mode: In MII mode this pin will be configured as RX_ER. This pin is asserted high synchronously to rising edge of RX_CLK. Use of this pin is optional.
44	RX_D0	O	PD, S	RECEIVE DATA: Signal RX_D [3:0] carries data from the PHY to the MAC
45	RX_D1	O	PD, S	in RGMII mode and in MII mode. Symbols received on the cable are
46	RX_D2	O	PD	decoded and presented on these pins synchronous to RX_CLK.
47	RX_D3	O	PD	RX_D2 and RX_D3 should be pulled down by a 2.49-kΩ resistor.
48	TX_EN/TX_CTRL	I	PD	TX_EN: In MII mode, this pin will function as TX_EN. TRANSMIT CONTROL: In RGMII mode, TX_CTRL combines the transmit enable and the transmit error signal inputs from the MAC using both clock edges.
49	RX_DV/RX_CTRL	O	PD, S	RX_DV: In MII mode, this pin will function as RX_DV. RECEIVE CONTROL: In RGMII mode, the receive data available and receive error are combined (RXDV_ER) using both rising and falling edges of the receive clock (RX_CLK).
50	SMI_DISABLE	I	PD, S	0 = SMI (MDIO) writes are enabled. (Default) 1 = Station Management Interface (MDIO) writes are disabled.
51	VDD1P1_3	I	A	1.1-V digital supply (±5%). Each pin requires a 1-µF and 0.1-µF capacitor to GND.
52	CLK_OUT	O	O	CLOCK OUTPUT: Output clock
53	MDIO	I/O	—	MANAGEMENT DATA I/O: Bi-directional management instruction/data signal that may be sourced by the management station or the PHY. This open-drain pin requires a 2.2-kΩ pull-up resistor.
54	MDC	I	—	MANAGEMENT DATA CLOCK: Synchronous clock to the MDIO serial management input/output data. This clock may be asynchronous to the MAC transmit and receive clocks. The maximum clock rate is 25-MHz. There is no minimum clock rate.
55	INT_STTMCHNE_N	O	OD	STATE MACHINE INTERRUPT: This pin will be asserted low when an invalid state machine transition, condition, or other invalid condition is detected. When operating this pin as an open-drain interrupt, an external 2.2-kΩ resistor connected to the VDDIO supply is recommended.

FIGURE 2. Terminal connections - Continued.

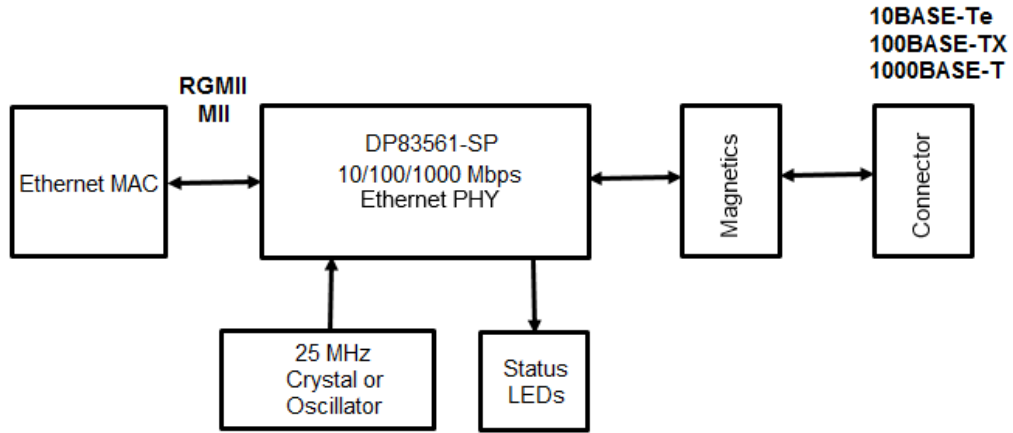| STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-20216
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PIN		I/O	TYPE 2/	DESCRIPTION
NO.	NAME			
56	INT_ECC_N	O	OD	ECC INTERRUPT: This pin will be asserted low when a configuration register error is detected or corrected by register ECC. When operating this pin as an open-drain interrupt, an external 2.2-kΩ connected to the VDDIO supply is recommended.
57	INT_SUP_CUR_N	O	OD	SUPPLY CURRENT INTERRUPT: This pin will be asserted low when an abnormal supply current is detected during normal operation. When operating this pin as an open- drain interrupt, an external 2.2kΩ connected to the VDDIO supply is recommended.
58	VDDIO_3	I	A	I/O Power: 1.8V (±5%), 2.5V (±5%) or 3.3V (±5%). Each pin requires a 1-µF and 0.1-µF capacitor to GND.
59	RESET_N	I	PU, S	RESET_N: This pin is an active-low reset input that initializes or re-initializes all the internal registers of the DP83561-SP. Asserting this pin low for at least 1µs will force a reset process to occur.
60	PWDN_N/INT_N	I/O	PU	PWDN_N (Default): This is an Active Low Input. Asserting this signal low enables the power-down mode of operation. In this mode, the device powers down and consumes minimum power. Register access is available through the Management Interface to configure and power up the device. INT_N: The interrupt pin is an open-drain, active low output signal indicating an interrupt condition has occurred. Register access is required to determine which event caused the interrupt. Recommended to use an external 2.2-kΩ resistor connected to the VDDIO supply. When register access is disabled through pin option, the interrupt will be asserted for 500 ms before self-clearing.
61	LED_2/GPIO_0	O	S	LED_2: This pin is part of the VDDIO voltage domain. Default functionality is RX/TX activity. General Purpose I/O: This signal provides a multi-function configurable I/O. Please refer to the GPIO_MUX_CTRL register for details.
62	LED_1	O	S	LED_1: This pin is part of the VDDIO voltage domain. Default functionality is 1000BT link is up.
63	LED_0	O	S	LED_0: This pin is part of the VDDIO voltage domain. Default functionality is Link OK.
64	VDDA1P8_2	I	A	No external supply is required for this pin in two-supply mode. When unused, no connections should be made to these pins. In three-supply mode, an external 1.8-V (±5%) supply can be connected to these pins. When using an external supply, each pin requires a 1-µF and 0.1-µF capacitor to GND.
DA	DAP 3/	-	GND	DIE ATTACH PAD, connect to GND.

NOTES:

    1/ NC = No connection. Pin may be grounded.
    2/ The functionality of the pins are defined below:
        Type I: input
        Type O: output
        Type I/O: input/output
        Type PD or PU: internal pull-down or pull-up
        Type S: strap configuration pin
        Type A: analog pins
    3/ The metal lid is internally grounded and attached to the DAP

FIGURE 2. Terminal connections - Continued.

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FIGURE 3. Block diagram.

FIGURE 4. Power up timing.

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FIGURE 5. Reset timing.

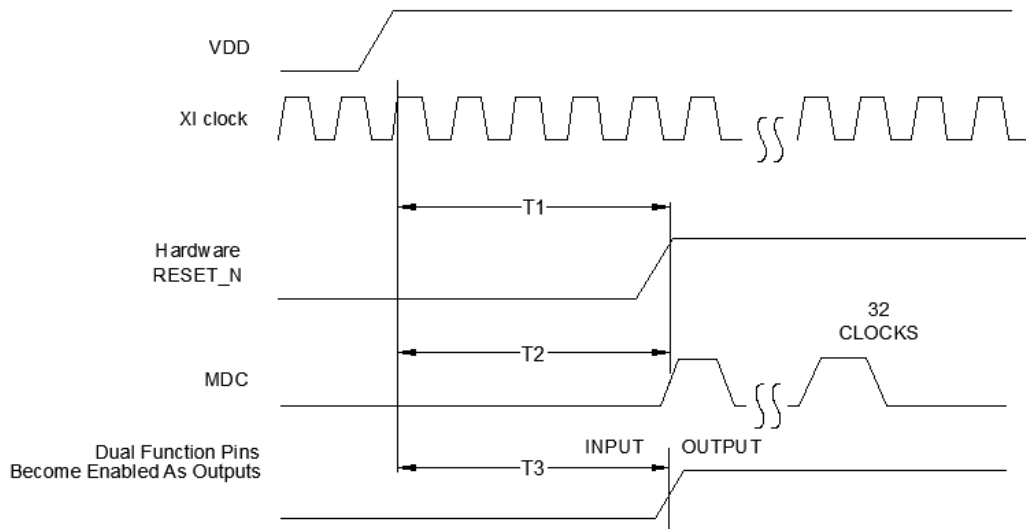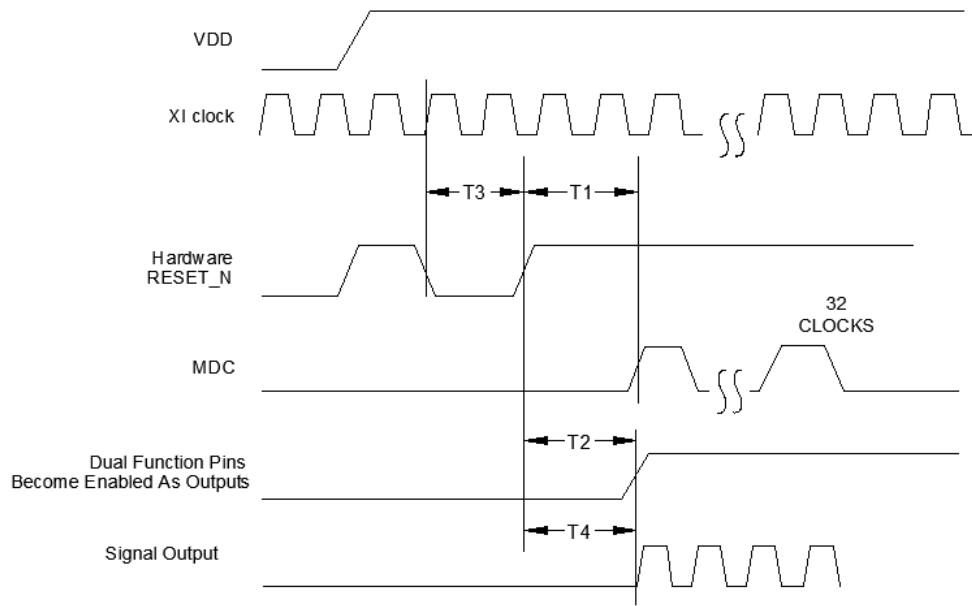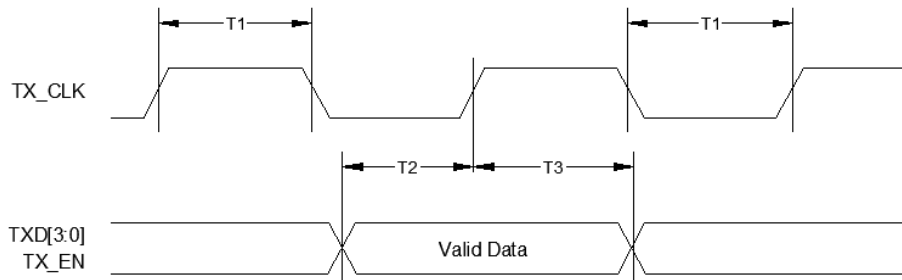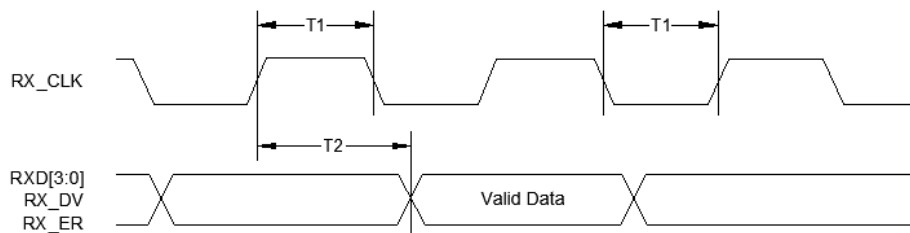FIGURE 6. 100-Mbps MII transmit timing.

FIGURE 7. 100-Mbps MII receive timing.

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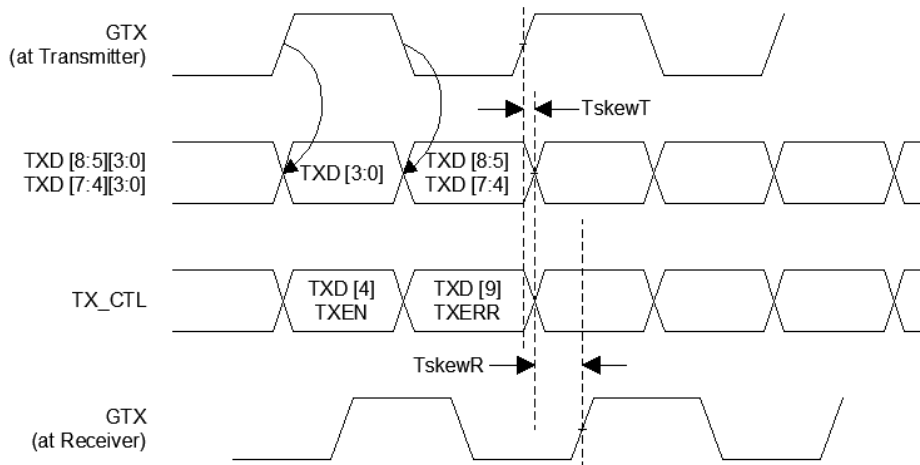
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FIGURE 8. RGMII transmit multiplexing and timing diagram.
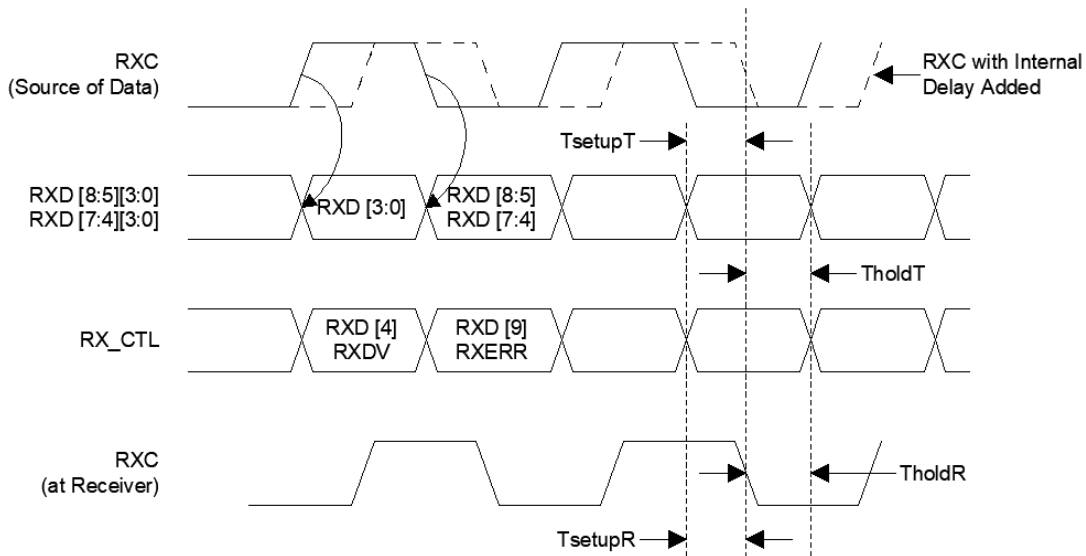
FIGURE 9. RGMII receive multiplexing and timing diagram.

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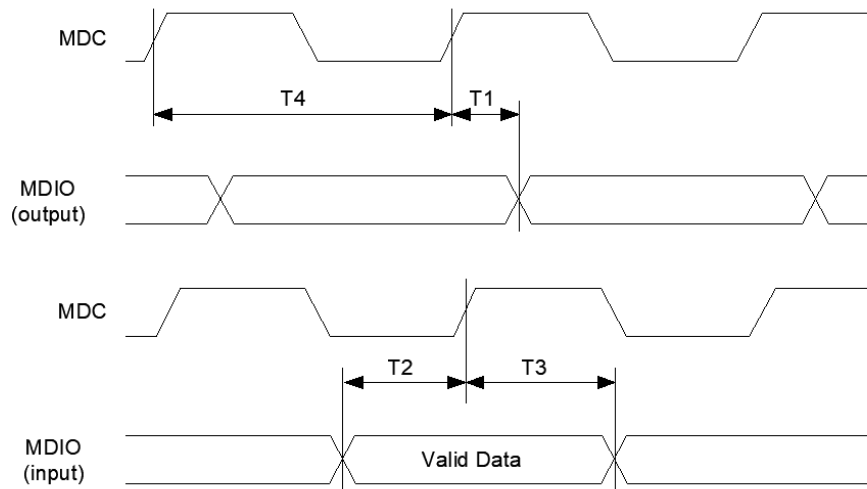
FIGURE 10. Serial management interface timing.

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4. VERIFICATION

4.1 <u>Sampling and inspection</u>. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 <u>Screening</u>. For device classes Q, and V screening test shall be performed in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 <u>Additional criteria for device classes Q and V</u>.

a. The burn-in test shall be performed in accordance with method 1015 of MIL-STD-883. Burn-in test duration, test condition and test temperature, or approved alternatives shall be specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535 and JEDEC JEP163. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. For static burn-in I, all inputs shall be connected to GND or low.

c. For static burn-in II, all inputs shall be connected to high through resistors to the supply voltage (V_{CC}).

d. Unless otherwise specified in the QM plan, for devices class V dynamic burn-in shall be performed with test condition D, method 1015 of MIL-STD-883.

e. For devices class V, interim and post burn-in final electrical test delta parameters shall be specified in delta burn-in table IIB herein.

4.3 <u>Qualification inspection for device classes Q and V</u>. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 <u>Conformance inspection</u>. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 <u>Group A inspection</u>.

a. Tests shall be as specified in table IIA herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

4.4.2 <u>Group B inspection.</u> When applicable, the group B inspection end-point electrical parameters subgroups shall be as specified in table IIA herein.

4.4.3 <u>Group C inspection</u>. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3.1 <u>Additional criteria for device classes Q and V</u>. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.4 <u>Group D inspection</u>. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, Group A (electrical test) table III)	
	Device class Q	Device class V
Interim (pre burn-in) electrical parameters, (see 4.2)	1, 7, 9 1/	1, 7, 9 1/ 2/
Static burn-in I and II, (see 4.2.1)	Required 3/	Required 4/
Dynamic burn-in, (see 4.2.1)	Required 3/	Required 5/
Post burn-in electrical parameters (see 4.2.1)	1, 7, 9 1/	1, 7, 9 1/ 2/
Group A (Final electrical) test requirements, (see 4.4.1) 6/	1, 2, 3, 4, 5, 6, 7, 8, 9 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9 10, 11
Group B end point electrical parameters, (see 4.4.2)	1, 2, 3, 4, 5, 6, 7, 8, 9 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9 10, 11
Group C end-point electrical parameters, (see 4.4.3)	1, 2, 3, 4, 5, 6, 7, 8, 9 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9 10, 11
Group D end-point electrical parameters, (see 4.4.4)	1, 2, 3, 4, 5, 6, 7, 8, 9 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9 10, 11
Group E (RHA) end-point electrical parameters, (see 4.4.5)	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1 (see 4.2). For device class V PDA applies to subgroups 1 and 7 (see 4.2.1).
2/ For device class V (class level S): 100 percent of the devices shall be tested. Pre and post burn-in test results shall be read and recorded for those parameters requiring delta calculations. Delta parameters shall be specified in table IIB.
3/ The burn-in configuration, either static or dynamic burn-in test shall be performed per TM 1015 with test condition A or B or C or D (see MIL-PRF-38535 and JEDEC JEP163)
4/ For device class V (class level S): If the device operates in a static mode, then static burn-in I and/or II test shall be performed per TM 1015 with test condition A or C (see MIL-PRF-38535 and JEDEC JEP163).
5/ For device class V (class level S): If the device operates in a dynamic mode, then dynamic burn-in test shall be performed per TM 1015 with test condition D (see MIL-PRF-38535 and JEDEC JEP163).
6/ For solder termination devices, ball grid array (BGA) and column grid array (CGA) packages end-point electrical parameters test shall be performed at the land grid array (LGA) level prior to ball or column attach. After column attach, electrical test shall be performed at 25°C (Group A, subgroup 1) as a minimum to verify that no electrical/mechanical damage has been introduced due to the column attach process.

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TABLE IIB. <u>Burn-in and operating life test delta parameters (+25°C).</u>

Parameter 1/	Symbol	Delta limits 2/
$I_{DD\_IEEEPWRDN}$	$I_{DDpwrdwn(3P3)}$	±0.060 mA
I_{DD_RESET}	$I_{DDreset(3P3)}$	±0.060 mA
High level output voltage (V_{DDIO} = 3.3V)	$V_{OH(3p3)}$	±0.615 V
Low level output voltage (V_{DDIO} = 3.3V)	$V_{OL(3p3)}$	±0.301 V
High level output voltage (V_{DDIO} = 2.5V)	$V_{OH(2p5)}$	±0.480 V
Low level output voltage (V_{DDIO} = 2.5V)	$V_{OL(2p5)}$	±0.301 V
High level output voltage (V_{DDIO} = 1.8V)	$V_{OH(1p8)}$	±0.239 V
Low level output voltage (V_{DDIO} = 1.8V)	$V_{OL(1p8)}$	±0.350 V

1/ The above parameter shall be recorded before and after the required burn-in and life tests to
     determine the delta (Δ) burn-in electrical limit.

2/   Unless otherwise specified, the characteristics, test methods, conditions and limits shall be
     corresponding to the test defined in Table IA (electrical performance characteristics). The drift
     values shall not be exceeded for each characteristic specified in Table IA.

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4.4.5 <u>Group E inspection</u>. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

    a. RHA levels for device classes Q, and V shall be as specified in MIL-PRF-38535 and the end-point electrical parameters subgroups shall be as specified in table IIA herein.

    b. For device classes Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet postirradiation end-point electrical parameter limits as defined in table IA at TA = +25°C±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.5.1 <u>Total dose irradiation testing</u>. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A, and as specified herein.

4.4.5.1.1 <u>Accelerated aging test</u>. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5 krad(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.5.2 <u>Neutron irradiation</u>. When specified in the purchase order or contract, Neutron irradiation test shall be conducted by using a neutron fluence of approximately 1 x 10^{12} neutrons/cm^2.

4.4.5.3 <u>Single event phenomena (SEP)</u>. When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latch-up characteristics. Test four devices with zero failures. ASTM F1192 or JESD57 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

    a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beams due to fixturing or package related affects is allowed.

    b. The fluence shall be $\geq$ 100 errors or $\geq 10^7$ ions/cm^2.

    c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

    d. The particle range shall be $\geq$ 20 microns in silicon.

    e. The test temperature shall be the maximum rated operating temperature 25°C ±10°C for the latch-up measurements.

    f. Bias conditions shall be defined by the manufacturer for the latch-up measurements.

    g. For SEP test limits, see table IB herein.

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5. PACKAGING

5.1 <u>Packaging requirements</u>. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 <u>Intended use</u>. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 <u>Replaceability</u>. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 <u>Configuration control of SMD's</u>. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 <u>Record of users</u>. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 <u>Comments</u>. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 <u>Abbreviations, symbols, and definitions</u>. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 <u>Sources of supply</u>.

6.6.1 <u>Sources of supply for device classes Q and V</u>. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 <u>Additional information</u>. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

    a.   RHA test conditions of SEP.

    b   Number of upsets (SEU).

    c.   Number of transients (SET).

    d.   Occurrence of latch-up (SEL).

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 22-05-20

Approved sources of supply for SMD 5962-20216 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962F2021601VXC	01295	DP83561-SP

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. PO Box 660199 Dallas, TX 75243