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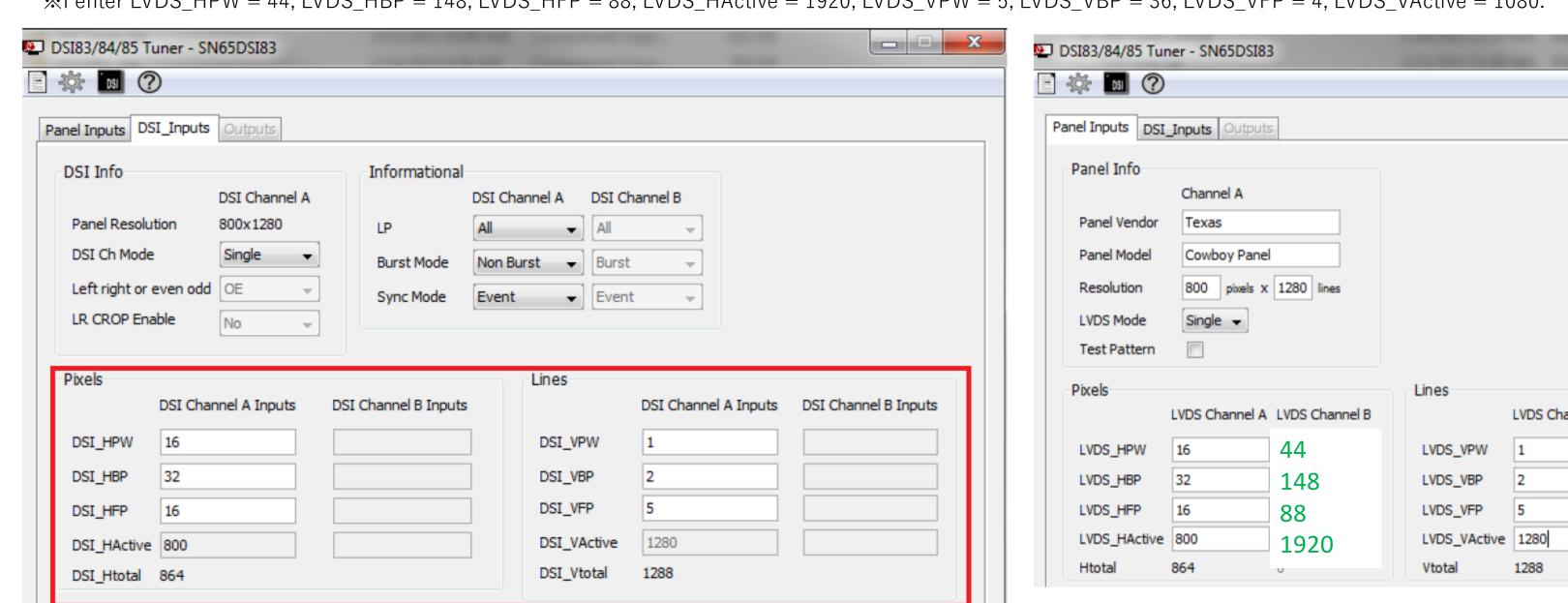
TEXAS INSTRUMENTS

LVDS Channel A

## 2. Question

## Q1 What should I enter for DSI\_HPW, DSI\_HBP, DSI\_HFP, DSI\_VPW, DSI\_VBP, DSI\_VFP?

፠I think the number of NOPs will change for each LINE. Therefore, I do not know how to set it. XI enter LVDS\_HPW = 44, LVDS\_HBP = 148, LVDS\_HFP = 88, LVDS\_HActive = 1920, LVDS\_VPW = 5, LVDS\_VBP = 36, LVDS\_VFP = 4, LVDS\_VActive = 1080.



Q2 What should I enter for CHA\_SYNC\_DELAY\_LOW and CHA\_SYNC\_DELAY\_HIGH? Should I enter 2200? CHA\_SYNC\_HIGH=0x8, CHA\_SYNC\_LOW=0x98

	0x28	7:0	CHA_SYNC_DELAY_LOW This field controls the delay in pixel clocks from when an HSync or VSync is received on the DSI to when it is transmitted on the LVDS interface for channel A. The delay specified by this field is in addition to the pipeline and synchronization delays in the SN65DSI83 device. The additional delay is approximately 10 pixel clocks. The sync delay must be programmed to at least 32 pixel clocks to ensure proper operation. The value in this field is the lower 8 bits of the 12-bit value for the sync delay.
	0x29	3:0	CHA_SYNC_DELAY_HIGH This field controls the delay in pixel clocks from when an HSync or VSync is received on the DSI to when it is transmitted on the LVDS interface for channel A. The delay specified by this field is in addition to the pipeline and synchronization delays in the SN65DSI83 device. The additional delay is approximately 10 pixel clocks. The sync delay must be programmed to at least 32 pixel clocks to ensure proper operation. The value in this field is the lower 4 bits of the 12-bit value for the sync delay.