KEYSIGHT TECHNOLOGIES

Test Report

FAIL

Test Configuration Details	
Application	
Name	D9021HDMC HDMI Test
Version	2.40.3007.0
Device Description	
HDMITestType	TMDS Physical Layer
DeviceID	Transmitter
Device Name	Device1
Comments	User comments
FixtureType	Wilder HDMI2 TPA-P 12 inch
Probe Head Type	N5380X/1169X*
Probe Connection Choice	4 Probes
Lane Connection	3 Data Lanes
Test Session Details	
Infiniium SW Version	06.74.01816
Infiniium Model Number	DSO91304A
Infiniium Serial Number	MY53240113
Debug Mode Used	No
Compliance Limits	Standard
Probe (Channel 1)	Model: 1169A Serial: US49411824 Head: N5380A/B Atten: Calibrated (16 MAY 2025 11:08:12), Using Cal Atten (2.0449E+00) Skew: Calibrated (16 MAY 2025 11:12:33), Using Cal Skew
Probe (Channel 2)	Model: 1169B Serial: US55394596 Head: N5380A/B Atten: Calibrated (16 MAY 2025 11:26:49), Using Cal Atten (2.0489E+00) Skew: Calibrated (16 MAY 2025 11:27:06), Using Cal Skew
Probe (Channel 3)	Model: 1169B Serial: US55394679 Head: N5380A/B Atten: Calibrated (16 MAY 2025 11:38:55), Using Cal Atten (2.0100E+00) Skew: Calibrated (16 MAY 2025 11:39:06), Using Cal Skew
Probe (Channel 4)	Model: 1169B Serial: US55394827 Head: N5380A/B Atten: Calibrated (16 MAY 2025 11:45:43), Using Cal Atten (2.0199E+00) Skew: Calibrated (16 MAY 2025 11:53:06), Using Cal Skew
Last Test Date	2025-06-09 16:22:20 UTC +09:00

Summary of Results

Test Statistics	
Failed	6
Passed	2
Incomplete	0
Total	8

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	7-4: Clock Rise Time	189.971 ps	153.295 %	VALUE >= 75.000 ps
✓	0	1	7-4: Clock Fall Time	182.862 ps	143.816 %	VALUE >= 75.000 ps
✗	1	1	7-4: D0 Rise Time	69.771 ps	**-6.97160 %**	VALUE >= 75.000 ps
✗	1	1	7-4: D0 Fall Time	67.350 ps	**-10.2005 %**	VALUE >= 75.000 ps
✗	1	1	7-4: D1 Rise Time	65.920 ps	**-12.1069 %**	VALUE >= 75.000 ps
✗	1	1	7-4: D1 Fall Time	66.300 ps	**-11.5995 %**	VALUE >= 75.000 ps
✗	1	1	7-4: D2 Rise Time	70.731 ps	**-5.69227 %**	VALUE >= 75.000 ps
✗	1	1	7-4: D2 Fall Time	70.318 ps	**-6.24267 %**	VALUE >= 75.000 ps

Report Detail

Next

✓7-4: Clock Rise Time

Reference: Test ID 7-4

Test Summary: Pass Test Description: 2 Channels Connection Model: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

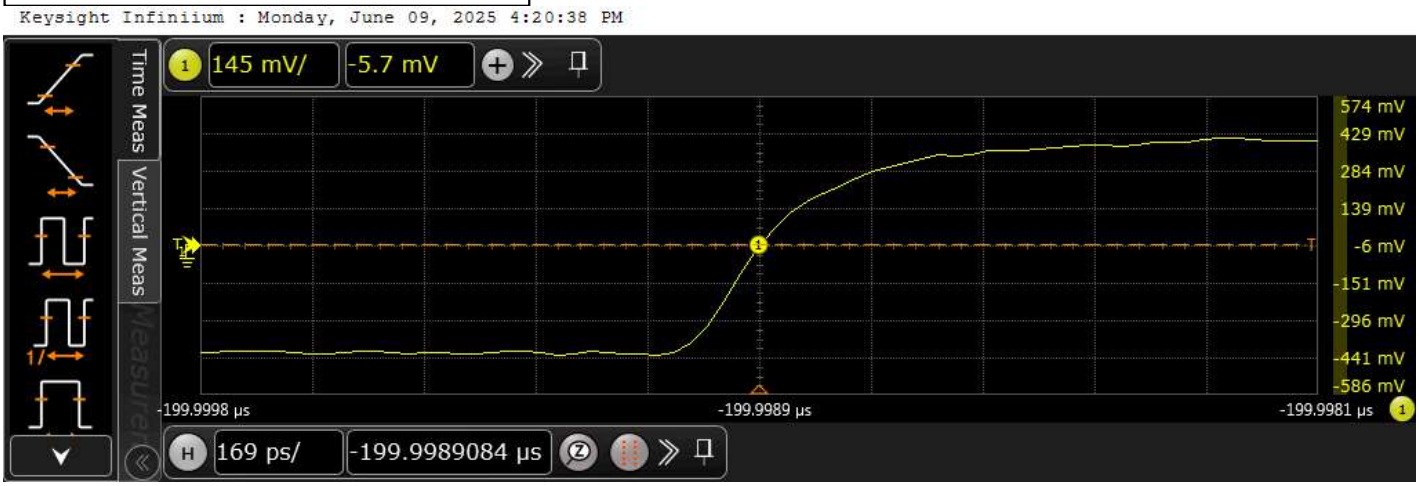
Pass Limits: >= 75.000 ps | **7-4 Clock Rise Time** 189.971 ps

Result Details

HDMIAutomationConfig Timing 100 | **Test Frequency(MHz)** 296.692 MHz | **Upper Threshold(%)** 80.000 | **Lower Threshold(%)** 20.000 | **VTop(V)** 405 m | **VBase(V)** -417 m | **Upper Threshold(V)** 241 m | **Lower Threshold(V)** -252 m | **# Edges** 118.677 k

Trial 1

Trial 1: 7-4 Clock Rise Time



Next

✓7-4: Clock Fall Time

Reference: Test ID 7-4

Test Summary: Pass Test Description: 2 Channels Connection Model: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

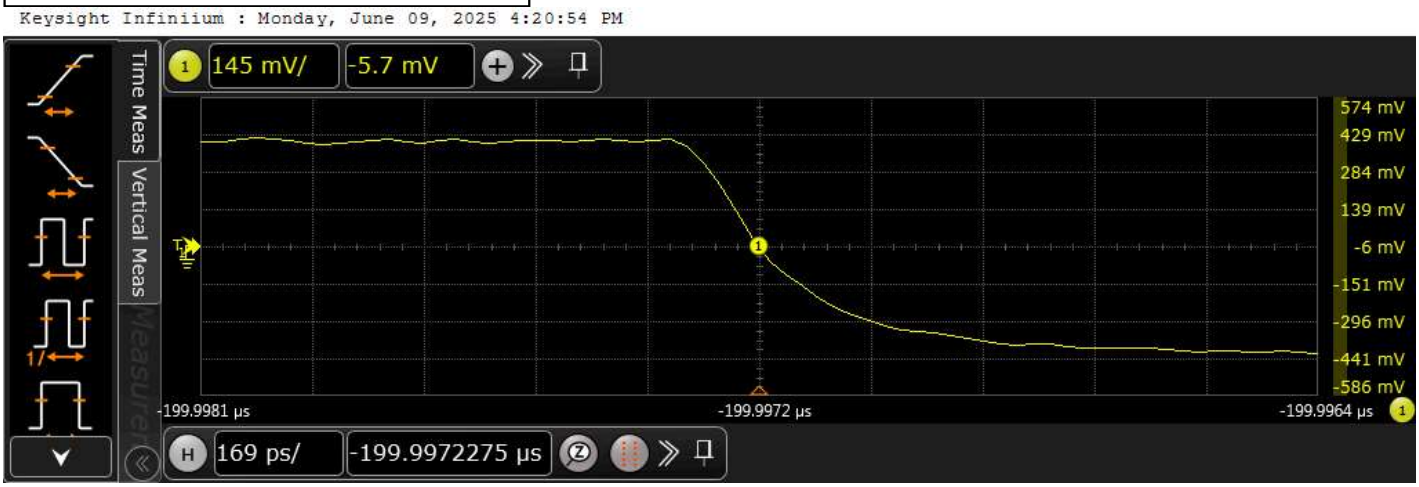
Pass Limits: >= 75.000 ps | **7-4 Clock Fall Time** 182.862 ps

Result Details

HDMIAutomationConfig	Timing 100	**Test Frequency(MHz)**	296.692 MHz	**Upper Threshold(%)**	80.000				
Lower Threshold(%)	20.000	**VTop(V)**	405 m	**VBase(V)**	-417 m	**Upper Threshold(V)**	241 m	**Lower Threshold(V)**	-252 m
# Edges	118.676 k								

Trial 1

Trial 1: 7-4 Clock Fall Time



Next

✗7-4: D0 Rise Time

Reference: Test ID 7-4

Test Summary: FAIL Test Description: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

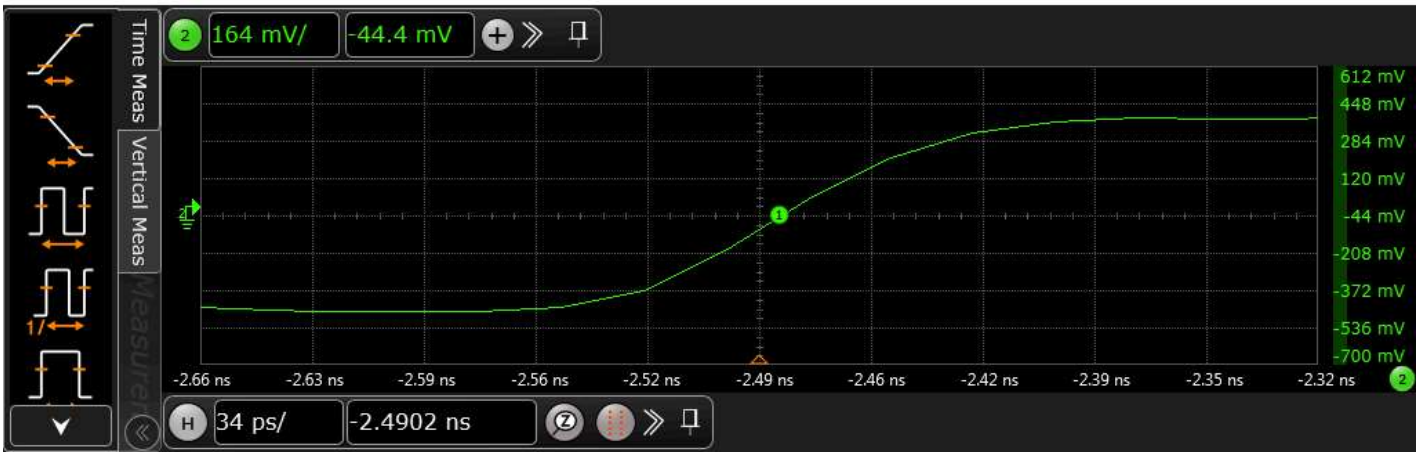
Pass Limits:	>= 75.000 ps	**7-4 D0 Rise Time**	69.771 ps

Result Details

HDMIAutomationConfig	Timing 100	**Test Frequency(MHz)**	296.692 MHz	**Data Lane A**	D0	**Edge Type**	All edges		
Upper Threshold(%)	80.000	**Lower Threshold(%)**	20.000	**VTop(V)**	423 m	**VBase(V)**	-518 m	**Upper Threshold(V)**	235 m
Lower Threshold(V)	-329 m	**#Edge**	275.489 k						

Trial 1

Trial 1: 7-4 D0 Rise Time



Next

✗7-4: D0 Fall Time

Reference: Test ID 7-4

Test Summary: FAIL Test Description: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Pass Limits:	>= 75.000 ps	**7-4 D0 Fall Time**	67.350 ps

Result Details

HDMIAutomationConfig	Timing 100	**Test Frequency(MHz)**	296.692 MHz	**Data Lane A**	D0	**Edge Type**	All edges		
Upper Threshold(%)	80.000	**Lower Threshold(%)**	20.000	**VTop(V)**	423 m	**VBase(V)**	-518 m	**Upper Threshold(V)**	235 m
Lower Threshold(V)	-329 m	**#Edge**	278.113 k						

Trial 1

Trial 1: 7-4 D0 Fall Time

Keysight Infiniium : Monday, June 09, 2025 4:21:22 PM

Next

✗7-4: D1 Rise Time

Reference: Test ID 7-4

Test Summary: FAIL Test Description: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Pass Limits: >= 75.000 ps	**7-4 D1 Rise Time** 65.920 ps

Result Details

HDMIAutomationConfig Timing 100	**Test Frequency(MHz)** 296.692 MHz	**Data Lane A** D1	**Edge Type** All edges

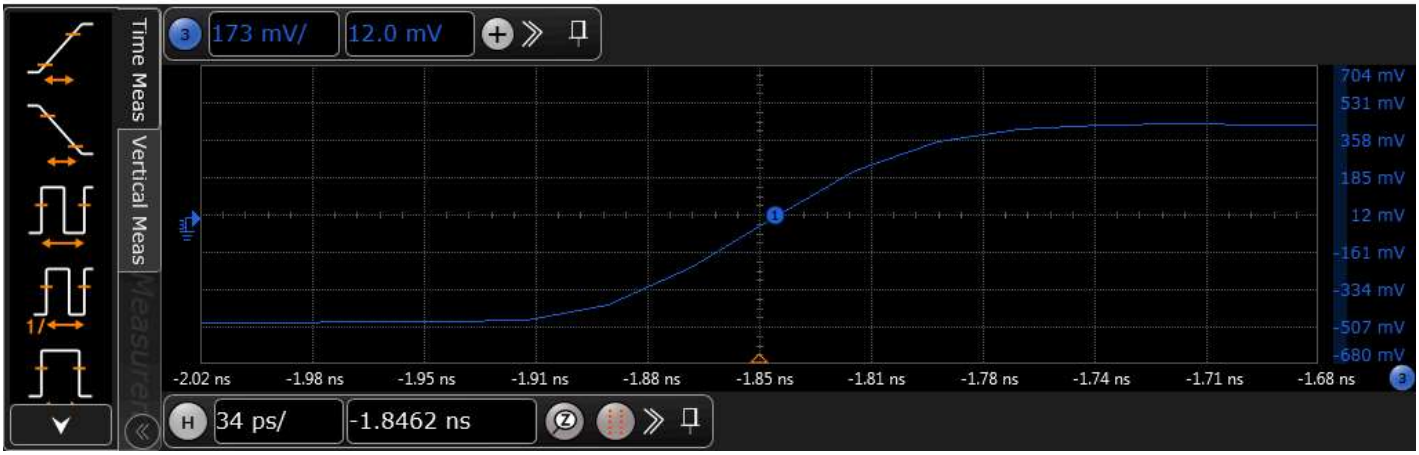
Upper Threshold(%) 80.000	**Lower Threshold(%)** 20.000	**VTop(V)** 493 m	**VBase(V)** -478 m	**Upper Threshold(V)** 299 m

Lower Threshold(V) -284 m	**#Edge** 280.141 k

Trial 1

Trial 1: 7-4 D1 Rise Time

Keysight Infiniium : Monday, June 09, 2025 4:21:39 PM



Next

✗7-4: D1 Fall Time

Reference: Test ID 7-4

Test Summary: FAIL Test Description: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Pass Limits: >= 75.000 ps	**7-4 D1 Fall Time** 66.300 ps

Result Details

HDMIAutomationConfig Timing 100	**Test Frequency(MHz)** 296.692 MHz	**Data Lane A** D1	**Edge Type** All edges

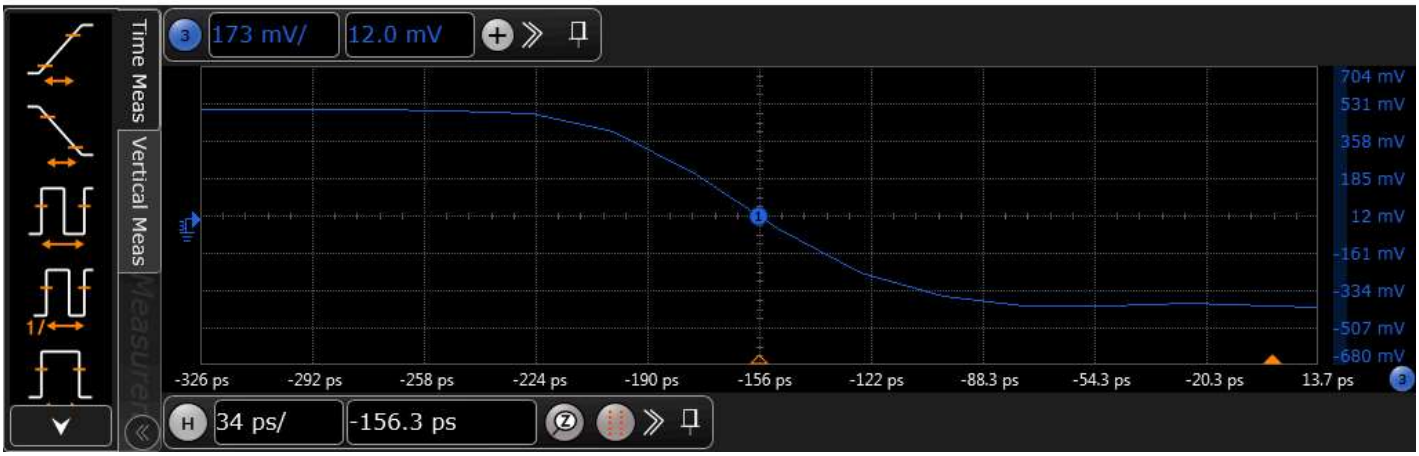
Upper Threshold(%) 80.000	**Lower Threshold(%)** 20.000	**VTop(V)** 493 m	**VBase(V)** -478 m	**Upper Threshold(V)** 299 m

Lower Threshold(V) -284 m	**#Edge** 279.268 k

Trial 1

Trial 1: 7-4 D1 Fall Time

Keysight Infiniium : Monday, June 09, 2025 4:21:51 PM



Next

✗7-4: D2 Rise Time

Reference: Test ID 7-4

Test Summary: FAIL Test Description: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Pass Limits: >= 75.000 ps	**7-4 D2 Rise Time** 70.731 ps

Result Details

HDMIAutomationConfig Timing 100	**Test Frequency(MHz)** 296.692 MHz	**Data Lane A** D2	**Edge Type** All edges

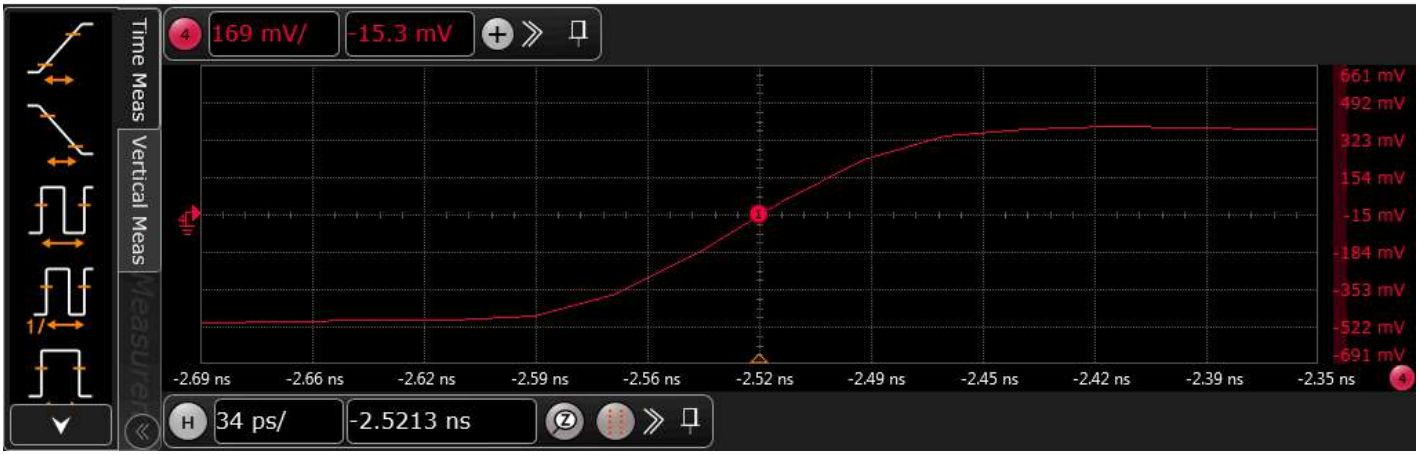
Upper Threshold(%) 80.000	**Lower Threshold(%)** 20.000	**VTop(V)** 460 m	**VBase(V)** -494 m	**Upper Threshold(V)** 269 m

Lower Threshold(V) -303 m	**#Edge** 282.738 k

Trial 1

Trial 1: 7-4 D2 Rise Time

Keysight Infiniium : Monday, June 09, 2025 4:22:08 PM



Next

✗7-4: D2 Fall Time

Reference: Test ID 7-4

Test Summary: FAIL Test Description: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Pass Limits: >= 75.000 ps	**7-4 D2 Fall Time** 70.318 ps

Result Details

HDMIAutomationConfig Timing 100	**Test Frequency(MHz)** 296.692 MHz	**Data Lane A** D2	**Edge Type** All edges

Upper Threshold(%) 80.000	**Lower Threshold(%)** 20.000	**VTop(V)** 460 m	**VBase(V)** -494 m	**Upper Threshold(V)** 269 m

Lower Threshold(V) -303 m	**#Edge** 275.064 k

Trial 1

Trial 1: 7-4 D2 Fall Time

Keysight Infiniium : Monday, June 09, 2025 4:22:20 PM