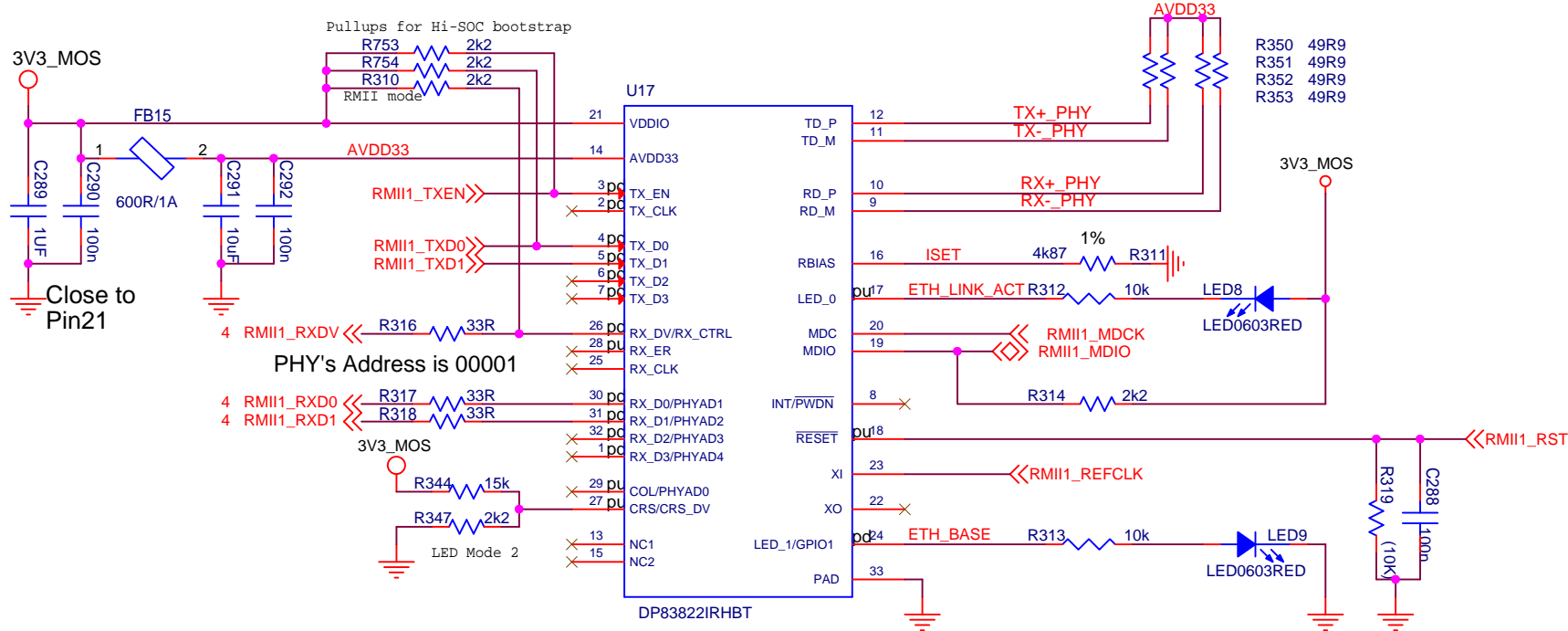


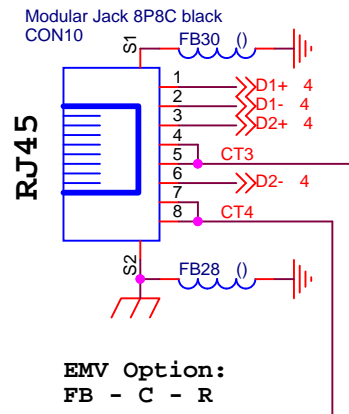
24 - Ethernet PHY



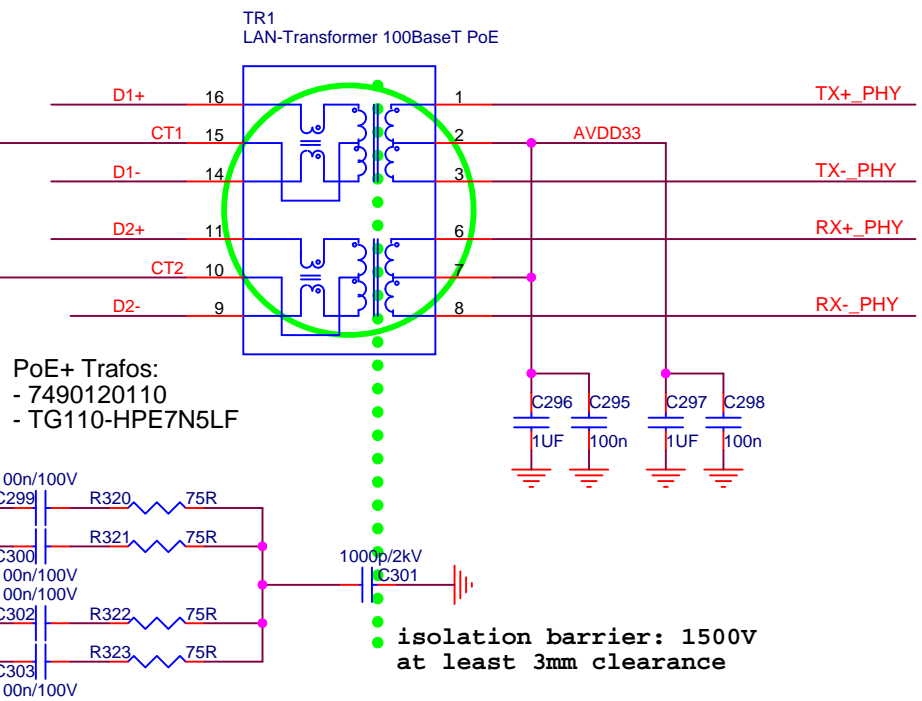
PHY's Address is 00001

**** Design guideline ****
A. RMII interface
 1. The REFCLK trace should be separated from other traces by GND

B. TX+_PHY/TX-_PHY & RX+_PHY/RX-_PHY differential pairs
 1. Route as 100 Ohm differential impedance on TOP layer
 2. Match trace length of differential pairs, 10 mils max within a pair.

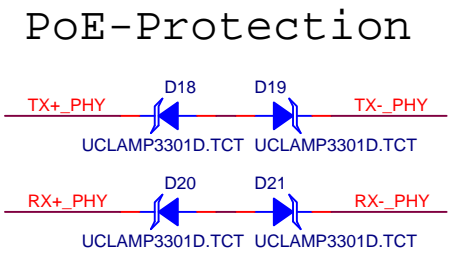


EMV Option:
 FB - C - R



PoE+ Trafos:
 - 7490120110
 - TG110-HPE7N5LF

isolation barrier: 1500V
 at least 3mm clearance



PoE-Protection