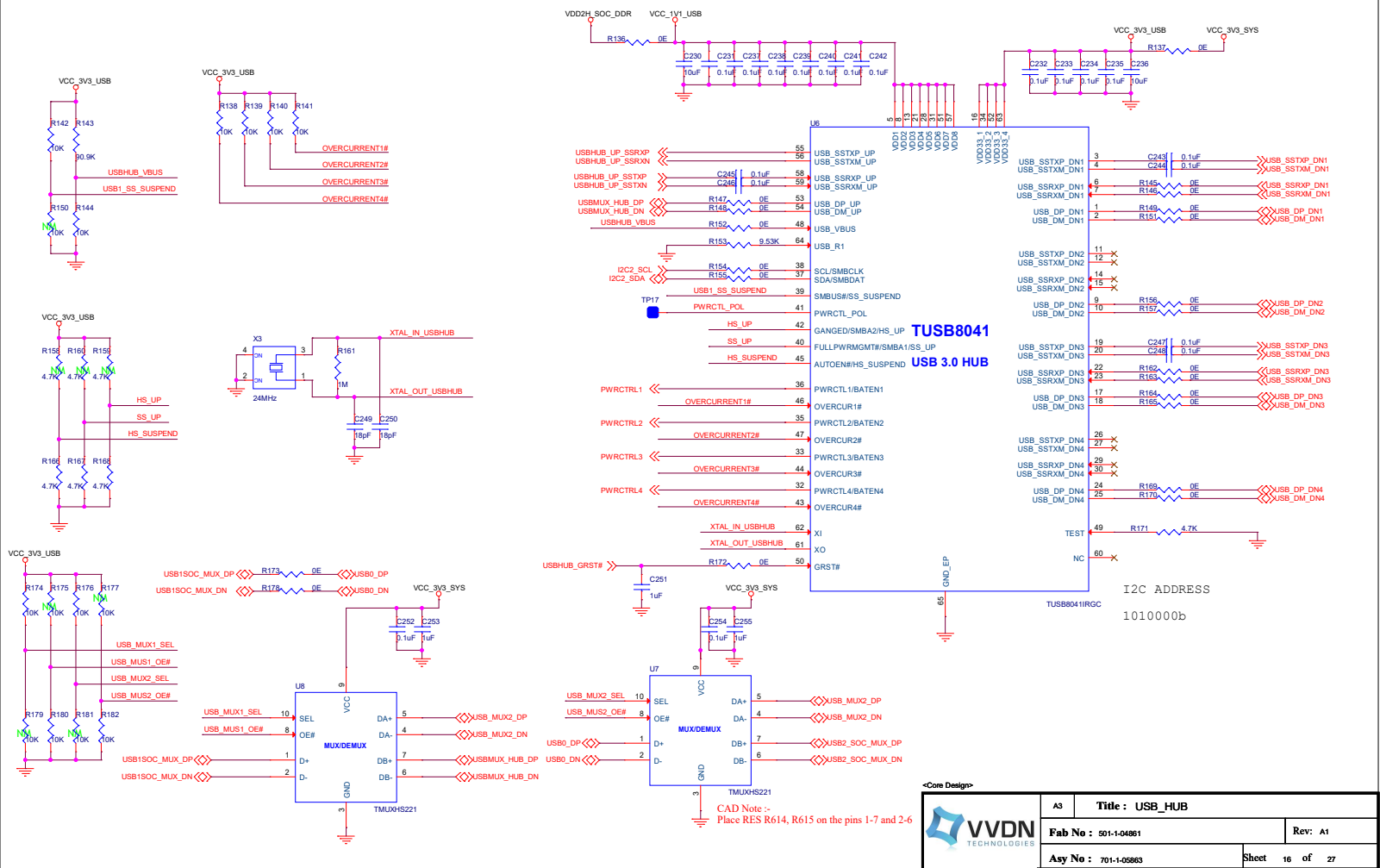
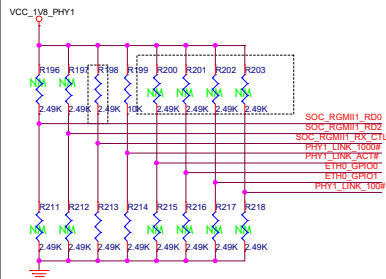
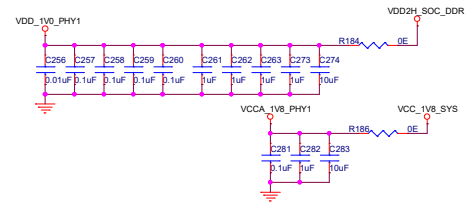
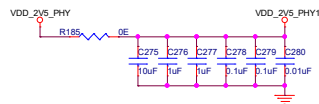
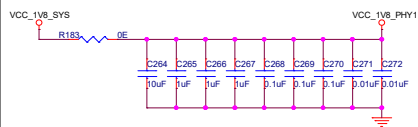


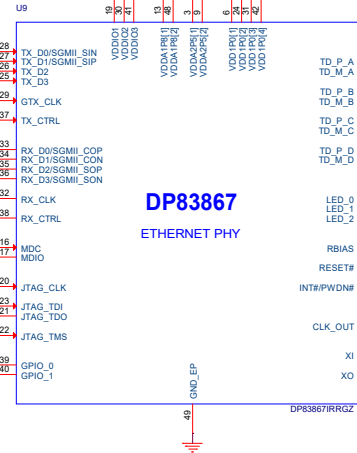
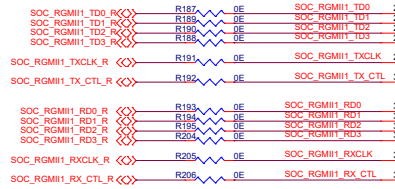
USB HUB



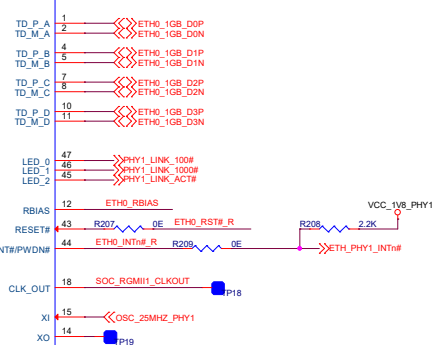
ETHERNET PHY1



CAD Note :-
TX termination resistor need to be placed on SOC side
RX termination resistor need to be placed on PHY side



DP83867
ETHERNET PHY



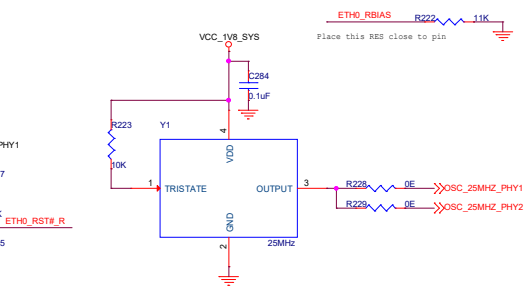
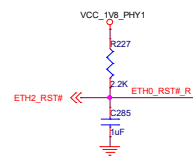
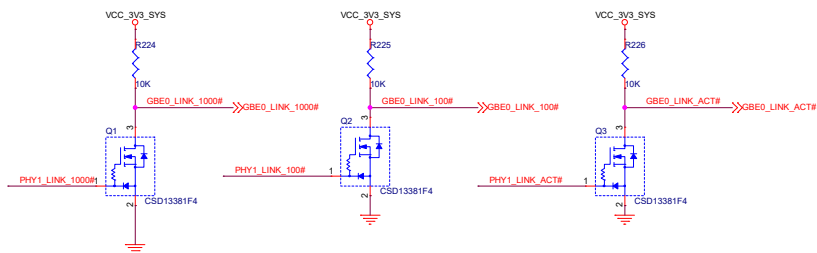
PHY ADDRESS = 0000

Auto-negotiation Enabled

10/100/1000 advertised, Auto-MDI-X

Tx Clock Skew = 0ns

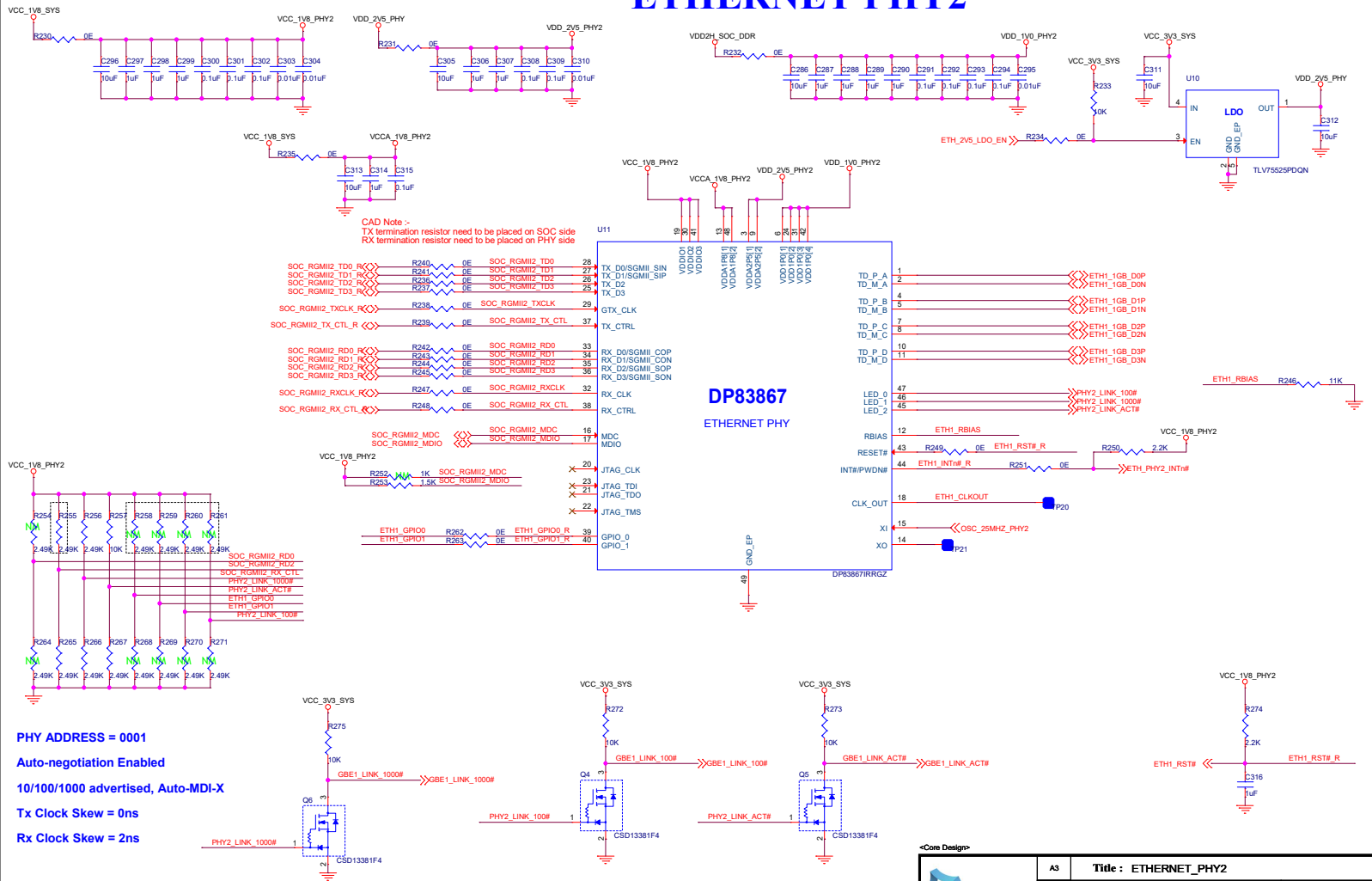
Rx Clock Skew = 2ns



<Core Design>

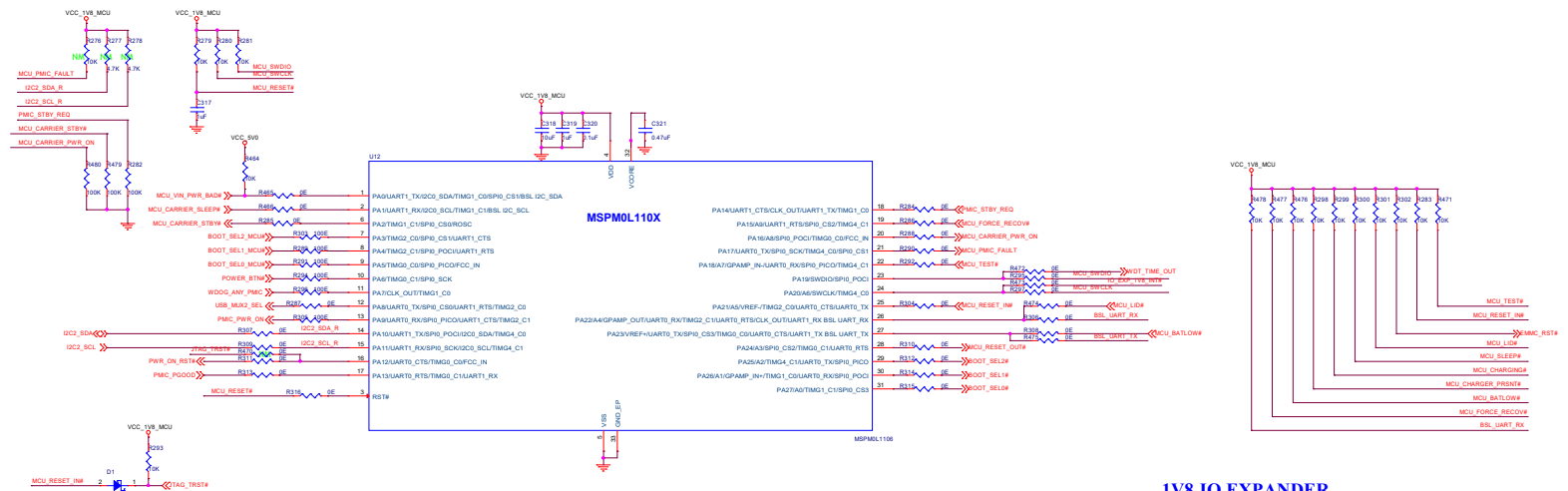
	A3	Title : ETHERNET_PHY1	
	Fab No : 501-1-04861		Rev: A1
	Asy No : 701-1-05863		Sheet 17 of 27

ETHERNET PHY2

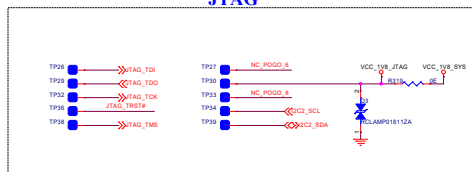


 VVDN TECHNOLOGIES		A3	Title : ETHERNET_PHY2	
		Fab No : 501-1-04861		Rev: A1
		Assy No : 701-1-05863		Sheet 18 of 27

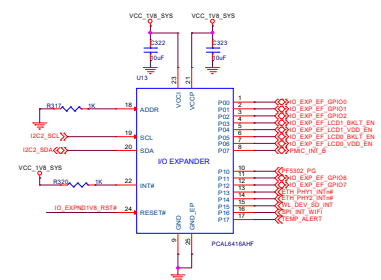
MCU POWER MANAGEMENT



JTAG

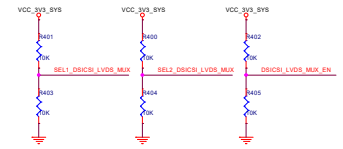
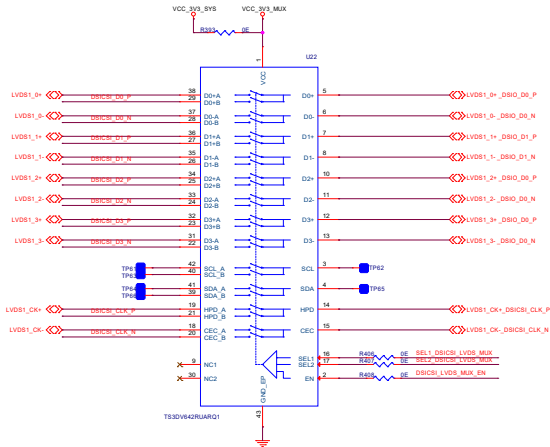
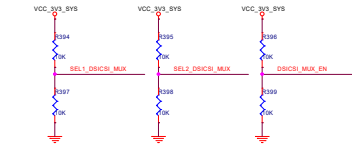
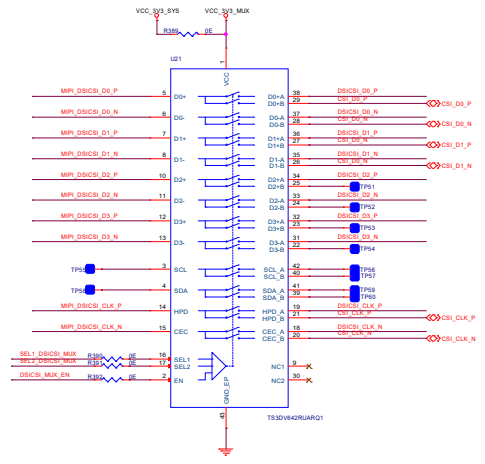
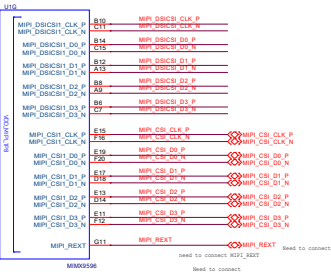


1V8-IO EXPANDER



 VVDN TECHNOLOGIES		A2	Title: MCU_PWR_MANAGEMENT
		Part No: 501-04081	Rev: A1
		Any No: 701-05083	Sheet 19 of 27

MIPI_LVDS_MUX



	A2	Title : <Sheet Name>	Rev: <Rev>
	Part No : 501-X-XXXXX		Any No : 701-X-XXXXX
	Sheet 34 of 37		