MDIO interface Access Issue Debug

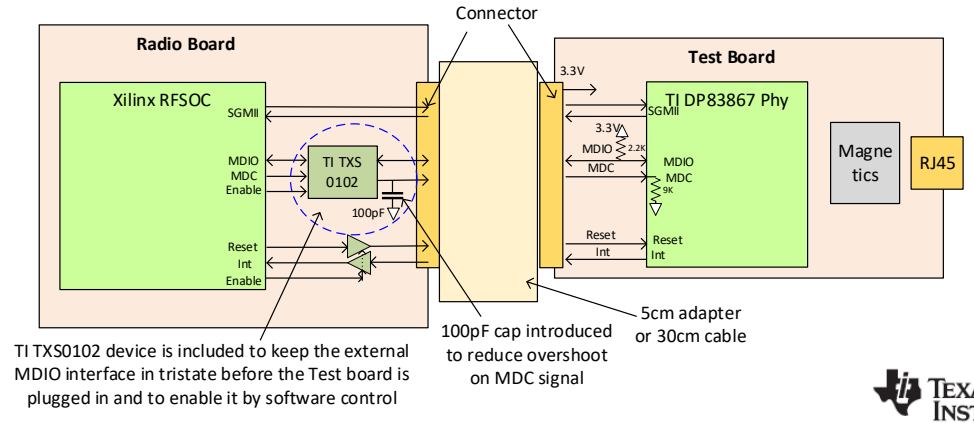
Capture of waveforms at Phy end

Version 0.3

02 Dec 2022

Overview – 1GE LMP port implementation

The 1GE Local Management port is implemented as shown to the right



The MDIO read access waveform from TI DP83867 Phy datasheet is shown to the right.

Note that there are two clock cycles for turn around time before the Phy starts driving the Read Register daa on the MDIO line

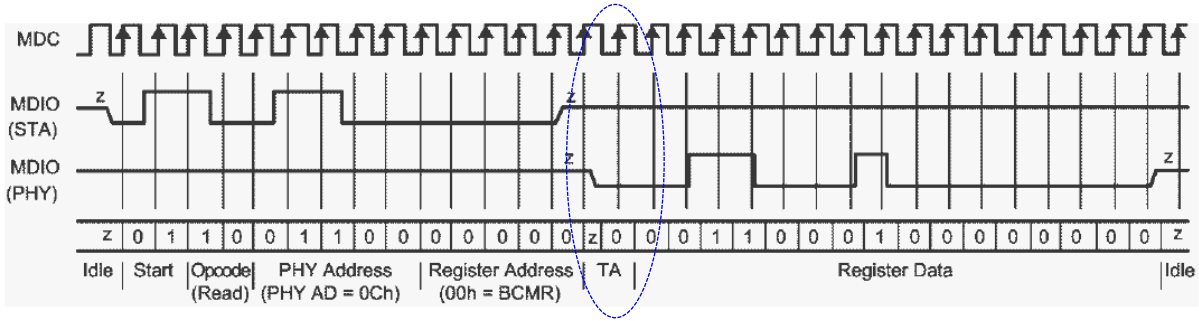
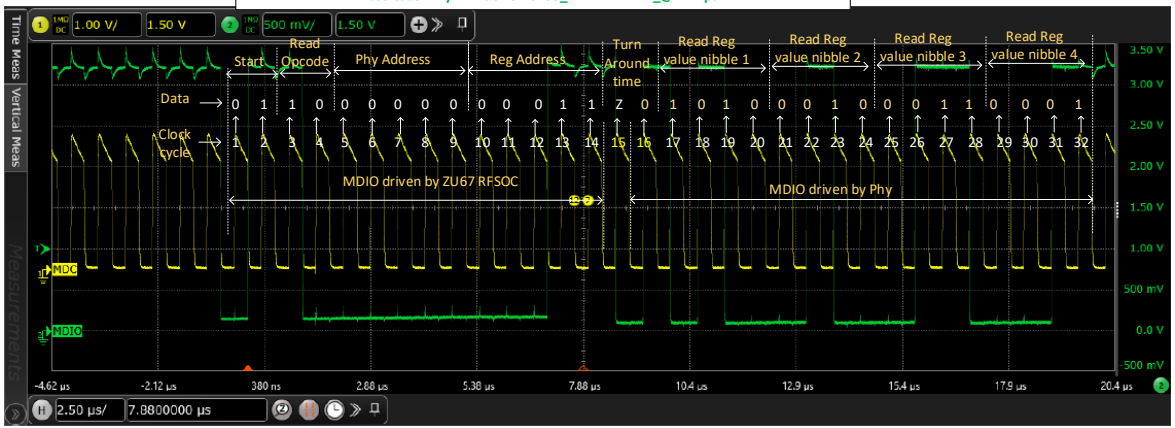


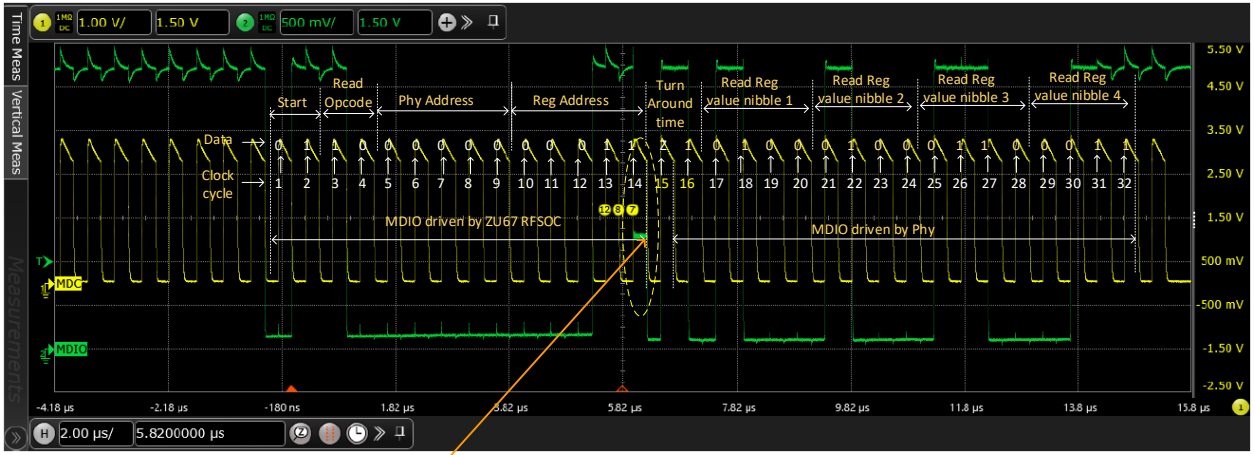
Figure 17. Typical MDC/MDIO Read Operation

MDIO access PHYID2 read waveform for Passing vs Failing case captured at Phy end

Pass Case: Phy ID2: 30Nov: JP95_PHYID2 READ_@HTB.pdf



Fail Case: Phy ID2: 30Nov: JP95_PHYID2 READ_FAIL2@HTB.pdf



<u>MDIO read access to PHYID2 register</u>
Register address: 0x3
Register data: 0xA231

In fail case value read is 0x4463
(bits shifted to left by 1)

Observation: Between the 14th Clock cycle rising edge and 15th Clock cycle rising edge, ZU67 and Phy device are expected to tristate the bus. However in the Fail case, it appears the Phy device is driving 0 (seems to have started driving the read response 1 clock cycle early)

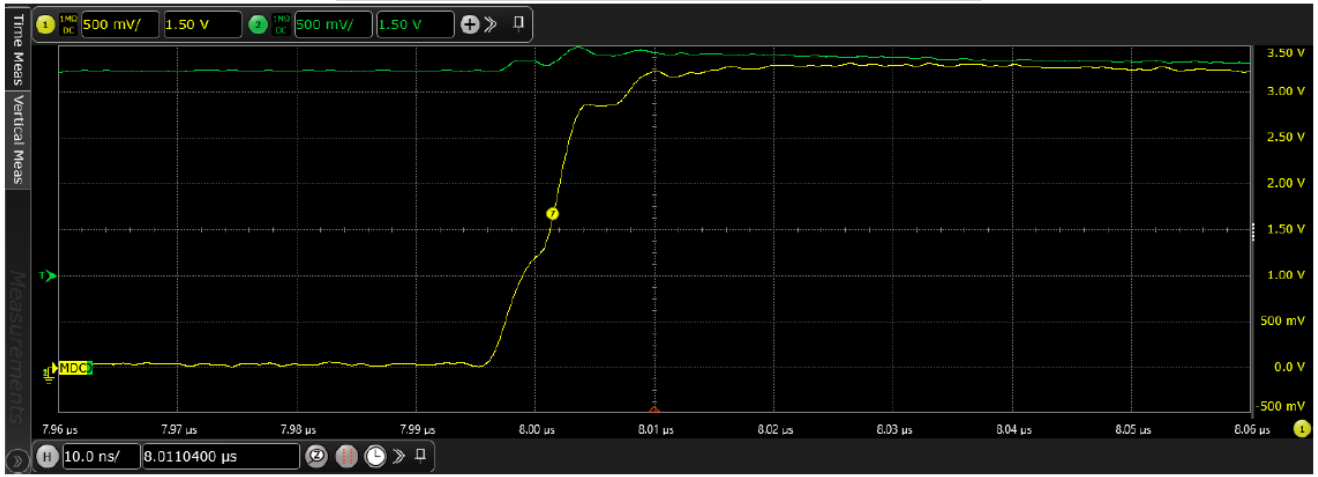
MDIO access PHYID2 read waveform for Passing case captured at Phy end

MDIO read access to PHYID2 register
Register address: 0x3
Register data: 0xA231

In Passing case at 14th Clock cycle rising edge MDIO is high.
After 15th Clock cycle rising edge MDIO is driven Low by PHY

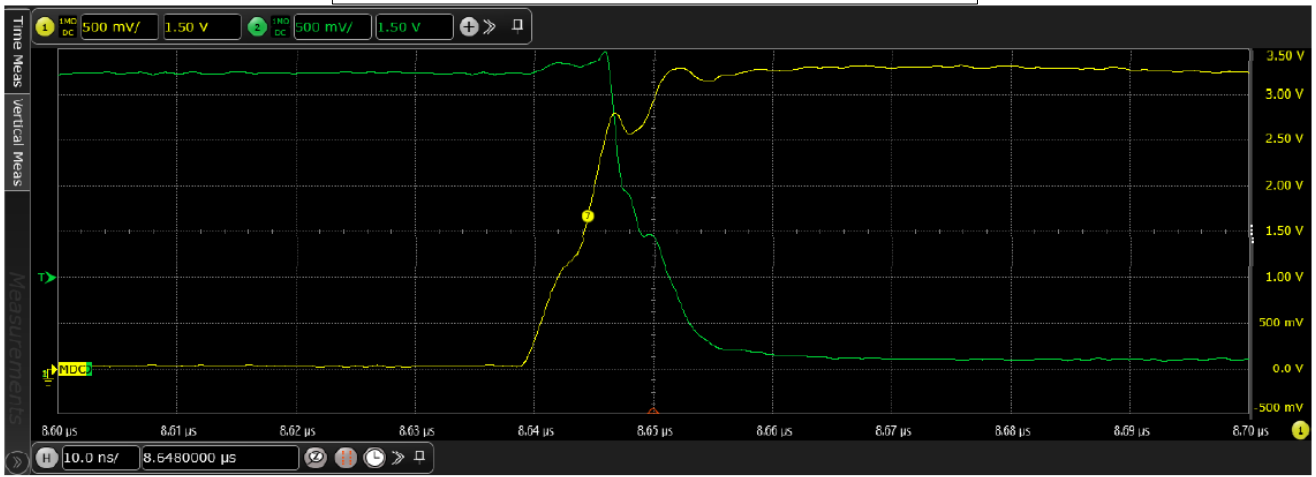
Zoom in on MDC rising edge 14

Pass Case: Phy ID2: 30Nov: JP95_PHYID2 READ_CLK14a_@HTB.pdf

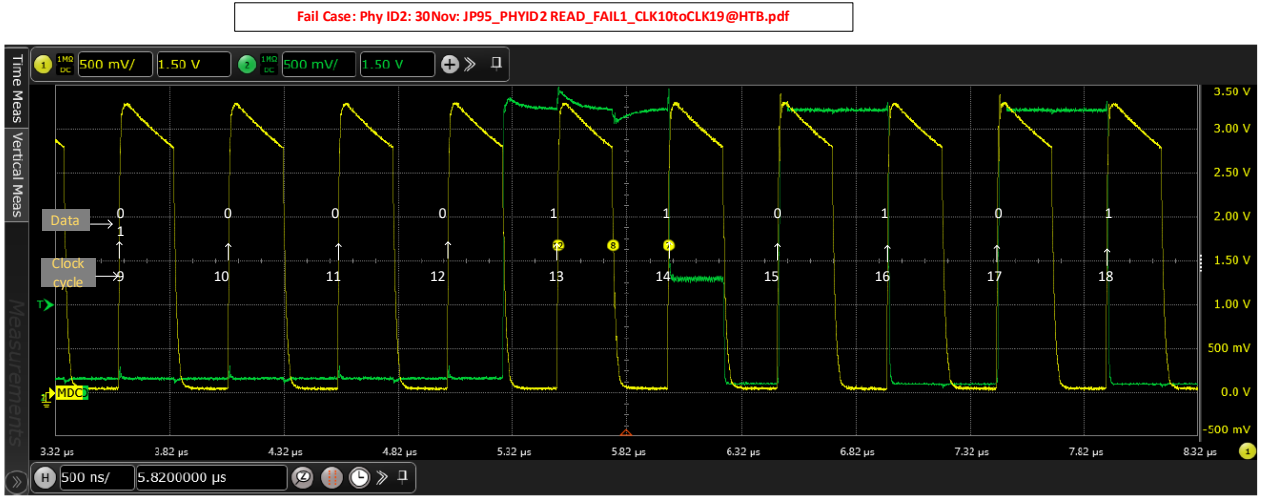


Zoom in on MDC rising edge 15

Pass Case: Phy ID2: 30Nov: JP95_PHYID2 READ_CLK15a_@HTB.pdf



MDIO access PHYID2 read waveform for Failing case captured at Phy end



<u>MDIO read access to PHYID2 register</u>
Register address: 0x3
Register data: 0xA231

In fail case value read is 0x4463
(bits shifted to left by 1)
In Failing case immediately after 14th MDC Clock cycle rising edge and next falling edge MDIO is at 1.5V indicating contention on the MDIO signal.
It appears Phy is unexpectedly driving 0 on MDIO at 14th MDC clock cycle falling edge which is in contention with the 1 being driven by ZU67.
After 15th Clock cycle rising edge MDIO is driven High by PHY

MDIO access PHYID2 read waveform for Failing case captured at Phy end

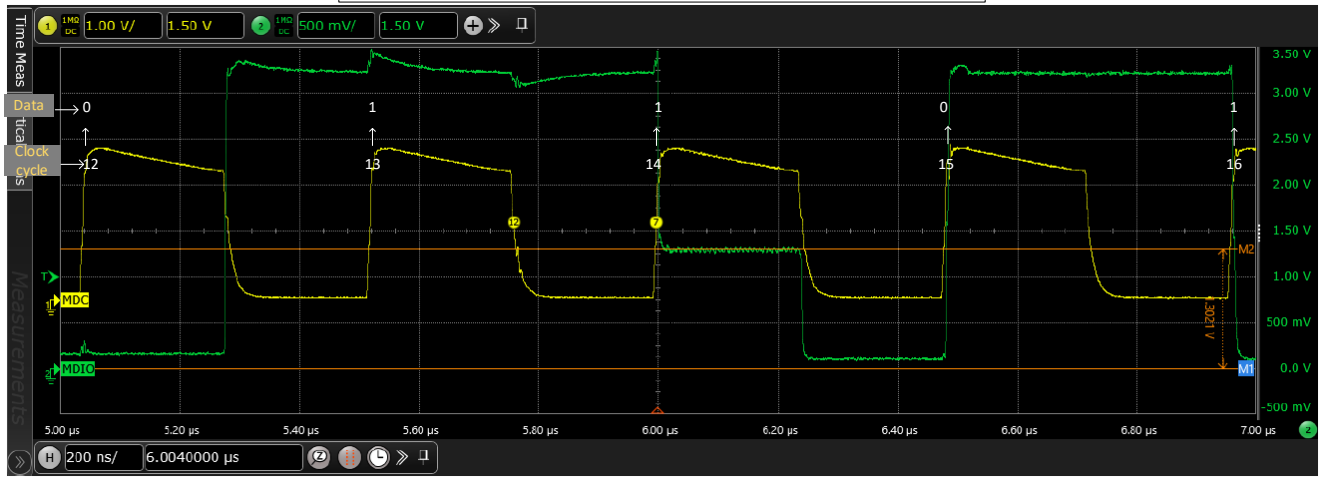
MDIO read access to PHYID2 register

In Failing case immediately after 14th MDC Clock cycle rising edge and next falling edge MDIO is at 1.5V indicating contention on the MDIO signal.

It appears Phy is unexpectedly driving 0 on MDIO at 14th MDC clock cycle falling edge which is in contention with the 1 being driven by ZU67

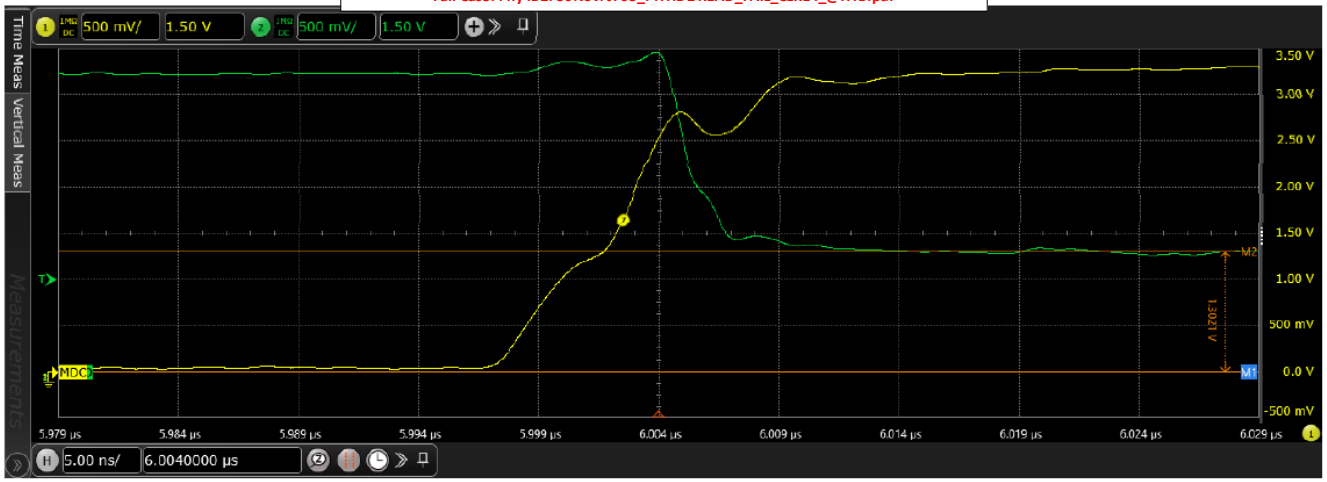
Zoom in on MDC rising edges 12 to 16

Fail Case: Phy ID2: 30Nov: JP95_PHYID2 READ_FAIL_CLK14 & 15_@HTB.pdf



Zoom in on MDC rising edge 14

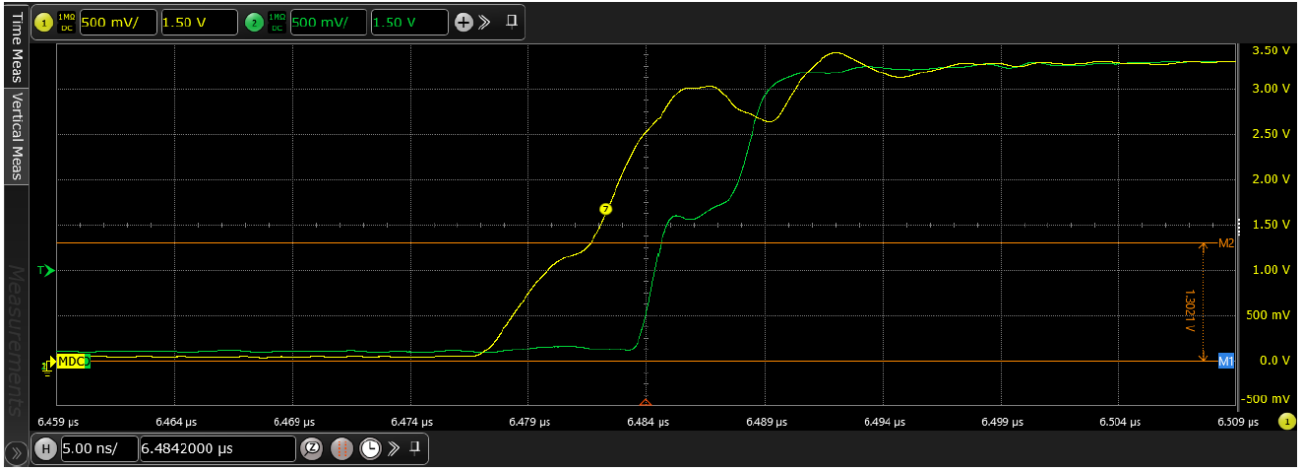
Fail Case: Phy ID2: 30Nov: JP95_PHYID2 READ_FAIL_CLK14_@HTB.pdf



MDIO access PHYID2 read waveform for Failing case captured at Phy end

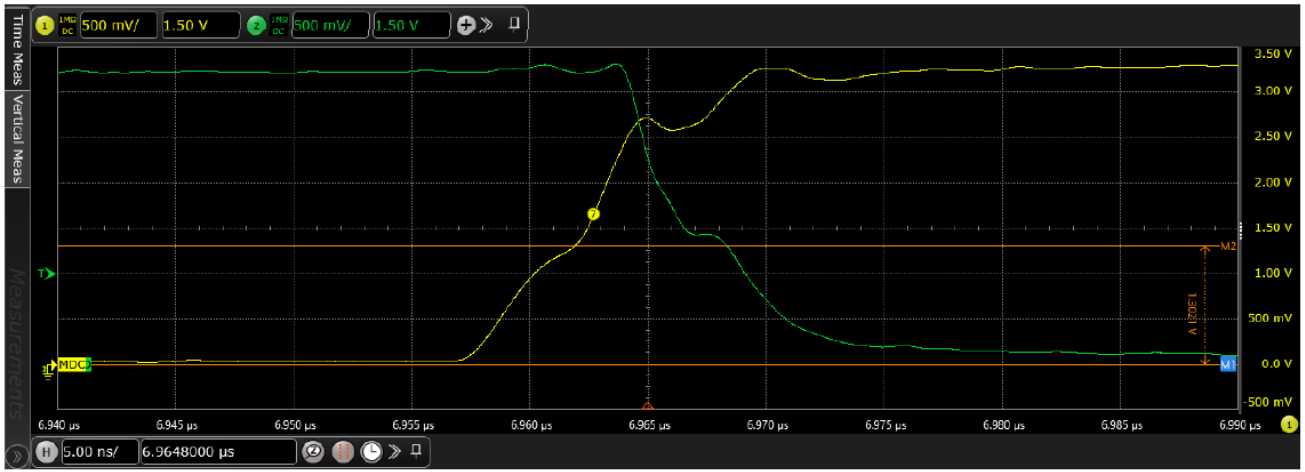
Zoom in on MDC rising edge 15

Fail Case: Phy ID2: 30Nov: JP95_PHYID2 READ_FAIL_CLK15a_@HTB.pdf



Zoom in on MDC rising edge 16

Fail Case: Phy ID2: 30Nov: JP95_PHYID2 READ_FAIL_CLK16_@HTB.pdf



MDIO read access to PHYID2 register
Register address: 0x3
Register data: 0xA231

In fail case value read is 0x4463
(bits shifted to left by 1)

MDIO access waveform analysis

The Previous slides capture the MDIO read waveform for Pass and Failing case for (PHYID2 (Phy register address :0x03)). Phy Address is 0x0

On comparing the MDIO read access waveform in Pass and Fail case, we find that during the turnaround time (duration between RFSOC driving and TI Phy there is a difference.

In the fail case, the TI Phy device seems to have started driving seems to have started driving the Read register value one clock cycle early compared to expected.

We do not see issues in the signal integrity of the waveforms.

We need clarification on what could be causing the TI PHY to drive the MDIO bus one MDC clock cycle earlier than expected.

Note:
With removal of the 100pF capacitor on TXS0102 MDC output, we are not seeing MDIO access failures. However there is higher overshoot on the MDC signal. H
ow does the 100pF capacitor presence on the MDC line cause the TI PHY to sometimes drive the MDIO bus one MDC clock cycle earlier than expected?