

# 953/954 Spectrum Analysis

**FPD Link**

**9/19/19**

# Summary

- This presentation covers the theory behind the frequency spacing of 953 output data spectrum
- Frequency spacing is related to the FPD encoding and will shift as the FPD line rate changes

# Example Spectral Peaks – 25 MHz REFCLK

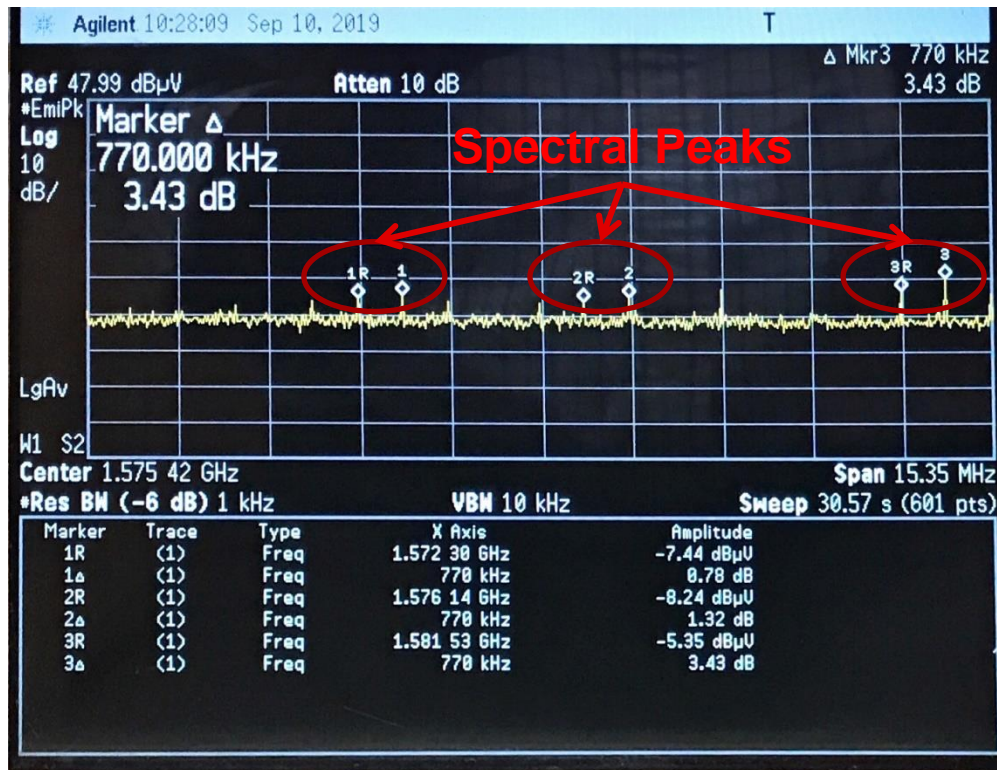
- $Spectral\ Separation = \Delta f$
- $\Delta f = \frac{FPD\ Rate}{130 * FPD\ Frame\ Length}$
- For example FPD Rate = 4Gbps

$$\frac{4000\ Mbps}{40\ bits} = 100\ MHz$$

$$\frac{100\ MHz}{130} \approx 0.77\ MHz = 770\ kHz$$

\*Every 130 bits a DCA/DCB code is inserted

\*FPD frame is 40 bits wide



# System Level EMC Mitigation Techniques

- EMC is a system level specification and will depend on housing, shielding, PCB layout, component selection.
- The following techniques are recommended at the system level to improve EMC performance
  - Use of metal shielding
  - Good grounding techniques
  - Proper differential layout of PCB traces
  - Trace impedance control
- TI's FPD Link III product family supports several clocking features to control emissions at the system level
  - Spread spectrum REFCLK on deserializer when using synchronous clock mode – this spreads the energy across multiple frequencies
    - 953/954/936/936/960/962 FPD Link products fully support SSC feature
  - Use AON clock mode on 953 – this provides inherent spreading from the serializer without needing external SSC REFCLK
  - Where applicable, changing line rate from 4G -> 2G mode to shift energy to different bands

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