Schematic Review Form

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Pin #	Name	Info	Violations	*Description*
1	CC1	Common mode choke to connector		Type-C configuration channel signal 1
2	CC2	Common mode choke to connector		Type-C configuration channel signal 2
3	PORT	4.7K pulldown, UFP mode		Tri-level input pin to indicate port mode. H - DFP (Pull-up to VDD if DFP mode is desired) NC - DRP (Leave unconnected if DRP mode is desired) L - UFP (Pull-down or tie to GND if UFP mode is desired)
4	VBUS_DET	Connected to Type-C VBUS through 909K resistor, F1, and FL11	What is FL11 in the schematic?	5-V to 28-V VBUS input voltage. VBUS detection determines UFP attachment. One 900-kΩ external resistor required between system VBUS and VBUS_DET pin.
5	ADDR	NC, GPIO mode		Tri-level input pin to indicate I2C address or GPIO mode: H — I2C is enabled and I2C 7-bit address is 0x67. NC — GPIO mode (I2C is disabled) L — I2C is enabled and I2C 7-bit address is 0x47. ADDR pin should be pulled up to VDD if high
6	INT_N/OUT3	Pulled up with 200K		The INT_N/OUT3 is a dual-function pin. When used as the INT_N, the pin is an open drain output in I2C control mode and is an active low interrupt signal for indicating changes in I2C registers. When used as OUT3, the pin is in audio accessory detect in GPIO mode: no detection (H), audio accessory connection detected (L).

7	SDA/OUT1	4.7K pullup		The SDA/OUT1 is a dual-function pin. When I2C is enabled (ADDR pin is high or low), this pin is the I2C communication data signal. When in GPIO mode (ADDR pin is NC), this pin is an open drain output for communicating Type-C current mode detect when the device is in UFP mode
8	SCL/OUT2	4.7K pullup		The SCL/OUT2 is a dual function pin. When I2C is enabled (ADDR pin is high or low), this pin is the I2C communication clock signal. When in GPIO mode (ADDR pin is NC), this pin is an open drain output for communicating Type-C current mode detect when the device is in UFP mode
9	ID	NC		Open drain output; asserted low when the CC pins detect device attachment when port is a source (DFP), or dual-role (DRP) acting as source (DFP).
10	GND	GND		Ground
11	EN_N	Pulled to GND		Enable signal; active low. Pulled up to VDD internally to disable the TUSB320L device. If controlled externally, must be held low at least for 50ms after VDD has reached its valid voltage level.
12	VDD	Connected to VBUS		Positive supply voltage. VDD must ramp within 25 ms or less

Comments