PROGRAMMERS REFERENCE

The top 4 control pins PRTAD[4:1] determine the device port address. In this mode, TLK10232 will respond if the PHY address field on the MDIO protocol (PA[4:1]) matches PRTAD[4:1] pin value. In both Clause 45 and Clause 22 modes, the 2 individual channels in TLK10232 are classified as 2 different ports. So for any PRTAD [4:1] value there will be 2 ports per TLK10232. LSB of PHY address field (PA[0]) will determine which channel/port within TLK10232 to respond.
Channel A can be accessed by setting LSB bit of PHY address to 1'b0.
Channel B can be accessed by setting LSB bit of PHY address to 1'b1.
Following Table illustrates device modes with respect to ST and MODE_SEL pins. 10G mode referenced in below table and in the rest of programmer's reference is equivalent to General purpose SERDES mode.

Table 1: Model Selection

	ST = 0 (Clause 45)	ST = 1 (Clause 22)
{MODE_SEL pin, SW bit (30.1.10)}		
1x	10G	10G
01	10G	10G
00	10G-KR/1G-KX (Determined by Auto Neg)	1G-KX (No Auto Neg)

REGISTER ORGANIZATION

- Vendor Specific device Registers (Can be accessed through Clause 45 and Clause 22)
  - Clause 45 device address = 30 (Valid in 10G-KR/1G-KX/10G modes)
    - 30.0 -> Global control registers. These registers contain global control bits and are channel independent.
    - 30.1 to 30.31 -> Channel control/Status registers. These registers contain non-standard defined control/status bits and are per channel basis.
    - 30.32768 to 30.33025 -> Channel control/Status registers. These registers contain non-standard defined control/status bits and are per channel basis. Requires indirect access in Clause 22 mode. Registers that are not implemented
    - 30.40960 to 30.41241 -> Global control/Status registers. These registers contain non-standard defined control/status bits and are channel independent. Requires indirect access in Clause 22 mode
- Standard Device Registers (Can be accessed only through Clause 45 and are channel independent)
  - Clause 45 device address = 1 (Valid in 10G-KR mode)
    - 1.0 to 1.11 -> PMA/PMD control/Status registers.
    - 1.150 to 1.175 -> 10G-KR standard control/Status registers.
    - 1.32768 to 1.36905 -> 10G-KR vendor specific control/Status registers. Also included are link/autotrain related registers. These are also accessible using clause 22 (through indirect addressing and in clause 45 (through device address 30)
  - Clause 45 device address = 3 (Valid in 10G-KR mode)
    - 3.0 to 3.43 -> PCS standard control/Status registers
    - 3.32768, 3.32784 -> PCS vendor specific control/Status registers
  - Clause 45 device address = 7 (Valid in 10G-KR/1G-KX modes)
    - 7.0 to 7.27, 7.48 -> Auto Negotiation standard control/Status registers.
    - 7.32768, 7.32784 -> Auto Negotiation vendor specific control/status registers.

Note: Registers that are not implemented return 0 when read.

REGISTER BIT DEFINITIONS

RW: Read-Write

User can write 0 or 1 to this register bit. Reading this register bit returns the same value that has been written.

RW/SC: Read-Write Self-Clearing

User can write 0 or 1 to this register bit. Writing a "1" to this register creates a high pulse. Reading this register bit always returns 0.

RO: Read-Only

This register can only be read. Writing to this register bit has no effect. Reading from this register bit returns its current value.

RO/LH: Read-Only Latched High

This register can only be read. Writing to this register bit has no effect. Reading a "1" from this register bit indicates that either the condition is occurring or it has occurred since the last time it was read. Reading a "0" from this register bit indicates that the condition is not occurring presently, and it has not occurred since the last time the register was read. A latched high register, when read high, should be read again to distinguish if a condition occurred previously or is still occurring. If it occurred previously, the second read will read low. If it is still occurring, the second read will read high. Reading this register bit automatically resets its value to 0.

RO/LL: Read-Only Latched Low

This register can only be read. Writing to this register bit has no effect. Reading a "0" from this register bit indicates that either the condition is occurring or it has occurred since the last time it was read. Reading a "1" from this register bit indicates that the condition is not occurring presently, and it has not occurred since the last time the register was read. A latched low register, when read low, should be read again to distinguish if a condition occurred previously or is still occurring. If it occurred previously, the second read will read high. If it is still occurring, the second read will read low. Reading this register bit automatically sets its value to 1.

COR: Clear-On-Read counter

This register can only be read. Writing to this register bit has no effect. Reading from this register bit returns its current value, then resets its value to 0. Counter value freezes at Max.

Following code letters in Name field of each control/status register bit(s) indicate the mode that they are applicable/valid.

R = Indicates control/status bit(s) valid in 10GKR mode
X = Indicates control/status bit(s) valid in 1GKX mode
G = Indicates control/status bit(s) valid in 10G general purpose serdes mode

VENDOR SPECIFIC DEVICE REGISTERS

Below registers can be accessed directly through Clause 22 and Clause 45. In Clause 45 mode, these registers can be accessed by setting device address field to 0x1E (DA[4:0] = 5'b11110). In Clause 22 mode, these registers can be accessed by setting 5 bit register address field to same value as 5 LSB bits of Register Address field specified for each register. For example, 16 bit register address 0x001C in clause 45 mode can be accessed by setting register address field to 5'h1C in clause 22 mode.

Table 2: GLOBAL_CONTROL_1[1]

Device Address: 0x1E	Register Address:0x0000	Default: 0x0610	
Bit(s)	**Name**	**Description**	**Access**
30.0.15	GLOBAL_RESET (RXG)	Global reset. 0 = Normal operation (Default 1'b0) 1 = Resets TX and RX data path including MDIO registers. Equivalent to asserting RESET_N.	RW SC[2]
30.0.14:12	PRTAD0_PIN_EN_SEL[2:0] (RXG)	PRTAD0 pin selection control. Valid only when 30.0.5 is 1. PRTAD0 is used for the assignment specified below. 000 = Channel A stopwatch (Default 3'b000) 001 = Channel B stopwatch 010 = Channel A Tx data switch 011 = Channel A Rx data switch 100 = Channel B Tx data switch 101 = Channel B Rx data switch 11x = Reserved	RW
30.0.11	GLOBAL_WRITE (RXG)	Global write enable. 0 = Control settings are specific to channel addressed (Default 1'b0) 1 = Control settings in channel specific registers are applied to both channels regardless of channel addressed	
30.0.10:8	RESERVED SE_CLK_DIV[2:0] (RXG)	For TI use only (Default 3'b110) Single Ended REFCLK Control clock divide selection. This value is used to divide selected single ended reference clock which is used for STCI, EFUSE etc. Divider value should be chosen such that the resulting frequency is at least 2X of MDC. 000 = Divide by 1 001 = Divide by 2 010 = Divide by 4 011 = Divide by 8 100 = Divide by 16 101 = Divide by 32 110 = Divide by 64 (Default 3'b110) 111 = Divide by 128	
30.0.7	RESERVED SE_CLK_SEL (RXG)	For TI use only (Default 1'b0) Single ended REFCLK clock source selection. This clock is used for STCI, EFUSE etc. 0 = Selects single ended version of channel A HS reference clock (as selected by REFCLK _SEL) (Default 1'b0) 1 = Selects single ended version of channel B HS reference clock (as selected by REFCLK_SEL)	
30.0.5	PRTAD0_PIN_EN (RXG)	PRTAD0 pin enable control. 0 = Input pin (PRTAD0) is used for assignment specified in 30.0.14:12 (Default 1'b0) 1 = Input pin (PRTAD0) is not used for assignment specified in 30.0.14:12	

[1] This global register is channel independent.
[2] After reset bit is set to one, it automatically sets itself back to zero on the next MDC clock cycle.

30.0.4:0	PRBS_PASS_OVERLAY[4:0] (RXG)	PRBS_PASS pin status selection. Applicable only when PRBS test pattern verification is enabled on HS side or LS side. PRBS_PASS pin reflects PRBS verification status on selected Channel HS/LS side. LS Serdes lanes 1/2/3 are not applicable in 1GKX modes. 1xx00 = PRBS_PASS reflects combined status of Channel A/B HS serdes PRBS verification. If PRBS verification fails on any channel HS serdes, PRBS_PASS will be asserted low. (Default 5'b10000) 00000 = Status from Channel A HS Serdes side 00001 = Reserved Status from Channel A HS core side 0001x = Reserved 00100 = Status from Channel A LS Serdes side Lane 0 00101 = Status from Channel A LS Serdes side Lane 1 00110 = Status from Channel A LS Serdes side Lane 2 00111 = Status from Channel A LS Serdes side Lane 3 01000 = Status from Channel B HS Serdes side 01001 = Reserved Status from Channel B HS core side 0101x = Reserved 01100 = Status from Channel B LS Serdes side Lane 0 01101 = Status from Channel B LS Serdes side Lane 1 01110 = Status from Channel B LS Serdes side Lane 2 01111 = Status from Channel B LS Serdes side Lane 3	

Table 3: CHANNEL_CONTROL_1

Device Address: 0x1E	Register Address:0x0001	Default: 0x0B00	
Bit(s)	**Name**	**Description**	**Access**
30.1.15	POWERDOWN (RXG)	Setting this bit high powers down entire data path with exception that MDIO interface stays active. 0 = Normal operation (Default 1'b0) 1 = Power Down mode is enabled.	RW
30.1.14	LT_TRAINING_CONTROL (XG)	Link training control. Valid in 10G and 1GKX modes only. 0 = Link training disabled(Default 1'b0) 1 = Link training enable control dependent on LT_TRAINING_ENABLE (1/30.150.1).	
30.1.13	10G_RX_MODE_SEL (G)	RX mode selection. Valid in 10G only. 0 = RX mode dependent upon RX_DEMUX_SEL(Default 1'b0) 1 = Enables 1 to 1 mode on receive channel.	
30.1.12	10G_TX_MODE_SEL (G)	TX mode selection Valid in 10G only. 0 = TX mode dependent upon TX_MUX_SEL (Default 1'b0) 1 = Enables 1 to 1 mode on transmit channel.	
30.1.11	SW_PCS_SEL (RX)	Applicable in Clause 45 mode only. Valid only when MODE_SEL pin is 0, AN_ENABLE (7.0.12) is 0 and SW_DEV_MODE_SEL (30.1.10) is 0. 1 = Set device to 10G-KR mode(Default 1'b1) 0 = Set device to 1G-KX mode	
30.1.10	SW_DEV_MODE_SEL (RXG)	Valid only when MODE_SEL pin is 0 1 = Device set to 10G mode 0 = In clause 45 mode, device mode is set using Auto negotiation. In clause 22 mode, device set to 1G-KX mode(Default 1'b0)	
30.1.9	10G_RX_DEMUX_SEL (G)	RX De-Mux selection control for lane de-serialization on receive channel. Valid in 10G and when 10G_RX_MODE_SEL (30.1.13) is LOW 0 = 1 to 2 1 = 1 to 4 (Default 1'b1)	
30.1.8	10G_TX_MUX_SEL (G)	TX Mux selection control for lane serialization on transmit channel. Valid in 10G and when 10G_TX_MODE_SEL (30.1.12) is LOW 0 = 2 to 1 1 = 4 to 1 (Default 1'b1)	

30.1.7:5	RESERVED HS_FINAL_EQPRE[2:0] (RXG)	For TI use only Final HS Serdes EQPRE value.	RO
30.1.4	RESERVED HS_ FINAL_H1CDRMODE (RXG)	For TI use only Final HS Serdes H1CDR mode value	
30.1.3	RESERVED HS_ FINAL_PK_DISABLE (RXG)	For TI use only Final HS Serdes peak disable value	
30.1.2	RESERVED HS_ FINAL_AGCCTRL_0 (RXG)	For TI use only BIT [0] of final HS Serdes AGCCTRL value	
30.1.1	REFCLK_SW_SEL (RXG)	Channel HS Reference clock selection. 0 = Selects REFCLK_0_P/N as clock reference to Channel x HS side serdes macro(Default 1'b0) 1 = Selects REFCLK_1_P/N as clock reference to Channel x HS side serdes macro	RW
30.1.0	LS_REFCLK_SEL (RXG)	Channel LS Reference clock selection. 0 = LS side serdes macro reference clock is same as HS side serdes reference clock (E.g. If REFCLK_0_P/N is selected as HS side serdes macro reference clock, REFCLK_0_P/N is selected as LS side serdes macro reference clock and vice versa) (Default 1'b0) 1 = Alternate reference clock is selected as clock reference to Channel x LS side serdes macro (E.g. If REFCLK_0_P/N is selected as HS side serdes macro reference clock, REFCLK_1_P/N is selected as LS side serdes macro reference clock and vice versa)	

Table 4: HS_SERDES_CONTROL_1

Device Address: 0x1E	**Register Address:0x0002**	**Default: 0x831D**	
Bit(s)	**Name**	**Description**	**Access**
30.2.15	RESERVED HS_TXCM CFGTX[9] (RXG)	For TI use only (Default 1'b1) Transmit output common mode control. 0 = Normal common mode. Valid for DC settings 1 = Raised common mode. Valid for AC settings (Default 1'b1)	RW
30.2.14	RESERVED HS_ENQOL CFGRX[22] (RXG)	For TI use only (Default 1'b0) 0 = QOL interface port not active 1 = QOL interface port active	
30.2.13	RESERVED HS_ADCGAIN CFGRX[13] (RXG)	For TI use only. (Default 1'b0) HS Serdes ADCGAIN control 0 = AGC Digital control word has normal 1x strength 1 = AGC Digital control word has 2x strength.	
30.2.12	RESERVED HS_JOG CFGRX[12] (RXG)	For TI use only (Default 1'b0) 0 = Vote summation corrected to avoid extra phase updates 1 = Vote summation as in original design	
30.2.11:10	RESERVED HS_CLK_BYPASS[1:0] CFGPLL[11:10] (RXG)	For TI use only (Default 2'b00) HS Serdes PLL bypass settings 00 = No bypass. Macro operates normally from PLL 01 = Reserved 10 = Functional bypass. Macros operate at low speed using TESTCLKT and TESTCLKR 11 = REFCLK observe. Divided version of REFCLKP/N is observable on serial TXP/N pins	
30.2.9:8	HS_LOOP_BANDWIDTH[1:0] CFGPLL[9:8] (RXG)	HS Serdes PLL Loop Bandwidth settings 00 = Medium Bandwidth 01 = Low Bandwidth 10 = High Bandwidth 11 = Ultra High Bandwidth (Default 2'b11)	
30.2.7	RESERVED CFGPLL[7] (RXG)	For TI use only (Default 1'b0) Mapped to HS Serdes CFGPLL[7] for future use	

30.2.6	HS_VRANGE CFGPLL[6] (RXG)	HS Serdes PLL VCO range selection. 0 = VCO runs at higher end of frequency range (Default 1'b0) 1 = VCO runs at lower end of frequency range This bit needs to be set HIGH if VCO frequency (REFCLK * HS_PLL_MULT) is below 2.5 Ghz.	
30.2.5	RESERVED CFGPLL[5] (RXG)	For TI use only (Default 1'b0) Mapped to HS Serdes CFGPLL[5] for future use	
30.2.4	HS_ENPLL CFGPLL[0] (RXG)	HS Serdes PLL enable control. HS Serdes PLL is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 30.1.15 is set HIGH. 0 = Disables PLL in HS serdes 1 = Enables PLL in HS serdes (Default 1'b1)	
30.2.3:0	HS_PLL_MULT[3:0] CFGPLL[4:1] (RXG)	HS Serdes PLL multiplier setting (Default 4'b1101). Refer Table 5: HS PLL multiplier control. In KR/KX modes, this setting is automatically controlled and value set through these register bits is ignored unless REFCLK_FREQ_SEL_1 or related OVERRIDE bit is set. Please see Appendix B for more information on PLL multiplier settings	

Table 5: HS PLL multiplier control

30.2.3:0		30.2.3:0	
Value	**PLL Multiplier factor**	**Value**	**PLL Multiplier factor**
0000	Reserved	1000	12x
0001	Reserved	1001	12.5x
0010	4x	1010	15x
0011	5x	1011	16x
0100	6x	1100	16.5x
0101	8x	1101	20x
0110	8.25x	1110	25x
0111	10x	1111	Reserved

Table 6: HS_ SERDES_CONTROL_2

Device Address: 0x1E	Register Address:0x0003	Default: 0xA848	
Bit(s)	**Name**	**Description**	**Access**
30.3.15:12	HS_SWING[3:0] CFGTX[13:10] (RXG)	Transmitter Output swing control for HS Serdes. During autotrain, this setting is automatically controlled and value set through this register bit is ignored unless related OVERRIDE bit is set. (Default 4'b1010) Refer Table 7: HSTX AC mode output swing control	RW
30.3.11	HS_ENTX CFGTX[0] (RXG)	HS Serdes transmitter enable control. HS Serdes transmitter is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 30.1.15 is set HIGH. 0 = Disables HS serdes transmitter 1 = Enables HS serdes transmitter (Default 1'b1)	
30.3.10	HS_EQHLD CFGRX[24] (RXG)	HSRX Equalizer hold control. During autotrain, this setting is automatically controlled and value set through this register bit is ignored unless related OVERRIDE bit is set. 0 = Normal operation (Default 1'b0) 1 = Holds equalizer and long tail correction in its current state	

30.3.9:8	HS_RATE_TX [1:0] CFGTX[5:4] (RXG)	HS Serdes TX rate settings. In KR/KX modes, this setting is automatically controlled and value set through these register bits is ignored unless REFCLK_FREQ_SEL_1 or related OVERRIDE bit is set. 00 = Full rate (Default 2'b00) 01 = Half rate 10 = Quarter rate 11 = Eighth rate	
30.3.7:6	HS_AGCCTRL[1:0] CFGRX[26:25] (RXG)	Adaptive gain control loop. During autotrain, this setting is automatically controlled and value set through this register bit is ignored unless related OVERRIDE bit is set. 00 = Attenuator will not change after lock has been achieved, even if AGC becomes unlocked 01 = Attenuator will not change when in lock state, but could change when AGC becomes unlocked (Default 2'b01) 10 = Force the attenuator off 11 = Force the attenuator on	
30.3.5:4	HS_AZCAL[1:0] CFGRX[4:3] (RXG)	Auto zero calibration. During autotrain, this setting is automatically controlled and value set through this register bit is ignored unless related OVERRIDE bit is set. 00 = Auto zero calibration initiated when receiver is enabled (Default 2'b00) 01 = Auto zero calibration disabled 10 = Forced with automatic update. 11 = Forced without automatic update	
30.3.3	HS_ENRX CFGRX[0] (RXG)	HS Serdes receiver enable control. HS Serdes receiver is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 30.1.15 is set HIGH. During autotrain, this setting is automatically controlled and value set through this register bit is ignored unless related OVERRIDE bit is set. 0 = Disables HS serdes receiver 1 = Enables HS serdes receiver (Default 1'b1)	
30.3.2:0	HS_RATE_RX [2:0] CFGRX[14], CFGRX[6:5] (RXG)	HS Serdes RX rate settings. In KR/KX modes, this setting is automatically controlled and value set through these register bits is ignored unless REFCLK_FREQ_SEL_1 or related OVERRIDE bit is set. 000 = Full rate (Default 3'b000) 101 = Half rate 110 = Quarter rate 111 = Eighth rate 001 = Reserved 01x = Reserved 100 = Reserved	

Table 7: HSTX AC mode output swing control

Value 30.3[15:12]	AC Mode Typical Amplitude (mVdfpp)
0000	130
0001	220
0010	300
0011	390
0100	480
0101	570
0110	660
0111	750
1000	830
1001	930
1010	1020
1011	1110
1100	1180
1101	1270

1110	1340
1111	1400

Table 8: HS_SERDES_CONTROL_3

Device Address: 0x1E	Register Address:0x0004	Default: 0x1500	
Bit(s)	**Name**	**Description**	**Access**
30.4.15	HS_ENTRACK CFGRX[23] (RXG)	HSRX ADC Track mode. During autotrain, this setting is automatically controlled and value set through this register bit is ignored unless related OVERRIDE bit is set. 0 = Normal operation (Default 1'b0) 1 = Forces ADC into track mode	RW
30.4.14:12	HS_EQPRE[2:0] CFGRX[21:19] (RXG)	Serdes Rx precursor equalizer selection. During autotrain, this setting is automatically controlled and value set through this register bit is ignored unless related OVERRIDE bit is set. 000 = 1/9 cursor amplitude 001 = 3/9 cursor amplitude (Default 3'b001) 010 = 5/9 cursor amplitude 011 = 7/9 cursor amplitude 100 = 9/9 cursor amplitude 101 = 11/9 cursor amplitude 110 = 13/9 cursor amplitude 111 = Disable	
30.4.11:10	HS_CDRFMULT[1:0] CFGRX[18:17] (RXG)	Clock data recovery algorithm frequency multiplication selection(Default 2'b01) During autotrain, this setting is automatically controlled and value set through this register bit is ignored unless related OVERRIDE bit is set. 00 = First order. Frequency offset tracking disabled 01 = Second order. 1x mode 10 = Second order. 2x mode 11 = Reserved	
30.4.9:8	HS_CDRTHR[1:0] CFGRX[16:15] (RXG)	Clock data recovery algorithm threshold selection(Default 2'b01) During autotrain, this setting is automatically controlled and value set through this register bit is ignored unless related OVERRIDE bit is set. 00 = Four vote threshold 01 = Eight vote threshold 10 = Sixteen vote threshold 11 = Thirty two vote threshold	
30.4.7	RESERVED HS_EQLIM CFGRX[2] (RXG)	For TI use only HSRX Equalizer limit control(Default 1'b0) 0 = Normal operation 1 = Limits equalizer DFE tap weights	
30.4.6	HS_PEAK_DISABLE CFGRX[1] (RXG)	HS Serdes PEAK_DISABLE control. During autotrain, this setting is automatically controlled and value set through this register bit is ignored unless related OVERRIDE bit is set. 0 = Normal operation (Default 1'b0) 1 = Disables high frequency peaking. Suitable for <6 Gbps operation	
30.4.5	HS_H1CDRMODE CFGRX[10] (RXG)	HS Serdes H1CDRMODE control. During autotrain, this setting is automatically controlled and value set through this register bit is ignored unless related OVERRIDE bit is set. 0 = Normal operation (Default 1'b0) 1 = Enables CDR mode suitable for short channel operation. Mapped to HS Serdes CFGRX[10]	
30.4.4:0	HS_TWCRF[4:0] CFGTX[22:18] (RXG)	Cursor Reduction Factor (Default 5'b00000. In KR mode, this setting is automatically controlled and value set through this register bits is ignored unless related OVERRIDE bit is set. Refer Table 9: HSTX Cursor reduction factor weights	

Table 9: HSTX Cursor reduction factor weights

30.4.4:0		30.4.4:0	
Value	**Cursor reduction (%)**	**Value**	**Cursor reduction (%)**
00000	0	10000	17
00001	2.5	10001	20
00010	5.0	10010	22
00011	7.5	10011	25
00100	10.0	10100	27
00101	12	10101	30
00110	15	10110	32
00111	Reserved	10111	35
01000		11000	37
01001		11001	40
01010		11010	42
01011		11011	45
01100		11100	47
01101		11101	50
01110		11110	52
01111		11111	55

Table 10: HS_SERDES_CONTROL_4

Device Address: 0x1E	**Register Address:0x0005**	**Default: 0x2000**	
Bit(s)	**Name**	**Description**	**Access**
30.5.15	HS_RX_INVPAIR CFGRX[7] (RXG)	Receiver polarity. 0 = Normal polarity. HSRXxP considered positive data. HSRXxN considered negative data (Default 1'b0) 1 = Inverted polarity. HSRXxP considered negative data. HSRXxN considered positive data	RW
30.5.14	HS_TX_INVPAIR CFGTX[6] (RXG)	Transmitter polarity. 0 = Normal polarity. HSTXxP considered positive data and HSTXxN considered negative data (Default 1'b0) 1 = Inverted polarity. HSTXxP considered negative data and HSTXxN considered positive data	
30.5.13	RESERVED HS_FIRUPT CFGTX[3] (RXG)	For TI use only (Default 1'b1) HS Serdes Tx pre/post cursor filter update control. During autotrain, this setting is automatically controlled and value set through this register bit is ignored unless related OVERRIDE bit is set. 0 = Pre/Post cursor fields cannot be updated 1 = Pre/Post cursor fields can be updated by changing respective fields (Default 1'b1)	
30.5.12:8	HS_TWPOST1[4:0] CFGTX[28:24] (RXG)	Adjacent post cursor1 Tap weight. Selects TAP settings for TX waveform. (Default 5'b00000). In KR mode, this setting is automatically controlled and value set through this register bits is ignored unless related OVERRIDE bit is set. Refer Table 11: HSTX Post-cursor1 transmit tap weights	
30.5.7:4	HS_TWPRE[3:0] CFGTX[17:14] (RXG)	Pre cursor Tap weight. Selects TAP settings for TX waveform. (Default 4'b0000). In KR mode, this setting is automatically controlled and value set through this register bits is ignored unless related OVERRIDE bit is set. Refer Table 13: HSTX Pre-cursor transmit tap weights	
30.5.3:0	HS_TWPOST2[3:0] CFGTX[32:29] (RXG)	Adjacent post cursor2 Tap weight. Selects TAP settings for TX waveform. (Default 4'b0000). In KR mode, this setting is automatically controlled and value set through this register bits is ignored unless related OVERRIDE bit is set. Refer Table 12: HSTX Post-cursor2 transmit tap weights	

Table 11: HSTX Post-cursor1 transmit tap weights

30.5.12:8		30.5.12:8	
Value	**Tap weight (%)**	**Value**	**Tap weight (%)**
00000	0	10000	0
00001	+2.5	10001	-2.5
00010	+5.0	10010	-5.0
00011	+7.5	10011	-7.5
00100	+10.0	10100	-10.0
00101	+12.5	10101	-12.5
00110	+15.0	10110	-15.0
00111	+17.5	10111	-17.5
01000	+20.0	11000	-20.0
01001	+22.5	11001	-22.5
01010	+25.0	11010	-25.0
01011	+27.5	11011	-27.5
01100	+30.0	11100	-30.0
01101	+32.5	11101	-32.5
01110	+35.0	11110	-35.0
01111	+37.5	11111	-37.5

Table 12: HSTX Post-cursor2 transmit tap weights

30.5.3:0		30.5.3:0	
Value	**Tap weight (%)**	**Value**	**Tap weight (%)**
0000	0	1000	0
0001	+2.5	1001	-2.5
0010	+5.0	1010	-5.0
0011	+7.5	1011	-7.5
0100	+10.0	1100	-10.0
0101	+12.5	1101	-12.5
0110	+15.0	1110	-15.0
0111	+17.5	1111	-17.5

Table 13: HSTX Pre-cursor transmit tap weights

30.5.7:4		30.5.7:4	
Value	**Tap weight (%)**	**Value**	**Tap weight (%)**
0000	0	1000	0
0001	+2.5	1001	-2.5
0010	+5.0	1010	-5.0
0011	+7.5	1011	-7.5
0100	+10.0	1100	-10.0
0101	+12.5	1101	-12.5
0110	+15.0	1110	-15.0
0111	+17.5	1111	-17.5

Table 14: LS_SERDES_CONTROL_1

Device Address: 0x1E	**Register Address:0x0006**	**Default: 0xF115**	
Bit(s)	**Name**	**Description**	**Access**

30.6.15:12	LS_LN_CFG_EN[3:0] (RXG)	Configuration control for LS Serdes Lane settings (Default 4'b1111) [3] corresponds to LN3, [2] corresponds to LN2 [1] corresponds to LN1, [0] corresponds to LN0 Lanes 1/2/3 are not valid in 1GKX mode 0 = Writes to LS_SERDES_CONTROL_2 & LS_SERDES_CONTROL_3 & LS_CH_CONTROL_1 control registers do not affect respective LS Serdes lane 1 = Writes to LS_SERDES_CONTROL_2 & LS_SERDES_CONTROL_3 & LS_CH_CONTROL_1 control registers affect respective LS Serdes lane For example, if subsequent writes to LS_SERDES_CONTROL_2 & LS_SERDES_CONTROL_3 & LS_CH_CONTROL_1 registers need to affect the settings in Lanes 0 and 1, LS_LN_CFG_EN[3:0] should be set to 4'b0011 Read values in LS_SERDES_CONTROL_2 & LS_SERDES_CONTROL_3 & LS_CH_CONTROL_1 reflect the settings value for Lane selected through LS_LN_CFG_EN[3:0]. **To read settings for Lane 0, LS_LN_CFG_EN[3:0] should be set to 4'b0001** **To read settings for Lane 1, LS_LN_CFG_EN[3:0] should be set to 4'b0010** **To read settings for Lane 2, LS_LN_CFG_EN[3:0] should be set to 4'b0100** **To read settings for Lane 3, LS_LN_CFG_EN[3:0] should be set to 4'b1000** **Read values of LS_SERDES_CONTROL_2 & LS_SERDES_CONTROL_3 & LS_CH_CONTROL_1 registers are not valid for any other LS_LN_CFG_EN[3:0] combination**	RW
30.6.11:10	RESERVED LS_CLK_BYPASS[1:0] TESTCFG[5:4] (RXG)	For TI use only(Default 2'b00) LS Serdes PLL bypass settings 00 = No bypass. Macro operates normally from PLL 01 = Reserved 10 = Functional bypass. Macros operate at low speed using TESTCLKT and TESTCLKR 11 = REFCLK observe. Divided version of REFCLKP/N is observable on serial OUTx pins	
30.6.9:8	LS_LOOP_BANDWIDTH[1:0] CFGPLL[9:8] (RXG)	LS Serdes PLL Loop Bandwidth settings 00 = Reserved 01 = Applicable when external JC_PLL is NOT used (Default 2'b01) 10 = Applicable when external JC_PLL is used 11 = Reserved	
30.6.7	RESERVED (RXG)	For TI use only (Default 1'b0)	
30.6.6:5	RESERVED CFGPLL[6:5] (RXG)	For TI use only Mapped to LS Serdes CFGPLL[6:5] for future use	
30.6.4	LS_ENPLL CFGPLL[0] (RXG)	LS Serdes PLL enable control. LS Serdes PLL is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 30.1.15 is set HIGH. 0 = Disables PLL in LS serdes 1 = Enables PLL in LS serdes (Default 1'b1)	
30.6.3:0	LS_MPY[3:0] CFGPLL[4:1] (RXG)	LS Serdes PLL multiplier setting (Default 4'b0101). In KR/KX modes, this setting is automatically controlled and value set through this register bits is ignored unless REFCLK_FREQ_SEL_1 or related OVERRIDE bit is set. Refer Table 15: LS PLL multiplier control Please see Appendix B for more information on PLL multiplier settings	

Table 15: LS PLL multiplier control

30.6.3:0		30.6.3:0	
Value	**PLL Multiplier factor**	**Value**	**PLL Multiplier factor**
0000	4x	1000	15x
0001	5x	1001	20x

0010	6x	1010	25x
0011	Reserved	1011	Reserved
0100	8x	1100	Reserved
0101	10x	1101	50x
0110	12x	1110	65x
0111	12.5x	1111	Reserved

Table 16: LS_SERDES_CONTROL_2

Device Address: 0x1E	Register Address:0x0007	Default: 0xDC04	
Bit(s)	**Name**	**Description**	**Access**
30.7.15	RESERVED LS_CM CFGTX[8] (RXG)	For TI use only. LS Serdes output common mode adjustment 0 = Normal common mode. Valid for DC settings 1 = Raised common mode. Valid for AC settings (Default 1'b1)	RW
30.7.14:12	LS_SWING[2:0] CFGTX[11:9] (RXG)	Output swing control on LS Serdes side. (Default 3'b101) Refer Table 17: LSRX Output AC mode output swing control	
3.7.11	LS_LOS CFGRX[15] (RXG)	LS Serdes LOS detector control 0 = Disable Loss of signal detection on LS serdes lane inputs 1 = Enable Loss of signal detection on LS serdes lane inputs (Default 1'b1)	
30.7.10	LS_TX_ENRX CFGRX[0] (RXG)	LS Serdes enable control on the transmit channel. LS Serdes per lane on transmitter channel is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 30.1.15 is set HIGH. Lanes 3 and 2 are automatically disabled when in 2ln 10G mode on transmit channel. Lanes 3, 2 and 1 are automatically disabled when in 1ln 10G mode or 1G-KX mode on transmit channel. 0 = Disables LS serdes lane 1 = Enables LS serdes lane (Default 1'b1)	
30.7.9:8	LS_TX_RATE [1:0] CFGRX[6:5] (RXG)	LS Serdes lane rate settings on transmit channel. In KR/KX modes, this setting is automatically controlled and value set through this register bits is ignored unless REFCLK_FREQ_SEL_1 or related OVERRIDE bit is set. 00 = Full rate (Default 2'b00) 01 = Half rate 10 = Quarter rate 11 = Reserved	
30.7.7:4	LS_DE[3:0] CFGTX[15:12] (RXG)	LS Serdes De-emphasis settings. (Default 4'b0000) Refer Table 18: LSRX Output De-emphasis	
30.7.3	RESERVED LS_ENFTP CFGTX[16] (RXG)	For TI use only . LS Serdes TXBCLK phase control 0 = Arbitrary phase (Default 1'b0) 1 = Fixed phase	
30.7.2	LS_RX_ENTX CFGTX[0] (RXG)	LS Serdes lane enable control on receive channel. LS Serdes per lane on receiver channel is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 30.1.15 is set HIGH. Lanes 3 and 2 are automatically disabled when in 2ln 10G mode on receive channel. Lanes 3, 2 and 1 are automatically disabled when in 1ln 10G or 1G-KX mode on receive channel. 0 = Disables LS serdes lane 1 = Enables LS serdes lane (Default 1'b1)	
30.7.1:0	LS_RX_RATE [1:0] CFGTX[6:5] (RXG)	LS Serdes lane rate settings on receive channel. In KR/KX modes, this setting is automatically controlled and value set through this register bits is ignored unless REFCLK_FREQ_SEL_1 or related OVERRIDE bit is set. 00 = Full rate (Default 2'b00) 01 = Half rate 10 = Quarter rate 11 = Reserved	

Table 17: LSRX Output AC mode output swing control

Value 30.7.14:12	AC Mode Typical Amplitude (mVdfpp)
000	190
001	380
010	560
011	710
100	850
101	950
110	1010
111	1050

Table 18: LSRX Output De-emphasis

30.7.7:4			30.7.7:4		
Value	Amplitude reduction		Value	Amplitude reduction	
	(%)	dB		(%)	dB
0000	0	0	1000	38.08	-4.16
0001	4.76	-0.42	1001	42.85	-4.86
0010	9.52	-0.87	1010	47.61	-5.61
0011	14.28	-1.34	1011	52.38	-6.44
0100	19.04	-1.83	1100	57.14	-7.35
0101	23.8	-2.36	1101	61.9	-8.38
0110	28.56	-2.92	1110	66.66	-9.54
0111	33.32	-3.52	1111	71.42	-10.87

Table 19: LS_SERDES_CONTROL_3

Device Address: 0x1E	Register Address:0x0008	Default: 0x000D	
Bit(s)	**Name**	**Description**	**Access**
30.8.15	LS_RX_INVPAIR CFGTX[7] (RXG)	LS Serdes lane outputs polarity on the receive channel. (x = Channel A or B or C or D, y = Lane 0 or 1 or 2 or 3) 0 = Normal polarity. OUTxyP considered positive data. OUTxyN considered negative data (Default 1'b0) 1 = Inverted polarity. OUTxyP considered negative data. OUTxyN considered positive data	RW
30.8.14	LS_TX_INVPAIR CFGRX[7] (RXG)	LS Serdes lane inputs polarity on the transmit channel. (x = Channel A or B or C or D, y = Lane 0 or 1 or 2 or 3) 0 = Normal polarity. INxyP considered positive data and INxyN considered negative data (Default 1'b0) 1 = Inverted polarity. INxyP considered negative data and INxyP considered positive data	
30.8.13:12	RESERVED LS_ALIGN[1:0] CFGRX[13:12] (RXG)	For TI use only (Default 2'b00) LS Serdes symbol alignment control on the inputs 00 = Alignment disabled 01 = Comma alignment enabled 10 = Alignment jog 11 = Reserved	
30.8.11:8	LS_EQ[3:0] CFGRX[22:19] (RXG)	LS Serdes Equalization control (Default 4'b0000). Table 20: LS_EQ Serdes Equalization	
30.8.7	RESERVED LS_ENOC CFGRX[23] (RXG)	For TI use only (Default 1'b0) LS Serdes Offset compensation control (Default 1'b0)	

30.8.6:4	RESERVED LS_CDR[2:0] CFGRX[18:16] (RXG)	For TI use only (Default 3'b000) LS Serdes CDR control (Default 3'b000) 000 = 1st Order. Threshold of 1 001 = 1st Order. Threshold of 17 010 = 2nd Order. High precision. Threshold of 1 011 = 2nd Order. High precision. Threshold of 17 100 = 1st Order. Low precision. Threshold of 1 101 = 2nd Order. Low precision. Threshold of 17 11x = Reserved	
30.8.3	RESERVED LS_TX_ENTEST CFGRX[1] (RXG)	For TI use only (Default 1'b1) LS Serdes test mode control on the transmit channel 0 = Normal operation 1 = Enable test mode	
30.8.2	RESERVED LS_RX_ENTEST CFGTX[1] (RXG)	For TI use only (Default 1'b1) LS Serdes test mode control on the receive channel 0 = Normal operation 1 = Enable test mode	
30.8.1:0	RESERVED LS_TERM CFGRX[9:8] (RXG)	For TI use only (Default 2'b01) LS Serdes input termination 00 = Common point connected to VDDT (for AC coupled systems) 01 = Common point set to 0.8 VDDT (for AC coupled systems) 10 = Reserved 11 = Common point floating (for AC coupled systems)	

Table 20: LS_EQ Serdes Equalization

30.8.11:8			30.8.11:8		
Value	**Low Freq Gain**	**Zero Freq**	**Value**	**Low Freq Gain**	**Zero Freq**
0000	Maximum		1000	Adaptive	365 MHz
0001	Adaptive		1001		275 MHz
0010	Reserved		1010		195 MHz
0011			1011		140 MHz
0100			1100		105 MHz
0101			1101		75 MHz
0110			1110		55 MHz
0111			1111		50 MHz

Table 21: HS_OVERLAY_CONTROL

Device Address: 0x1E	**Register Address:0x0009**	**Default: 0x0380**	
Bit(s)	**Name**	**Description**	**Access**
30.9.15:14	LS_OK_OUT_GATE[1:0] (G)	LS_OK_OUT gating control X0 = Gating disabled (Default 2'b00) 01 = Gating enabled. LS_OK_OUT gated to LOW 11 = Gating enabled. LS_OK_OUT gated to HIGH	RW
30.9.13:12	LS_OK_IN_GATE[1:0] (G)	LS_OK_IN gating control X0 = Gating disabled (Default 2'b00) 01 = Gating enabled. LS_OK_IN gated to LOW 11 = Gating enabled. LS_OK_IN gated to HIGH	
30.9.11	RESERVED RESERVED_TBD (RXG)	For TI use only. (Default 1'b0) TBD	
30.9.10	RESERVED HS_ENTXCKS CFGTX[1] (RXG)	For TI use only (Default 1'b0) Valid only when HS_ENTX is LOW. 0 = HS serdes transmitter is fully powered off 1 = Enable serdes byte clock generation	

30.9.9:8	RESERVED HS_BUSWIDTH CFGRX[9:8] (RXG)	For TI use only. (Default 2'b11) HS TX/RX Buswidth control. 00 = 8-bit Operation. Valid during Auto Negotiation only. 01 = Reserved 10 = 16-bit Operation. Valid in 10GKR mode only. 11 = 20-bit Operation. Valid in 1GKX and 10G mode only.	
30.9.7	HS_LOS_MASK (G)	0 = HS Serdes LOS status is used to generate HS channel synchronization status. If HS Serdes indicates LOS, channel synchronization indicates synchronization is not achieved 1 = HS Serdes LOS status is not used to generate HS channel synchronization status (Default 1'b1)	
30.9.5	HS_CH_SYNC_OVERLAY (RXG)	0 = LOSx pin does not reflect receive channel loss of channel synchronization status or loss of block lock (Default 1'b0) 1 = Allows channel loss of synchronization or loss of block lock to be reflected on LOSx pin	
30.9.4	HS_INVALID_CODE_OVERLAY (RXG)	0 = LOSx pin does not reflect receive channel invalid code word error (Default 1'b0) 1 = Allows invalid code word error to be reflected on LOSx pin	
30.9.3	HS_AGCLOCK_OVERLAY (RXG)	0 = LOSx pin does not reflect HS Serdes AGC unlock status (Default 1'b0) 1 = Allows HS Serdes AGC unlock status to be reflected on LOSx pin	
30.9.2	HS_AZDONE_OVERLAY (RXG)	0 = LOSx pin does not reflect HS Serdes auto zero calibration not done status (Default 1'b0) 1 = Allows auto zero calibration not done status to be reflected on LOSx pin	
30.9.1	HS_PLL_LOCK_OVERLAY (RXG)	0 = LOSx pin does not reflect loss of HS Serdes PLL lock status (Default 1'b0) 1 = Allows HS Serdes loss of PLL lock status to be reflected on LOSx pin	
30.9.0	HS_LOS_OVERLAY (RXG)	0 = LOSx pin does not reflect HS Serdes Loss of signal condition (Default 1'b0) 1 = Allows HS Serdes Loss of signal condition to be reflected on LOSx pin	

Table 22: LS_OVERLAY_CONTROL

Device Address: 0x1E	**Register Address:0x000A**	**Default: 0x4000**	
Bit(s)	**Name**	**Description**	**Access**
30.10.15:14	RESERVED LAM_SEQ_REPEAT[1:0] (G)	For TI use only (Default 2'b01) LAM Sequence repeat control 00 = LAM sequence repeated 2 times 01 = LAM sequence repeated 4 times 10 = LAM sequence repeated 8 times 11 = LAM sequence repeated 16 times	RW
30.10.13	RESERVED (RXG)	For TI use only (Default 1'b0)	
30.10.12	LS_PLL_LOCK_OVERLAY (RXG)	0 = LOSx pin does not reflect loss of LS SERDES PLL lock status (Default 1'b0) 1 = Allows LS SERDES loss of PLL lock status to be reflected on LOSx pin	
30.10.11:8	LS_CH_SYNC_OVERLAY_LN[3:0] (RXG)	[3] Corresponds to Lane 3, [2] Corresponds to Lane 2 [1] Corresponds to Lane 1, [0] Corresponds to Lane 0 0 = LOSx pin does not reflect LS Serdes lane loss of synchronization condition (Default 1'b0) 1 = Allows LS serdes lane loss of synchronization condition to be reflected on LOSx pin	
30.10.7:4	LS_INVALID_CODE_OVERLAY_LN[3:0] (RXG)	[3] Corresponds to Lane 3, [2] Corresponds to Lane 2 [1] Corresponds to Lane 1, [0] Corresponds to Lane 0 0 = LOSx pin does not reflect LS Serdes lane invalid code condition (Default 1'b0) 1 = Allows LS serdes lane invalid code condition to be reflected on LOSx pin	

30.10.3:0	LS_LOS_OVERLAY_LN[3:0] (RXG)	[3] Corresponds to Lane 3, [2] Corresponds to Lane 2 [1] Corresponds to Lane 1, [0] Corresponds to Lane 0 Lanes 1/2/3 are not applicable in 1GKX mode 0 = LOSx pin does not reflect LS Serdes lane Loss of signal condition (Default 1'b0) 1 = Allows LS serdes lane Loss of signal condition to be reflected on LOSx pin	

Table 23: LOOPBACK_TP_CONTROL

Device Address: 0x1E	Register Address:0x000B	Default: 0x0D10	
Bit(s)	**Name**	**Description**	**Access**
30.11.15:14	RESERVED HS_SERDES_TP_SEL[1:0] (RXG)	For TI use only. Test Pattern Selection. 00 = Reserved (Default 2'b00) 01 = Reserved 10 = Clock pattern with a period of 4 UI 11 = Clock pattern with a period of 2 UI (generation only)	RW
30.11.13	HS_TP_GEN_EN (RXG)	0 = Normal operation (Default 1'b0) 1 = Activates test pattern generation selected by bits 30.11.10:8 or 30.11.15:14	
30.11.12	HS_TP_VERIFY_EN (RXG)	0 = Normal operation (Default 1'b0) 1 = Activates test pattern verification selected by bits 30.11.10:8 or 30.11.15:14	
30.11.11	LS_TEST_PATT_SEL[2] (RXG)	See selection in 30.11.5:4	
30.11.10:8	HS_TEST_PATT_SEL[2:0] (RXG)	Test Pattern Selection. Refer Test pattern procedures section for more information. H/L/M/CRPAT valid in 1GKX/10G modes 000 = High Frequency Test Pattern 001 = Low Frequency Test Pattern 010 = Mixed Frequency Test Pattern 011 = CRPAT Long 100 = CRPAT Short PRBS pattern valid in 1GKX/10G/10GKR modes. 101 = 2^7 - 1 PRBS pattern (Default 3'b101) 110 = 2^{23} - 1 PRBS pattern 111 = 2^{31} - 1 PRBS pattern Errors can be checked by reading HS_ERROR_COUNT register For KR standard pattern generation and verification, please refer to Register 3.42 Valid only when SERDES_TP_SEL[1:0] (30.11.15:14) is 2'b00	
30.11.7	LS_TP_GEN_EN (RXG)	0 = Normal operation (Default 1'b0) 1 = Activates test pattern generation selected by bits {30.11.11, 30.11.5:4} on the LS side Requires setting of LS_RX_ENTEST (30.8.2) for desired lane on the LS side in case of PRBS pattern	
30.11.6	LS_TP_VERIFY_EN (RXG)	0 = Normal operation (Default 1'b0) 1 = Activates PRBS/CRPAT test pattern verification selected by bits {30.11.11, 30.11.5:4} on the LS side Requires setting of LS_TX_ENTEST (30.8.3) for desired lane on the LS side in case of PRBS pattern	

30.11.5:4	LS_TEST_PATT_SEL[1:0] (RXG)	LS Test Pattern Selection LS_TEST_PATT_SEL[2:0]. Refer Test pattern procedures section for more information. LS_TEST_PATT_SEL[2] is 30.11.11 000 = High Frequency Test Pattern 001 = Low Frequency Test Pattern 010 = Mixed Frequency Test Pattern 011 = CRPAT Long (In 1GKX mode only) 100 = CRPAT Short (In 1GKX mode only) 101 = 2^7 - 1 PRBS pattern (Default 3'b101) 110 = 2^{23} - 1 PRBS pattern 111 = 2^{31} - 1 PRBS pattern For XAUI standard test pattern generation and verification in KR mode, please refer register 1.32770 and 1.32771	
30.11.3	DEEP_REMOTE_LPBK TESTCFG[6] (RXG)	0 = Normal functional mode (Default 1'b0) 1 = Enable deep remote loopback mode Requires setting of LS_TX_ENTEST (30.8.3) and LS_RX_ENTEST (30.8.2) for desired lane on the LS side	
30.11.2	RESERVED PAD_REMOTE_LPBK (RXG)	For TI use only (Default 1'b0) Loopback control. Works in conjunction with DEEP_REMOTE_LPBK. Requires setting of LS_TX_ENTEST (30.8.3) and LS_RX_ENTEST (30.8.2) for desired lane on the LS side {30.11.3, 30.11.2} 00 = Loopback Disabled 01 = Inner loopback with CML drive disabled 10 = Inner loopback with CML driver enabled / Deep remote loopback enabled 11 = Pad loopback	
30.11.1	DEEP_LOCAL_LPBK (RXG)	0 = Normal functional mode (Default 1'b0) 1 = Enable deep local loopback mode	
30.11.0	SHALLOW_LOCAL_LPBK (RXG)	0 = Normal functional mode (Default 1'b0) 1 = Enable shallow local loopback mode	

Table 24: LS_CONFIG_CONTROL

Device Address: 0x1E	Register Address:0x000C	Default: 0x0330	
Bit(s)	**Name**	**Description**	**Access**
30.12.15	RESERVED KR_ALIGN_CODE_OVERIDE (R)	For TI use only. (Default 1'b0) Applicable in 10GKR mode only. 0 = Lane align on LS side operates normally as per XAUI standard. Uses /A/ character for lane alignment 1 = Use characters specified in VS_10G_ALIGN_ACODE_P/N instead /A/ character for lane alignment	RW
30.12.14	RESERVED LS_LN_ALIGN_BYPASS (RG)	For TI use only. (Default 1'b0) 0 = Lane align on LS side operates normally(Default 1'b0) 1 = Bypass lane align on LS side	
30.12.13:12	LS_STATUS_CFG[1:0] (RG)	Selects selected lane status to be reflected in LS_STATUS_1 register 0x15 00 = Lane 0 (Default 2'b00) 01 = Lane 1 10 = Lane 2 11 = Lane 3	
30.12.9:8	RESERVED LAS_LA_COL_CFG[1:0] (G)	For TI use only. (Default 2'b11) Minimum distance between align character in Lane alignment slave 00 = 8 01 = 16 1x = 24(Default 2'b11)	
30.12.7:6	RESERVED HS_FINAL_CDRFMULT[1:0] (RXG)	For TI use only Final HS Serdes CDRFMULT value.	RO

30.12.5	LS_LOS_MASK (G)	0 = LS Serdes LOS status of enabled lanes is used to generate link status 1 = LS Serdes LOS status of enabled lanes is not used to generate link status (Default 1'b1)	RW
30.12.4	LS_PLL_LOCK_MASK (G)	0 = LS Serdes PLL Lock status is used to generate link status 1 = LS Serdes PLL Lock status is not used to generate link status (Default 1'b1)	
30.12.2	FORCE_LM_REALIGN (G)	0 = Normal operation (Default 1'b0) 1 = Force lane realignment in Link status monitor	RW/SC
30.12.1:0	RESERVED HS_FINAL_CDRTHR[1:0] (RXG)	For TI use only Final HS Serdes CDRTHR value.	RO

Table 25: CLK_CONTROL

Device Address: 0x1E	Register Address:0x000D	Default: 0x2F80	
Bit(s)	**Name**	**Description**	**Access**
30.13.13	CLKOUT_EN (RXG)	Output clock enable. 0 = Holds CLKOUTx_P/N output to a fixed value. 1 = Allows CLKOUTx_P/N output to toggle normally (Default 1'b1)	RW
30.13.12	CLKOUT_POWERDOWN (RXG)	0 = Normal operation (Default 1'b0) 1 = Enable CLKOUTx_P/N Power Down.	
30.13.11	RESERVERD ADST_CLK_EN (RXG)	For TI use only. Enable clock for the regions after data switch regions on transmit direction. 0 = Disable clock for the regions after data switch regions on transmit direction 1 = Enable clock for the regions after data switch regions on transmit direction (Default 1'b1)	
30.13.10	RESERVERD BDST_CLK_EN (RXG)	For TI use only. Enable clock for the regions before data switch regions on transmit direction. 0 = Disable clock for the regions before data switch regions on transmit direction 1 = Enable clock for the regions before data switch regions on transmit direction (Default 1'b1)	
30.13.9	RESERVERD ADSR_CLK_EN (RXG)	For TI use only. Enable clock for the regions after data switch regions on receive direction. 0 = Disable clock for the regions after data switch regions on receive direction 1 = Enable clock for the regions after data switch regions on receive direction (Default 1'b1)	
30.13.8	RESERVERD BDSR_CLK_EN (RXG)	For TI use only. Enable clock for the regions before data switch regions on receive direction. 0 = Disable clock for the regions before data switch regions on receive direction 1 = Enable clock for the regions before data switch regions on receive direction (Default 1'b1)	

30.13.7:4	CLKOUT_DIV[3:0] (RXG)	Output clock divide setting. This value is used to divide selected clock (Selected using CLKOUT_SEL) before giving it out onto respective channel CLKOUTx_P/N. 0000 = Divide by 1 0001 = Divide by 2 RESERVED 0010 = Divide by 4 RESERVED 0011 = Divide by 5 RESERVED 0100 = Divide by 2 0101 = Divide by 4 RESERVED 0110 = Divide by 8 RESERVED 0111 = Divide by 10 RESERVED 1000 = Divide by 4 (Default 4'b1000) 1001 = Divide by 8 1010 = Divide by 16 1011 = Divide by 20 RESERVED 1100 = Divide by 5 1101 = Divide by 10 1110 = Divide by 20 1111 = Divide by 25	
30.13.3:0	CLKOUT_SEL[3:0] (RXG)	Output clock select. Selected Recovered clock sent out on CLKOUTxP/N pins (Default 4'b0000) 00x0 = Selects Ch A HS recovered byte clock as output clock 00x1 = Selects Ch A HS transmit byte clock as output clock 010x = Selects Ch A HSRX VCO divide by 4 clock as output clock 0110 = Selects Ch A LS recovered byte clock as output clock 0111 = Selects Ch A LS transmit byte clock as output clock 10x0 = Selects Ch B HS recovered byte clock as output clock 10x1 = Selects Ch B HS transmit byte clock as output clock 110x = Selects Ch B HSRX VCO divide by 4 clock as output clock 1110 = Selects Ch B LS recovered byte clock as output clock 1111 = Selects Ch B LS transmit byte clock as output clock	

Table 26: RESET_CONTROL

Device Address: 0x1E	Register Address:0x000E	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.14.7	RESERVED ADST_RESET (RXG)	For TI use only. Software datapath reset for the regions after data switch regions on transmit direction. 0 = Normal operation. (Default 1'b0) 1 = Resets ADST portion.	RW/ SC[3]
30.14.6	RESERVED BDST_RESET (RXG)	For TI use only. Software datapath reset for the regions before data switch regions on transmit direction. 0 = Normal operation. (Default 1'b0) 1 = Resets BDST portion.	
30.14.5	RESERVED ADSR_RESET (RXG)	For TI use only. Software datapath reset for the regions after data switch regions on receive direction. 0 = Normal operation. (Default 1'b0) 1 = Resets ADSR portion.	
30.14.4	RESERVED BDSR_RESET (RXG)	For TI use only. Software datapath reset for the regions before data switch regions on receive direction. 0 = Normal operation. (Default 1'b0) 1 = Resets BDSR portion.	

[3] After reset bit is set to one, it automatically sets itself back to zero on the next MDC clock cycle.

30.14.3	DATAPATH_RESET (RXG)	Channel datapath reset control. Required once the desired functional mode is configured. 0 = Normal operation. (Default 1'b0) 1 = Resets channel logic excluding MDIO registers. (Resets both Tx and Rx datapath)	RW SC[4]
30.14.2	TXFIFO_RESET (G)	Transmit FIFO reset control. Applicable in 10G mode only. Not required in 10GKR mode as 10GKR FIFO is self centering. 0 = Normal operation. (Default 1'b0) 1 = Resets transmit datapath FIFO.	
30.14.1	RXFIFO_RESET (G)	Receive FIFO reset control. Applicable in 10G mode only. Not required in 10GKR mode as 10GKR FIFO is self centering. 0 = Normal operation. (Default 1'b0) 1 = Resets receive datapath FIFO.	

Table 27: CHANNEL_STATUS_1

Device Address: 0x1E	Register Address:0x000F	Default: 0x0000

Bit(s)	Name	Description	Access
30.15.15	HS_TP_STATUS (XG)	Test Pattern status for High/Low/Mixed/CRPAT test patterns. Valid in 10G/1GKX modes. 1 = Alignment has achieved and correct pattern has been received. Any bit errors are reflected in HS_ERROR_COUNTER register (0x10) 0 = Alignment has not been determined	RO
30.15.14	LS_ALIGN_STATUS (RXG)	Lane alignment status In 1GKX mode, this bit reflects test pattern sync status for 1GKX High/Low/Mixed/CRPAT test patterns. 1 = Lane alignment is achieved on the LS side 0 = Lane alignment is not achieved on the LS side	RO/LL
30.15.13	HS_LOS (RXG)	Loss of Signal Indicator. When high, indicates that a loss of signal condition is detected on HS serial receive inputs	RO/LH
30.15.12	HS_AZ_DONE (RXG)	Auto zero complete indicator. When high, indicates auto zero calibration is complete	RO/LL
30.15.11	HS_AGC_LOCKED (RXG)	Adaptive gain control loop lock indicator. When high, indicates AGC loop is in locked state	
30.15.10	HS_CHANNEL_SYNC (RXG)	Channel synchronization status indicator. When high, indicates channel synchronization has achieved	
30.15.9	RESERVED HS_ENCODE_INVALID (RXG)	For TI use only Valid when encoder is enabled and during High//Low/Mixed/CRPAT test pattern generation. When high, indicates encoder received an invalid control word.	RO/LH
30.15.8	HS_DECODE_INVALID (RXG)	Valid when decoder is enabled and during CRPAT test pattern verification. When high, indicates decoder received an invalid code word, or a 8b/10b disparity error. In functional mode, number of DECODE_INVALID errors are reflected in HS_ERROR_COUNTER register (0x10)	
30.15.7	TX_FIFO_UNDERFLOW (RG)	Not applicable in 1GKX mode. When high, indicates underflow has occurred in the transmit datapath (CTC) FIFO.	
30.15.6	TX_FIFO_OVERFLOW (RXG)	When high, in 10GKR and 10G modes indicates overflow has occurred in the transmit datapath (CTC) FIFO. In 1GKX mode, indicates transmit FIFO is reset.	

[4] After reset bit is set to one, it automatically sets itself back to zero on the next MDC clock cycle.

30.15.5	RX_FIFO_UNDERFLOW (RG)	Not applicable in 1GKX mode. When high, indicates underflow has occurred in the receive datapath (CTC) FIFO.	
30.15.4	RX_FIFO_OVERFLOW (RXG)	When high, in 10GKR and 10G modes indicates overflow has occurred in the receive datapath (CTC) FIFO. In 1GKX mode, indicates receive FIFO is reset.	
30.15.3	RX_LS_OK (G)	Receive link status indicator from system side. Applicable in 10G mode only When high, indicates receive link status is achieved on the system side Mapped to input pin invert of LS_OK_IN_x of respective channel	RO/LL
30.15.2	TX_LS_OK (G)	Link status indicator from Lane alignment/Link training slave inside TLK10232 When high, indicates 10G Link align achieved sync and alignment Inverted Raw status signal sent out through output pin LS_OK_OUT_x of respective channel	
30.15.1	LS_PLL_LOCK (RXG)	LS Serdes PLL lock indicator When high, indicates LS Serdes PLL achieved lock to the selected incoming REFCLK0/1_P/N	
30.15.0	HS_PLL_LOCK (RXG)	HS Serdes PLL lock indicator When high, indicates HS Serdes PLL achieved lock to the selected incoming REFCLK0/1_P/N	

Table 28: HS_ERROR_COUNTER

Device Address: 0x1E	Register Address:0x0010	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
30.16.15:0	HS_ERR_COUNT[15:0] (RXG)	In functional mode, this counter reflects number of invalid code words (includes disparity errors) received by decoder. In 10GKR mode, reading this register also clears value in 3.33.7:0. In 10GKR mode, default value for this register is 16'h0000. In HS test pattern verification mode , this counter reflects error count for the test pattern selected through 30.11.10:8 When PRBS_EN pin is set, this counter reflects error count for selected PRBS pattern. Counter value cleared to 16'h0000 when read.	COR

Table 29: LS_LN0_ERROR_COUNTER

Device Address: 0x1E	Register Address:0x0011	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
30.17.15:0	LS_LN0_ERR_COUNT[15:0] (RXG)	Lane 0 Error counter In 10GKR/1GKX functional modes, this counter reflects number of invalid code words (includes disparity errors) received by decoder In 10G functional mode, this counter reflects number of invalid code words (includes disparity errors) received by decoder in lane alignment slave. In LS test pattern verification mode , this counter reflects error count for the test pattern selected through 30.11.5:4 Counter value cleared to 16'h0000 when read.	COR

Table 30: LS_LN1_ERROR_COUNTER

Device Address: 0x1E	Register Address:0x0012	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**

30.18.15:0	LS_LN1_ERR_COUNT[15:0] (RG)	Lane 1 Error counter In 10GKR functional mode, this counter reflects number of invalid code words (includes disparity errors) received by decoder In 10G functional mode, this counter reflects number of invalid code words (includes disparity errors) received by decoder in lane alignment slave. In LS test pattern verification mode , this counter reflects error count for the test pattern selected through 30.11.5:4 Counter value cleared to 16'h0000 when read.	COR

Table 31: LS_LN2_ERROR_COUNTER

Device Address: 0x1E	Register Address:0x0013	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
30.19.15:0	LS_LN2_ERR_COUNT[15:0] (RG)	Lane 2 Error counter In 10GKR functional mode, this counter reflects number of invalid code words (includes disparity errors) received by decoder In 10G functional mode, this counter reflects number of invalid code words (includes disparity errors) received by decoder in lane alignment slave. In LS test pattern verification mode , this counter reflects error count for the test pattern selected through 30.11.5:4 Counter value cleared to 16'h0000 when read.	COR

Table 32: LS_LN3_ERROR_COUNTER

Device Address: 0x1E	Register Address:0x0014	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
30.20.15:0	LS_LN3_ERR_COUNT[15:0] (RG)	Lane 3 Error counter In 10GKR functional mode, this counter reflects number of invalid code words (includes disparity errors) received by decoder In 10G functional mode, this counter reflects number of invalid code words (includes disparity errors) received by decoder in lane alignment slave. n LS test pattern verification mode , this counter reflects error count for the test pattern selected through 30.11.5:4 Counter value cleared to 16'h0000 when read.	COR

Table 33: LS_STATUS_1

Device Address: 0x1E	Register Address:0x0015	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.21.15	RESERVED LAM_ ALIGN_SEQ_ST (G)	For TI use only. LAM Lane align sequence state. Applicable in 10G mode only. 0 = Sending normal traffic 1 = Sending lane align sequence	RO
30.21.14:12	RESERVED LS_LN_ALIGN_STATE[2:0] (RG)	For TI use only. LS Lane alignment state	RO
30.21.11	LS_INVALID_DECODE (RXG)	LS Invalid decode error for selected lane. Lane can be selected through LS_STATUS_CFG[1:0] (Register 30.12). Error count for each lane can also be monitored through respective LS_LNx_ERR_COUNT registers	RO/LH
30.21.10	LS_LOS (RXG)	Loss of Signal Indicator. When high, indicates that a loss of signal condition is detected on LS serial receive inputs for selected lane. Lane can be selected through LS_STATUS_CFG[1:0] (Register 30.12)	RO/LH

30.21.9	LS_LN_ALIGN_FIFO_ERR (RG)	LS Lane alignment FIFO error status 1 = Lane alignment FIFO on LS side has error 0 = Lane alignment FIFO on LS side has no error	RO/LH
30.21.8	LS_CH_SYNC_STATUS (RXG)	LS Channel sync status for selected lane. Lane can be selected through LS_STATUS_CFG[1:0] (Register 30.12)	RO/LL
30.21.7:4	RESERVED LS_CH_SYNC_STATE[3:0] (RXG)	For TI use only. LS Channel sync state for selected lane. Lane can be selected through LS_STATUS_CFG[1:0] (Register 30.12). In 10GKR and 10G modes, [6:4] reflects 3 bit LS sync state. In 1GKX mode, [7:4] reflects 4 bit LS sync state. [7] always reads 0 in 10GKR and 10G modes.	RO
30.21.3:0	LS_CHSYNC_ROT[3:0] (RXG)	Channel synchronization pointer on LS side. Required for latency measurement function. See Latency Measurement function section for more details.	RO

Table 34: HS_STATUS_1

Device Address: 0x1E	Register Address:0x0016	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.22.15	RESERVED LS_PLL_LOCK_R (RXG)	For TI use only. LS Serdes PLL lock indicator. This is raw PLL LOCK status signal coming from LS serdes. When high, indicates LS Serdes PLL achieved lock to the selected incoming REFCLK0/1_P/N	RO
30.22.14	RESERVED HS_PLL_LOCK_R (RXG)	For TI use only. HS Serdes PLL lock indicator. This is raw PLL LOCK status signal coming from HS serdes. When high, indicates HS Serdes PLL achieved lock to the selected incoming REFCLK0/1_P/N	
30.22.13	RESERVED LS_PLL_LOCK_SYNC_LL (RXG)	For TI use only. LS Serdes PLL lock indicator. This LL signal is generated from sync'ed version of raw PLL LOCK status signal coming from LS serdes. When high, indicates LS Serdes PLL achieved lock to the selected incoming REFCLK0/1_P/N	RO/LL
30.22.12	RESERVED HS_PLL_LOCK_SYNC_LL (RXG)	For TI use only. HS Serdes PLL lock indicator. This LL signal is generated from sync'ed version of raw PLL LOCK status signal coming from HS serdes. When high, indicates HS Serdes PLL achieved lock to the selected incoming REFCLK0/1_P/N	
30.22.8	RESERVED RM_IDLE_COL_FOUND (G)	For TI use only. Applicable in 10G mode only. When HIGH, indicates 10g rate match FIFO has found IDLE column on its write side.	RO/LH
30.22.7	RESERVED HS_CH_SYNC_STATE[3] (X)	For TI use only. In 1GKX mode, [7] reflects bit 4 of HS sync state. Always reads 0 in 10GKR and 10G modes.	RO
30.22.6:4	HS_KR_CH_SYNC_ROT[6:4] HS_CH_SYNC_STATE[2:0] (RXG)	For TI use only. Channel synchronization pointer on HS side in 10GKR mode. Required for latency measurement function. See Latency Measurement function section for more details. In 10GKR mode, [6:4] reflects 3 MSB's of 7 bit HS sync rotation. Channel synchronization state on HS side in 1GKX and 10G modes. In 10G mode, [6:4] reflects 3 bit HS sync state. In 1GKX mode, [6:4] reflects 3 LSB's of 4 bit HS sync state.	

30.22.3:0	HS_KR_CH_SYNC_ROT[3:0] (RXG)	Channel synchronization pointer on HS side. Required for latency measurement function. See Latency Measurement function section for more details. In 10GKR mode, reflects 4 LSB's of 7 bit HS sync rotation. In 10G and 1GKX modes, reflects 4 bit HS sync rotation.	

Table 35: DST_CONTROL_1

Device Address: 0x1E	Register Address:0x0017	Default: 0x2000

Bit(s)	Name	Description	Access
30.23.15	RESERVED (RXG)	For TI use only (Default 1'b0)	RW
30.23.14	RESERVED (RXG)	For TI use only (Default 1'b0)	
30.23.13	RESERVED DST_FIFO_FLUSH_EN (RXG)	For TI use only (Default 1'b1) 1 = Enable auto FIFO flush through data switch on the transmit side 0 = Normal operation	
30.23.12	DST_PIN_SW_EN (RXG)	1 = Enable pin switch feature using top level pin. Ignore MDIO software switch. Requires setting PRTAD0_PIN_EN to high and setting PRTAD0_PIN_EN_SEL to control applicable channel Tx data switch. 0 = Disable pin switch feature. Only MDIO software switch is used (Default 1'b0)	
30.23.11:10	DST_PIN_SW_SRC_1[1:0] (RXG)	Applicable when top level pin (PRTAD0) is assigned to control transmit data-switch source input and if PRTAD0 is HIGH. 00 = Select same channel LS input(Default 2'b00) 01 = Select same channel HS input 10 = Select alternate channel LS input 11 = Select alternate channel HS output	
30.23.9:8	DST_PIN_SW_SRC_0[1:0] (RXG)	Applicable when top level pin (PRTAD0) is assigned to control transmit data-switch source input and if PRTAD0 is LOW. 00 = Select same channel LS input(Default 2'b00) 01 = Select same channel HS input 10 = Select alternate channel LS input 11 = Select alternate channel HS output	
30.23.7	DST_OFF_SEL (RX)	Applicable only in KR & KX modes. Selects data pattern to trigger ON condition (Default 1'b0)	

DST_ON_SEL	KR	KX
1	Local Fault (0x0100009c)	Match DST_OFF_CHAR specified in 30.32811
0	IDLE (0x07 on all lanes)	IDLE (Either /I1/ or /I2/)

30.23.6	DST_ON_SEL (RX)	Applicable only in KR & KX modes. Selects data pattern to trigger OFF condition (Default 1'b0)	

DST_OFF_SEL	KR	KX
1	Local Fault (0x0100009c)	Match DST_ON_CHAR specified in 30.32810
0	IDLE (0x07 on all lanes)	IDLE (Either /I1/ or /I2/)

30.23.5	DST_STUFF_SEL (RX)	Applicable only in KR & KX modes. Selects data pattern to stuff the output during data switching(Default 1'b0)	

DST_STUFF_SEL	KR	KX
1	Local Fault (0x0100009c)	/V/ Error propagation (K30.7)
0	IDLE (0x07 on all lanes)	/I2/ (/K28.5/D16.2/)

30.23.4:0	RESERVED DST_FORCE_SEL[4:0] (RXG)	For TI use only (Default 5'b00000) Manual data switch control. When DST_FORCE_SEL [4] is 1'b1, EN[3:0] value is equal to DST_FORCE_SEL [3:0] When DST_FORCE_SEL [4] is 1'b0, EN[3:0] value is set through data-switch control logic	

Table 36: DST_CONTROL_2

Device Address: 0x1E	Register Address:0x0018	Default: 0x0C20	
Bit(s)	**Name**	**Description**	**Access**
30.24.15:14	DST_DATA_SRC_SEL[1:0] (RXG)	Data selection for transmit data switch source input. Applicable when DST_PIN_SW_EN is LOW. 00 = Select same channel LS input(Default 2'b00) 01 = Select same channel HS input 10 = Select alternate channel LS input 11 = Select alternate channel HS output	RW
30.24.13:12	DST_DATA_SW_MODE[1:0] (RXG)	Selects condition to trigger data switch for the selected ON/OFF condition. (Default 2'b00)	
30.24.11:8	RESERVED DST_GAP[3:0] (RXG)	For TI use only (Default 4'b1100) Selects number of clock cycles of gap added during data switch. Recommended provision values are KR/KX modes : 2 10G mode : 6 If the gap is set to 0 or 1, the resultant gap still has 2 clock cycles	
30.24.7:0	DST_MASK_CYCLES[7:0] (RXG)	Duration of clock cycles that the data-switch output data is masked with the data pattern selected through DST_STUFF_SEL. (Default 8'b0010_0000)	

	OFF condition	ON condition
00	Wait for OFF trigger	Wait for ON trigger
01	Any data	Wait for ON trigger
10	Any data	Any data
11	Wait for OFF trigger	Any data

Table 37: DSR_CONTROL_1

Device Address: 0x1E	Register Address:0x0019	Default: 0x2500	
Bit(s)	**Name**	**Description**	**Access**
30.25.15	RESERVED (RXG)	For TI use only (Default 1'b0)	RW
30.25.14	RESERVED (RXG)	For TI use only (Default 1'b0)	
30.25.13	RESERVED DSR_FIFO_FLUSH_EN (RXG)	For TI use only (Default 1'b1) 1 = Enable auto FIFO flush through data switch on the receive side 0 = Normal operation	
30.25.12	DSR_PIN_SW_EN (RXG)	1 = Enable pin switch feature using top level pin. Ignore MDIO software switch. Requires setting PRTAD0_PIN_EN to high and setting PRTAD0_PIN_EN_SEL to control applicable channel Rx data switch. 0 = Disable pin switch feature. Only MDIO software switch is used (Default 1'b0)	

<table>
<tr><td>30.25.11:10</td><td>DSR_PIN_SW_SRC_1[1:0]
(RXG)</td><td>Applicable when top level pin (PRTAD0) is assigned to control receive data-switch source input and if PRTAD0 is HIGH.
00 = Select same channel LS input
01 = Select same channel HS input(Default 2’b01)
10 = Select alternate channel LS input
11 = Select alternate channel HS output</td><td></td></tr>
<tr><td>30.25.9:8</td><td>DSR_PIN_SW_SRC_0[1:0]
(RXG)</td><td>Applicable when top level pin (PRTAD0) is assigned to control receive data-switch source input and if PRTAD0 is LOW.
00 = Select same channel LS input
01 = Select same channel HS input(Default 2’b01)
10 = Select alternate channel LS input
11 = Select alternate channel HS output</td><td></td></tr>
<tr><td>30.25.7</td><td>DSR_OFF_SEL
(RX)</td><td>Applicable only in KR & KX modes. Selects data pattern to trigger OFF condition (Default 1’b0)
<table>
<tr><th>DSR_OFF_SEL</th><th>KR</th><th>KX</th></tr>
<tr><td>1</td><td>Local Fault
(0x0100009c)</td><td>Match DSR_OFF_CHAR specified in 30.32814</td></tr>
<tr><td>0</td><td>IDLE
(0x07 on all lanes)</td><td>IDLE
(Either /I1/ or /I2/)</td></tr>
</table></td><td></td></tr>
<tr><td>30.25.6</td><td>DSR_ON_SEL
(RX)</td><td>Applicable only in KR & KX modes. Selects data pattern to trigger ON condition (Default 1’b0)
<table>
<tr><th>DSR_ON_SEL</th><th>KR</th><th>KX</th></tr>
<tr><td>1</td><td>Local Fault
(0x0100009c)</td><td>Match DSR_ON_CHAR specified in 30.32813</td></tr>
<tr><td>0</td><td>IDLE
(0x07 on all lanes)</td><td>IDLE
(Either /I1/ or /I2/)</td></tr>
</table></td><td></td></tr>
<tr><td>30.25.5</td><td>DSR_STUFF_SEL
(RX)</td><td>Applicable only in KR & KX modes. Selects data pattern to stuff the output during data switching(Default 1’b0)
<table>
<tr><th>DSR_STUFF_SEL</th><th>KR</th><th>KX</th></tr>
<tr><td>1</td><td>Local Fault
(0x0100009c)</td><td>/V/ Error propagation
(K30.7)</td></tr>
<tr><td>0</td><td>IDLE
(0x07 on all lanes)</td><td>/I2/
(/K28.5/D16.2/)</td></tr>
</table></td><td></td></tr>
<tr><td>30.25.4:0</td><td>RESERVED
DSR_FORCE_SEL[4:0]
(RXG)</td><td>For TI use only (Default 5’b00000)
Manual data switch control.
When DSR_FORCE_SEL [4] is 1’b1, EN[3:0] value is equal to DSR_FORCE_SEL [3:0]
When DSR_FORCE_SEL [4] is 1’b0, EN[3:0] value is set through data-switch control logic</td><td></td></tr>
</table>

Table 38: DSR_CONTROL_2

<table>
<tr><th colspan="2">Device Address: 0x1E</th><th>Register Address:0x001A</th><th>Default: 0x4C20</th></tr>
<tr><th>Bit(s)</th><th>Name</th><th>Description</th><th>Access</th></tr>
<tr><td>30.26.15:14</td><td>DSR_DATA_SRC_SEL[1:0]
(RXG)</td><td>Data selection for receive data switch source input. Applicable when DST_PIN_SW_EN is LOW.
00 = Select same channel LS input
01 = Select same channel HS input(Default 2’b01)
10 = Select alternate channel LS input
11 = Select alternate channel HS output</td><td>RW</td></tr>
<tr><td>30.26.13:12</td><td>DSR_DATA_SW_MODE[1:0]
(RXG)</td><td>Selects condition to trigger data switch for the selected ON/OFF condition. (Default 2’b00)
<table>
<tr><th></th><th>OFF condition</th><th>ON condition</th></tr>
<tr><td>00</td><td>Wait for OFF trigger</td><td>Wait for ON trigger</td></tr>
<tr><td>01</td><td>Any data</td><td>Wait for ON trigger</td></tr>
<tr><td>10</td><td>Any data</td><td>Any data</td></tr>
<tr><td>11</td><td>Wait for OFF trigger</td><td>Any data</td></tr>
</table></td><td></td></tr>
</table>

30.26.11:8	RESERVED DSR_GAP [3:0] (RXG)	For TI use only (Default 4'b1100) Selects number of clock cycles of gap added during data switch. Recommended provision values are KR/KX modes : 2 10G 4 ln mode : 4 10G 2 ln mode : 6 10G 1 ln mode : 11 If the gap is set to 0 or 1, the resultant gap still has 2 clock cycles	
30.26.7:0	DSR_MASK_CYCLES[7:0] (RXG)	Duration of clock cycles that the data-switch output data is masked with the data pattern selected through DST_STUFF_SEL. (Default 8'b0010_0000)	

Table 39: DATA_SWITCH_STATUS

Device Address: 0x1E	Register Address:0x001B	Default: 0x1020	
Bit(s)	**Name**	**Description**	**Access**
30.27.15:12	DST_EN[3:0] (RXG)	Source input data selection status on transmit side. 0001 = Same channel LS data 0010 = Same channel HS data 0100 = Alternate channel LS data 1000 = Alternate channel HS data	RO
30.27.11	DST_SW_PENDING (RXG)	When HIGH, indicates data switching event is pending to be completed in the transmit side based on selected data source input	
30.27.10	DST_SW_DONE (RXG)	When HIGH, indicates data switching event has occurred in the transmit side based on selected data source input	RO/LH
30.27.9	DST_ON (RXG)	ON condition indicator from transmit data switch. When HIGH, indicates an ON condition has occurred in transmit data switch.	
30.27.8	DST_OFF (RXG)	OFF condition indicator from transmit data switch. When HIGH, indicates an OFF condition has occurred in transmit data switch.	
30.27.7:4	DSR_EN[3:0] (RXG)	Source input data selection status on receive side. 0001 = Same channel LS data 0010 = Same channel HS data 0100 = Alternate channel LS data 1000 = Alternate channel HS data	RO
30.27.3	DSR_SW_PENDING (RXG)	When HIGH, indicates data switching event is pending to be completed in the receive side based on selected data source input	
30.27.2	DSR_SW_DONE (RXG)	When HIGH, indicates data switching event has occurred in the receive side based on selected data source input	RO/LH
30.27.1	DSR_ON (RXG)	ON condition indicator from receive data switch. When HIGH, indicates an ON condition has occurred in receive data switch.	
30.27.0	DSR_OFF (RXG)	OFF condition indicator from receive data switch. When HIGH, indicates an OFF condition has occurred in receive data switch.	

Table 40: LS_CH_CONTROL_1

Device Address: 0x1E	Register Address:0x001C	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**

30.28.6	RESERVED LS_CHSYNC_JOG_PULSE (RG)	For TI use only (Default 1'b0) Applicable only if LS_CHSYNC_JOG_EN and LS_CHSYNC_FORCE_SYNC are 1 Lane can be selected in LS_SERDES_CONTROL_1. 0 = Normal operation (Default 1'b0) 1 = Moves current alignment by 1 bit	RW/SC
30.28.5	RESERVED LS_CHSYNC_FORCE_SYNC (RG)	For TI use only (Default 1'b0) Lane can be selected in LS_SERDES_CONTROL_1. 0 = Keep byte alignment determined by ch sync state machine (Default 1'b0) 1 = Force byte alignment to 9 unless LS_CHSYNC_JOG_EN is 1	RW
30.28.4	RESERVED LS_CHSYNC_JOG_EN (RG)	For TI use only (Default 1'b0) Lane can be selected in LS_SERDES_CONTROL_1. 0 = Disable manual jog function (Default 1'b0) 1 = Enable manual jog function	
30.28.3	RESERVED LS_ENC_BYPASS (RXG)	For TI use only (Default 1'b0) Lane can be selected in LS_SERDES_CONTROL_1. 1 = Bypass Encoder on LS side on selected lane. 0 = Bypass Encoder on LS side on selected lane (1'b0)	
30.28.2	RESERVED LS_DEC_BYPASS (RXG)	For TI use only (Default 1'b0) Lane can be selected in LS_SERDES_CONTROL_1. 1 = Bypass Decoder on LS side on selected lane. 0 = Bypass Decoder on LS side on selected lane (1'b0)	
30.28.1:0	LS_CH_SYNC_HYS_SEL[1:0] (RG)	LS Channel synchronization hysteresis selection for selected lane. Lane can be selected in LS_SERDES_CONTROL_1. 00 = The channel synchronization, when in the synchronization state, performs the Ethernet standard specified hysteresis to return to the LOS state (Default 2'b00) 01 = A single 8b/10b invalid decode error or disparity error causes the channel synchronization state machine to immediately transition from sync to LOS 10 = Two adjacent 8b/10b invalid decode errors or disparity errors cause the channel synchronization state machine to immediately transition from sync to LOS 11 = Three adjacent 8b/10b invalid decode errors or disparity errors cause the channel synchronization state machine to immediately transition from sync to LOS	

Table 41: HS_CH_CONTROL_1

Device Address: 0x1E	Register Address:0x001D	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.29.15	RESERVED IPG_MANAGER_BYPASS (R)	For TI use only (Default 1'b0) Applicable in 10GKR mode only 1 = Bypasses IPG manager on RX side (LS TX) 0 = Normal operation (Default 1'b0)	RW
30.29.14	RESERVED IPG_CHECKER_BYPASS (R)	For TI use only (Default 1'b0) Applicable in 10GKR mode only 1 = Bypasses IPG checker on TX side (LS RX) 0 = Normal operation (Default 1'b0)	
30.29.13	REFCLK_FREQ_SEL_1 (RX)	Input REFCLK frequency selection MSB. Applicable in 10GKR/1GKX modes only. When set, HS_PLL_MULT, LS_MPY and HS/LS TX/RX RATE settings can be set through related control bits specified in registers 30.2, 30.3, 30.6 0 = HS_PLL_MULT, LS_MPY and HS/LS TX/RX RATE are set automatically based on input REFCLK frequency as specified in REFCLK_FREQ_SEL_0(30.29.12) (Default 1'b0) 1 = Set this value if HS_PLL_MULT, LS_MPY and HS/LS TX/RX RATE values are NOT to be set automatically.	

30.29.12	REFCLK_FREQ_SEL_0 (RXG)	Input REFCLK frequency selection LSB. Applicable in 10GKR/1GKX modes only and when REFCLK_FREQ_SEL_1(30.29.13) is set to 1. 0 = Set this value if REFCLK frequency is 156.25 Mhz (Default 1'b0) 1 = Set this value if REFCLK frequency is 312.5 Mhz	
30.29.11	RX_CTC_BYPASS (RX)	Applicable in 10GKR, 1GKX modes only 0 = Normal operation. (Default 1'b0) 1 = Disables RX CTC operation.	
30.29.10	TX_CTC_BYPASS (RX)	Applicable in 10GKR, 1GKX modes only 0 = Normal operation. (Default 1'b0) 1 = Disables TX CTC operation.	
30.29.7	RESERVED HS_CHSYNC_FORCE_SYNC_DISABLE (G)	For TI use only (Default 1'b0) Applicable in 10G mode only. 0 = Enable forced sync of HS channel synchronization in 1ln mode 1 = Disable forced sync of HS channel synchronization in 1ln mode	RW
30.29.6	RESERVED HS_CHSYNC_JOG_PULSE (G)	For TI use only (Default 1'b0) Applicable only if HS_CHSYNC_JOG_EN and HS_CHSYNC_FORCE_SYNC are 1 0 = Normal operation (Default 1'b0) 1 = Moves current alignment by 1 bit	RW/SC
30.29.5	RESERVED HS_CHSYNC_FORCE_SYNC (G)	For TI use only (Default 1'b0) 0 = Keep byte alignment determined by ch sync state machine (Default 1'b0) 1 = Force byte alignment to 9 unless HS_CHSYNC_JOG_EN is 1	RW
30.29.4	RESERVED HS_CHSYNC_JOG_EN (G)	For TI use only (Default 1'b0) 0 = Disable manual jog function (Default 1'b0) 1 = Enable manual jog function	
30.29.3	HS_ENC_BYPASS (RXG)	0 = Normal operation. (Default 1'b0) 1 = Disables 8B/10B encoder on HS side.	
30.29.2	HS_DEC_BYPASS (RXG)	0 = Normal operation. (Default 1'b0) 1 = Disables 8B/10B decoder on HS side.	
30.29.1:0	HS_CH_SYNC_HYSTERESIS[1:0] (RXG)	Channel synchronization hysteresis control on the HS receive channel. 00 = The channel synchronization, when in the synchronization state, performs the Ethernet standard specified hysteresis to return to the unsynchronized state (Default 2'b00) 01 = A single 8b/10b invalid decode error or disparity error causes the channel synchronization state machine to immediately transition from sync to unsync 10 = Two adjacent 8b/10b invalid decode errors or disparity errors cause the channel synchronization state machine to immediately transition from sync to unsync 11 = Three adjacent 8b/10b invalid decode errors or disparity errors cause the channel synchronization state machine to immediately transition from sync to unsync	

Table 42: EXT_ADDRESS_CONTROL

Device Address: 0x1E	Register Address:0x001E	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.30.15:0	EXT_ADDR_CONTROL[15:0] (XG)	Applicable in Clause 22 mode only. This register should be written with the extended register address to be written/read. Contents of address written in this register can be accessed from Reg 31 (0x001F). (Default 16'h0000)	RW

Table 43: EXT_ADDRESS_DATA

Device Address: 0x1E	Register Address:0x001F	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**

30.31.15:0	EXT_ADDR_DATA[15:0] (XG)	Applicable in Clause 22 mode only. This register contains the data associated with the register address written in Register 30 (0x001E)	RW

Below registers can be accessed directly through Clause 45 and indirectly through Clause 22. Contains mode specific control/status registers and implemented per channel basis.

Table 44: TI_RESERVED_CONTROL(VS_10G_FIFO_CONTROL_1)

Device Address: 0x1E	Register Address: 0x8000	Default: 0x04C0	
Bit(s)	**Name**	**Description**	**Access**
30.32768.11	RESERVED RM_FIFO_CTC_BYPASS (G)	For TI use only (Default 1'b0) Applicable only when RATE_MATCH_FIFO_SEL = 1. 1 = Bypass CTC functionality in RATE MATCH FIFO 0 = CTC function enabled (1'b0)	RW
30.32768.10:8	RESERVED RM_FIFO_DEPTH_SEL[2:0] (G)	For TI use only (Default 3'b100) Applicable only when RATE_MATCH_FIFO_SEL = 1. Selects CTC FIFO depth. 1xx = 32 Deep (Default 3'b100) 011 = 24 deep 010 = 16 deep 001 = 12 deep 000 = 8 deep (no CTC)	
30.32768.7:6	RESERVED RM_FIFO_WMK_SEL[1:0] (G)	For TI use only (Default 2'b11) Applicable only when RATE_MATCH_FIFO_SEL = 1. Selects CTC low watermark setting. (Default 2'b11)	
30.32768.5	RESERVED RATE_MATCH_FIFO_SEL (G)	For TI use only (Default 1'b0) 1 = Selects rate match FIFO on RX side(Default 1'b0) 0 = Selects regular FIFO	

Depth ->	32	24	16	12/8
11	High	High	High	NA
10	Mid-high	Mid	High	
01	Mid	Low	Low	
00	Low	Low	Low	

Table 45: TI_RESERVED_CONTROL(VS_10G_RM_FIFO_SKIP_CHAR)

Device Address: 0x1E	Register Address: 0x8001	Default: 0x0207	
Bit(s)	**Name**	**Description**	**Access**
30.32769.9:0	RESERVED RM_FIFO_SKIP_CHAR[9:0] (G)	For TI use only (Default 10'h207) 10 bit word to be matched for insertion/deletion in Rate match FIFO (Default 10'h207)	RW

Table 46: TI_RESERVED_CONTROL(VS_10G_RM_FIFO_ERROR_CODE)

Device Address: 0x1E	Register Address: 0x8002	Default: 0x02FE	
Bit(s)	**Name**	**Description**	**Access**
30.32770.9:0	RESERVED RM_FIFO_ERROR_CODE[9:0] (G)	For TI use only (Default 10'h2FE) 10 bit word to be sent when LF or FIFO collision is detected in Rate match FIFO (Default 10'h2FE)	RW

Table 47: VS_10G_LN_ALIGN_ACODE_P

Device Address: 0x1E	Register Address: 0x8003	Default: 0x0283

Bit(s)	Name	Description	Access
30.32771.9:0	LN_ALIGN_ACODE_P[9:0] (G)	10 bit Alignment character to be matched (Default 10'h283)	RW

Table 48: VS_10G_LN_ALIGN_ACODE_N

Device Address: 0x1E	Register Address: 0x8004	Default: 0x017C	
Bit(s)	**Name**	**Description**	**Access**
30.32772.9:0	LN_ALIGN_ACODE_N[9:0] (G)	10 bit Alignment character to be matched (Default 10'h17C)	RW

Table 49: TI_RESERVED_CONTROL (VS_10G_LAS_REPLACE_CONTROL_1)

Device Address: 0x1E	Register Address: 0x8005	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.32773.14	RESERVED LAS_XAUI_SM_EN (G)	For TI use only (Default 1'b0) 0 = Normal operation (Default 1'b0) 1 = Make LAS lane align state machine XAUI compliant.	RW
30.32773.13:12	RESERVED LAS_MARKED_LANE[1:0] (G)	For TI use only (Default 1'b0) 00 = Marker insertion in lane 0 (Default 2'b00) 01 = Marker insertion in lane 1 10 = Marker insertion in lane 2 11 = Marker insertion in lane 3	
30.32773.9:0	RESERVED LAS_MARKER[9:0] (G)	For TI use only (Default 10'h000) 10 bit marker character to insert in place of LAS_REPLACE_CHAR character (Default 10'h000)	

Table 50: TI_RESERVED_CONTROL (VS_10G_LAS_REPLACE_CONTROL_2)

Device Address: 0x1E	Register Address: 0x8006	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.32774.15	RESERVED LAS_REPLACE_EN (G)	For TI use only (Default 1'b0) 0 = Disable character replacement (Default 1'b0) 1 = Enable character replacement by replacing LAS_REPLACE_CHAR with LAS_ MARKER	RW
30.32774.14:12	RESERVED LAS_REPLACE_FREQ[2:0] (G)	For TI use only (Default 3'b000) Frequency of char replacement 000 = Replace every LAS_REPLACE_CHAR (Default 3'b000) 001 = Replace every 4th LAS_REPLACE_CHAR 010 = Replace every 16th LAS_REPLACE_CHAR 011 = Replace every 64th LAS_REPLACE_CHAR 100 = Replace every 256th LAS_REPLACE_CHAR	
30.32774.9:0	RESERVED LAS_REPLACE_CHAR[9:0] (G)	10 bit character to be replaced by LAS_MARKER character (Default 10'h000)	

Table 51: TI_RESERVED_CONTROL (VS_10G_LAM_REPLACE_CONTROL_1)

Device Address: 0x1E	Register Address: 0x8007	Default: 0x8000	
Bit(s)	**Name**	**Description**	**Access**
30.32775.15	RESERVED RX_REORDER_BYPASS (G)	For TI use only (Default 1'b1) 0 = Normal operation 1 = Bypass Rx-reorder on LS (Default 1'b1)	RW
30.32775.14	RESERVED LAM_MANUAL_REORDER (G)	For TI use only (Default 1'b0) 0 = Detect marker and reorder (Default 1'b0) 1 = Ignore marker and reorder with LAM_JOG_SEL	
30.32775.13:12	RESERVED LAM_MARKED_LANE[1:0] (G)	For TI use only (Default 2'b00) 00 = Marker in lane 0 (Default 2'b00) 01 = Marker in lane 1 10 = Marker in lane 2 11 = Marker in lane 3	
30.32775.9:0	RESERVED LAM_MARKER[9:0] (G)	For TI use only (Default 10'h000) 10 bit marker character to match and replace (Default 10'h000)	

Table 52: TI_RESERVED_CONTROL (VS_10G_LAM_REPLACE_CONTROL_2)

Device Address: 0x1E	Register Address: 0x8008	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.32776.15	RESERVED LAM_JOG_PULSE (G)	For TI use only (Default 1'b0) 0 = Normal operation(Default 1'b0) 1 = Moves current alignment by 1 bit. Applicable only after LAM_JOG_SEL is set	RW/SC
30.32776.14	RESERVED LAM_REPLACE_EN (G)	For TI use only (Default 1'b0) 0 = Disable character replacement (Default 1'b0) 1 = Enable character replacement by replacing LAM_MARKER with LAM_REPLACE_CHAR	RW
30.32776.13	RESERVED LAM_SEND_A_EN (G)	For TI use only (Default 1'b0) 0 = K followed by lane align sequence in LA master (Default 1'b0) 1 = K, A followed by lane align sequence in LA master.	
30.32776.12	RESERVED LAM_JOG_SEL (G)	For TI use only (Default 1'b0) 0 = Use pin (LS_OK_IN) as jog control (Default 1'b0) 1 = Use LAM_JOG_PULSE as jog control	
30.32776.9:0	RESERVED LAM_REPLACE_CHAR[9:0] (G)	For TI use only (Default 10'h000) 10 bit character used to replace LAM_MARKER character (Default 10'h000)	

Table 53: TI_RESERVED_CONTROL (VS_10G_TX_SCR_CONTROL)

Device Address: 0x1E	Register Address: 0x8009	Default: 0xFC00	
Bit(s)	**Name**	**Description**	**Access**
30.32777.15:8	RESERVED TX_SCR_INIT_P3[7:0] (G)	For TI use only (Default 8'hFC) 8 bit pattern 3 to initialize selected 16 or 20 bit scrambler (Default 8'hFC)	RW
30.32777.7:6	RESERVED TX_SCR_FORCE_CTRL[1:0] (G)	For TI use only (Default 2'b00) 2 bit control input selected as scrambler input when TX_SCR_FORCE_DATA_EN is enabled	

30.32777.5	RESERVED TX_SCR_FORCE_DATA_EN (G)	For TI use only (Default 1'b0) 1 = When 20 bit scrambler is enabled, selects 20 bit data set through TX_SCR_SEED[20:1] as scrambler input. When 16 bit scrambler is enabled, selects 16 bit data set through TX_SCR_FORCE_DATA and 2 bit control set through TX_SCR_FORCE_CTRL as scrambler input 0 = Normal operation. Datapath data selected as scrambler input(Default 1'b0)	
30.32777.4	RESERVED TX_SCR_FORCE_1BIT_ERROR (G)	For TI use only (Default 1'b0) 1 = Enable error injection in scrambler 0 = Normal operation. No error injection. (Default 1'b0)	RW/SC
30.32777.3	RESERVED TX_SCR_PRBS_INVERT (G)	For TI use only (Default 1'b0) Valid only when core RPBS mode is enabled 1 = Inverts core PRBS pattern output 0 = Normal operation (Default 1'b0)	RW
30.32777.2	RESERVED TX_SCR_20_MODE (G)	For TI use only (Default 1'b0) Valid only when 20 bit scrambler is enabled through 30.32777.1 1 = Select core PRBS generation on transmit side. PRBS seed can be set through 30.32780 and 30.32781. For PRBS^{7} pattern, set TX_SCR_POLY[31:0] to 32'h0000_00C0 For PRBS^{23} pattern, set TX_SCR_POLY[31:0] to 32'h0084_0000 For PRBS^{31} pattern, set TX_SCR_POLY[31:0] to 32'h9000_0000 0 = Select self-synchronous scrambler on transmit side (Default 1'b0)	
30.32777.1	RESERVED TX_SCR_20_EN (G)	For TI use only (Default 1'b0) 1 = Enable 20 bit scrambler (post-encoder) on transmit side(Default 1'b0) 0 = Disable 20 bit scrambler (post-encoder) on transmit side	
30.32777.0	RESERVED TX_SCR_16_EN (G)	For TI use only (Default 1'b0) 1 = Enable 16 bit scrambler (pre-encoder) on transmit side. Seed can be set through 30.32780 and 30.32781 (Default 1'b0) 0 = Disable 16 bit scrambler (pre-encoder) on transmit side	

Table 54: TI_RESERVED_CONTROL (VS_10G_TX_SCR_PATT_CONTROL)

Device Address: 0x1E	Register Address: 0x800A	Default: 0xBC3C	
Bit(s)	**Name**	**Description**	**Access**
30.32778.15:8	RESERVED TX_SCR_INIT_P2[7:0] (G)	For TI use only (Default 8'hBC) 8 bit pattern 3 to initialize selected 16 or 20 bit scrambler (Default 8'hBC)	RW
30.32778.7:0	RESERVED TX_SCR_INIT_P1[7:0] (G)	For TI use only (Default 8'h3C) 8 bit pattern 3 to initialize selected 16 or 20 bit scrambler (Default 8'h3C)	

Table 55: TI_RESERVED_CONTROL (VS_10G_TX_SCR_FORCE_DATA)

Device Address: 0x1E	Register Address: 0x800B	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.32779.15:0	RESERVED TX_SCR_FORCE_DATA[15:0] (G)	For TI use only (Default 16'h0000) 15 data selected as scrambler input when TX_SCR_FORCE_DATA_EN is enabled	RW

Table 56: TI_RESERVED_CONTROL (VS_10G_TX_SCR_SEED_CONTROL_1)

Device Address: 0x1E	Register Address: 0x800C	Default: 0x0000

Bit(s)	Name	Description	Access
30.32780.15:0	RESERVED TX_SCR_SEED[31:16] (G)	For TI use only (Default 16'h0000) [31:16] bits of 32 bit Tx scrambler seed. TX_SCR_SEED[31:0] must be set to a non-zero value for scrambler to work properly (Default 16'h0000).	RW

Table 57: TI_RESERVED_CONTROL (VS_10G_TX_SCR_SEED_CONTROL_0)

Device Address: 0x1E	Register Address: 0x800D	Default: 0x01FC	
Bit(s)	**Name**	**Description**	**Access**
30.32781.15:0	RESERVED TX_SCR_SEED[15:0] (G)	For TI use only (Default 16'h01FC) [15:0] bits of 32 bit Tx scrambler seed. Bit 0 always set to 1'b0. TX_SCR_SEED[31:0] must be set to a non-zero value for scrambler to work properly (Default 16'h01FC).	RW

Table 58: TI_RESERVED_CONTROL (VS_10G_TX_SCR_POLY_CONTROL_1)

Device Address: 0x1E	Register Address: 0x800E	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.32782.15:0	RESERVED TX_SCR_POLY[31:16] (G)	For TI use only (Default 16'h0000) [31:16] bits of 32 bit Tx scrambler polynomial (Default 16'h0000).	RW

Table 59: TI_RESERVED_CONTROL (VS_10G_TX_SCR_POLY_CONTROL_0)

Device Address: 0x1E	Register Address: 0x800F	Default: 0x00C0	
Bit(s)	**Name**	**Description**	**Access**
30.32783.15:0	RESERVED TX_SCR_POLY[15:0] (G)	For TI use only (Default 16'h00C0) [15:0] bits of 32 bit Tx scrambler polynomial. Bit 0 always set to 1'b0. (Default 16'h00C0).	RW

Table 60: TI_RESERVED_CONTROL(VS_10G_LAM_HYSTERESIS)

Device Address: 0x1E	Register Address: 0x8011	Default: 0x7F00	
Bit(s)	**Name**	**Description**	**Access**
30.32785:15:8	RESERVED LAM_LS_HYSTERESIS[7:0] (G)	For TI use only. (Default 8'b0111_1111) Valid only in 10G mode. LS_OK_IN hysteresis counter value. LS_OK_IN* needs to be high at least this counter number of clock cycles for LAM to switch from lane align sequence to normal traffic LS_OK_IN* needs to be low at least this counter number of cycles for LAM to switch from normal traffic to lane align sequence. 8'b0000_0000 is invalid setting.	RW

Table 61: TI_RESERVED_STATUS(VS_10G_RX_CTC_DROP_COUNT)

Device Address: 0x1E	Register Address: 0x8012	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**

30.32786.15:0	RESERVED RX_CTC_DROP_COUNT (G)	For TI use only. Applicable in 10G mode and when Rate match FIFO is enabled. Counter for number of idle drops in the receive CTC.	COR

Table 62: TI_RESERVED_STATUS(VS_10G_RX_CTC_INSERT_COUNT)

Device Address: 0x1E	Register Address: 0x8013	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
30.32787.15:0	RESERVED RX_CTC_INS_COUNT (G)	For TI use only. Applicable in 10G mode and when Rate match FIFO is enabled. Counter for number of idle inserts in the receive CTC.	COR

Table 63: TI_RESERVED_STATUS(VS_10G_LS_MARKER_STATUS)

Device Address: 0x1E	Register Address:0x8014	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.32788.11	RESERVED LAM_REORDER_ERR (G)	For TI use only 1 = Marker position changed 0 = Marker position is same	RO/LH
30.32788.8	RESERVED LAM_MARKER_FOUND (G)	For TI use only 1 = Marker found on HS input 0 = Marker not found on HS input	
30.32788.4	RESERVED LAS_MARKER_INSERT (G)	For TI use only 1 = Marker inserted on designated lane 0 = Marker not inserted	
30.32788.3	RESERVED LAS_MARKER_FOUND_LN3 (G)	For TI use only 1 = Marker found on Lane 3 LS input 0 = Marker not found on Lane 3 LS input	
30.32788.2	RESERVED LAS_MARKER_FOUND_LN2 (G)	For TI use only 1 = Marker found on Lane 2 LS input 0 = Marker not found on Lane 2 LS input	
30.32788.1	RESERVED LAS_MARKER_FOUND_LN1 (G)	For TI use only 1 = Marker found on Lane 1 LS input 0 = Marker not found on Lane 1 LS input	
30.32788.0	RESERVED LAS_MARKER_FOUND_LN0 (G)	For TI use only 1 = Marker found on Lane 0 LS input 0 = Marker not found on Lane 0 LS input	

Table 64: TI_RESERVED_STATUS (LANE_ALIGN_STATUS_2)

Device Address: 0x1E	Register Address:0x8015	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.32789.15:12	RESERVED LN3_ALIGN_PTR[3:0] (RG)	For TI use only In 10GKR mode, consists of XAUI Lane align FIFO character location for lane 3. In 10G mode, consists of LAS Lane align FIFO character location for lane 3.	RO
30.32789.11:8	RESERVED LN2_ALIGN_PTR[3:0] (RG)	For TI use only In 10GKR mode, consists of XAUI Lane align FIFO character location for lane 2. In 10G mode, consists of LAS Lane align FIFO character location for lane 2.	
30.32789.7:4	RESERVED LN1_ALIGN_PTR[3:0] (RG)	For TI use only In 10GKR mode, consists of XAUI Lane align FIFO character location for lane 1. In 10G mode, consists of LAS Lane align FIFO character location for lane 1.	

30.32789.3:0	RESERVED LN0_ALIGN_PTR[3:0] (RG)	For TI use only In 10GKR mode, consists of XAUI Lane align FIFO character location for lane 0. In 10G mode, consists of LAS Lane align FIFO character location for lane 0.	

Table 65: TI_RESERVED_CONTROL (VS_10G_RX_DESCR_CONTROL)

Device Address: 0x1E	Register Address: 0x8019	Default: 0xFC00	
Bit(s)	**Name**	**Description**	**Access**
30.32793.15:8	RESERVED RX_DESCR_INIT_P3[7:0] (G)	For TI use only (Default 8'hFC) 8 bit pattern 3 to initialize selected 16 or 20 bit descrambler (Default 8'hFC)	RW
30.32793.3	RESERVED RX_DESCR_PRBS_INVERT (G)	For TI use only (Default 1'b0) Valid only when core RPBS mode is enabled 1 = Inverts core PRBS pattern input 0 = Normal operation (Default 1'b0)	
30.32793.2	RESERVED RX_DESCR_20_MODE (G)	For TI use only (Default 1'b0) Valid only when 20 bit descrambler is enabled through 30.32793.1 1 = Select core PRBS verification on receive side. For $PRBS^{7}$ pattern, set RX_DESCR_POLY[31:0] to 32'h0000_00C0 For $PRBS^{23}$ pattern, set RX_DESCR_POLY[31:0] to 32'h0084_0000 For $PRBS^{31}$ pattern, set RX_DESCR_POLY[31:0] to 32'h9000_0000 0 = Select self-synchronous descrambler on receive side (Default 1'b0)	
30.32793.1	RESERVED RX_DESCR_20_EN (G)	For TI use only (Default 1'b0) 1 = Enable 20 bit descrambler (pre-decoder) on receive side(Default 1'b0) 0 = Disable 20 bit descrambler (pre-decoder) on receive side	
30.32793.0	RESERVED RX_DESCR_16_EN (G)	For TI use only (Default 1'b0) 1 = Enable 16 bit descrambler (post-decoder) on receive side. Seed can be set through 30.32796 and 30.32797 (Default 1'b0) 0 = Disable 16 bit descrambler (post-decoder) on receive side	

Table 66: TI_RESERVED_CONTROL (VS_10G_RX_DESCR_PATT_CONTROL)

Device Address: 0x1E	Register Address: 0x801A	Default: 0xBC3C	
Bit(s)	**Name**	**Description**	**Access**
30.32794.15:8	RESERVED RX_DESCR_INIT_P2[7:0] (G)	For TI use only (Default 8'hBC) 8 bit pattern 3 to initialize selected 16 or 20 bit descrambler (Default 8'hBC)	RW
30.32794.7:0	RESERVED RX_DESCR_INIT_P1[7:0] (G)	For TI use only (Default 8'h3C) 8 bit pattern 3 to initialize selected 16 or 20 bit descrambler (Default 8'h3C)	

Table 67: TI_RESERVED_CONTROL (VS_10G_RX_DESCR_SEED_CONTROL_1)

Device Address: 0x1E	Register Address: 0x801C	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.32796.15:0	RESERVED RX_DESCR_SEED[31:16] (G)	For TI use only (Default 16'h0000) [31:16] bits of 32 bit Rx descrambler seed. RX_DESCR_SEED[31:0] must be set to a non-zero value for descrambler to work properly (Default 16'h0000).	RW

Table 68: TI_RESERVED_CONTROL (VS_10G_RX_DESCR_SEED_CONTROL_0)

Device Address: 0x1E	Register Address: 0x801D	Default: 0x01FC	
Bit(s)	**Name**	**Description**	**Access**
30.32797.15:0	RESERVED RX_DESCR_SEED[15:0] (G)	For TI use only (Default 16'h01FC) [15:0] bits of 32 bit Rx descrambler seed. Bit 0 always set to 1'b0. RX_DESCR_SEED[31:0] must be set to a non-zero value for descrambler to work properly (Default 16'h01FC).	RW

Table 69: TI_RESERVED_CONTROL (VS_10G_RX_DESCR_POLY_CONTROL_1)

Device Address: 0x1E	Register Address: 0x801E	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.32798.15:0	RESERVED RX_DESCR_POLY[31:16] (G)	For TI use only (Default 16'h0000) [31:16] bits of 32 bit Rx descrambler polynomial (Default 16'h0000).	RW

Table 70: TI_RESERVED_CONTROL (VS_10G_RX_DESCR_POLY_CONTROL_0)

Device Address: 0x1E	Register Address: 0x801F	Default: 0x00C0	
Bit(s)	**Name**	**Description**	**Access**
30.32799.15:0	RESERVED RX_DESCR_POLY[15:0] (G)	For TI use only (Default 16'h00C0) [15:0] bits of 32 bit Rx descrambler polynomial. Bit 0 always set to 1'b0. (Default 16'h00C0).	RW

Table 71: TI_RESERVED_CONTROL (VS_SERDES_CFG_OVERRIDE_CTRL)

Device Address: 0x1E	Register Address: 0x8020	Default: 0x0200	
Bit(s)	**Name**	**Description**	**Access**
30.32800.15	RESERVED LS_PLL_MULT_OVERRIDE (RXG)	For TI use only (Default 1'b0) Override PLL_MULT value going into Malfoy with MDIO configured value(Default 1'b0)	RW
30.32800.14	RESERVED LS_RATE_ OVERRIDE (RXG)	For TI use only (Default 1'b0) Override RATE value going into Malfoy with MDIO configured value(Default 1'b0)	
30.32800.13	RESERVED HS_PLL_MULT_OVERRIDE (RXG)	For TI use only (Default 1'b0) Override PLL_MULT value going into Copperfield with MDIO configured value(Default 1'b0)	RW
30.32800.12	RESERVED HS_RATE_OVERRIDE (RXG)	For TI use only (Default 1'b0) Override RATE value going into Copperfield with MDIO configured value(Default 1'b0)	
30.32800.10	RESERVED HS_BUSWIDTH_OVERRIDE (RXG)	For TI use only (Default 1'b0) Override BUSWIDTH value going into Copperfield with MDIO configured value(Default 1'b0)	
30.32800.9	RESERVED HS_FIRUPT_OVERRIDE (RXG)	For TI use only (Default 1'b1) Override FIRUPT value going into Copperfield with MDIO configured value(Default 1'b1)	

30.32800.8	RESERVED HS_ENRX_OVERRIDE (RXG)	For TI use only (Default 1'b0) Override ENRX value going into Copperfield with MDIO configured value(Default 1'b0)	
30.32800.7	RESERVED HS_AZCAL_OVERRIDE (RXG)	For TI use only (Default 1'b0) Override AZCAL value going into Copperfield with MDIO configured value(Default 1'b0)	
30.32800.6	RESERVED HS_ENTRACK_OVERRIDE (RXG)	For TI use only (Default 1'b0) Override ENTRACK value going into Copperfield with MDIO configured value(Default 1'b0)	
30.32800.5	RESERVED HS_EQHLD_OVERRIDE (RXG)	For TI use only (Default 1'b0) Override EQHLD value going into Copperfield with MDIO configured value(Default 1'b0)	
30.32800.4	RESERVED HS_TWCRF_OVERRIDE (RXG)	For TI use only (Default 1'b0) Override TWCRF value going into Copperfield with MDIO configured value(Default 1'b0)	
30.32800.3	RESERVED HS_TWPOST2_OVERRIDE (RXG)	For TI use only (Default 1'b0) Override TWPOST2 value going into Copperfield with MDIO configured value(Default 1'b0)	
30.32800.2	RESERVED HS_TWPOST_OVERRIDE (RXG)	For TI use only (Default 1'b0) Override TWPOST value going into Copperfield with MDIO configured value (Default 1'b0)	
30.32800.1	RESERVED HS_TWPRE_OVERRIDE (RXG)	For TI use only (Default 1'b0) Override TWPRE value going into Copperfield with MDIO configured value(Default 1'b0)	
30.32800.0	RESERVED HS_SWING_OVERRIDE (RXG)	For TI use only (Default 1'b0) Override SWING value going into Copperfield with MDIO configured value (Default 1'b0)	

Table 72: TI_RESERVED_CONTROL (MC_AUTO_CONTROL)

Device Address: 0x1E	Register Address:0x8021	Default: 0x000F	
Bit(s)	**Name**	**Description**	**Access**
30.32801.13	RESERVED HS_PK_DISABLE_OVERRIDE (RXG)	For TI use only (Default 1'b0) Override PEAK DISABLE value going into Copperfield with MDIO configured value(Default 1'b0)	RW
30.32801.12	RESERVED HS_H1CDRMODE_OVERRIDE (RXG)	For TI use only (Default 1'b0) Override H1CDRMODE value going into Copperfield with MDIO configured value(Default 1'b0)	
30.32801.11	RESERVED HS_CDRFMULT_OVERRIDE (RXG)	For TI use only (Default 1'b0) Override CDRFMULT value going into Copperfield with MDIO configured value(Default 1'b0)	
30.32801.10	RESERVED HS_CDRTHR_OVERRIDE (RXG)	For TI use only (Default 1'b0) Override CDRTHR value going into Copperfield with MDIO configured value(Default 1'b0)	
30.32801.9	RESERVED HS_AGCCTRL_OVERRIDE (RXG)	For TI use only (Default 1'b0) Override AGCCTRL value going into Copperfield with MDIO configured value(Default 1'b0)	
30.32801.8	RESERVED HS_EQPRE_OVERRIDE (RXG)	For TI use only (Default 1'b0) Override EQPRE value going into Copperfield with MDIO configured value(Default 1'b0)	
30.32801.7	RESERVED WATCHDOG_TIMER_EN (RXG)	For TI use only (Default 1'b0) 1 = Enable watchdog timer during 10GKR/1GKX/10G_MODE state in mode sequence SM 0 = Disable watchdog timer during 10GKR/1GKX/10G_MODE state in mode sequence SM	

30.32801.6	HS_PLL_LOCK_CHECK_DISABLE (RXG)	1 = Disable auto HS pll lock status check. 0 = Enable auto HS pll lock status check (Default 1'b0)	
30.32801.5	HS_LOS_CHECK_DISABLE (RXG)	1 = Disable auto HS los status check 0 = Enable auto HS los sync status check (Default 1'b0)	
30.32801.4	SYNC_STATUS_CHECK_DISABLE (RXG)	1 = Disable auto sync status check. 0 = Enable auto sync status check.	
30.32801.3	CLKOUT_EN_AUTO_DISABLE (RXG)	This bit controls the signal which flat lines CLKOUT and applicable only when CLKOUT is selected to have HS Recovered byte clock 1 = CLKOUT clock flat lined if HS LOS is detected (Default 1'b1) 0 = CLKOUT clock not flat lined if HS LOS is detected	
30.32801.2	RESERVED (RXG)	For TI use only (Default 1'b1)	
30.32801.1	RESERVED LT_CLK_ DISABLE (RXG)	For TI use only (Default 1'b1) 1 = Disable LT clock automatically upon link training completion 0 = Do not disable LT clock automatically upon link training completion	
30.32801.0	RESERVED ANEG_CLK_ DISABLE (RXG)	For TI use only (Default 1'b1) 1 = Disable AN clock automatically upon ANEG completion 0 = Do not disable AN clock automatically upon ANEG completion	

Table 73: TI_RESERVED_CONTROL (DP_RESET_TIMER)

Device Address: 0x1E	Register Address:0x8022	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.32802.15:0	RESERVED DP_RESET_TIMER[15:0] (RXG)	For TI use only (Default 16'h0000) Timer value for issuing Data path reset.	RW

Table 74: TI_RESERVED_CONTROL (AN_RESET_TIMER)

Device Address: 0x1E	Register Address:0x8023	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.32803.15:0	RESERVED AN_RESET_TIMER[15:0] (RXG)	For TI use only (Default 16'h0000) Timer value for issuing ANEG reset.	RW

Table 75: TI_RESERVED_CONTROL (LT_RESET_TIMER)

Device Address: 0x1E	Register Address:0x8024	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.32804.15:0	RESERVED LT_RESET_TIMER[15:0] (RXG)	For TI use only (Default 16'h0000) Timer value for issuing Link training reset.	RW

Table 76: TI_RESERVED_CONTROL (WATCHDOG_TIMER)

Device Address: 0x1E	Register Address:0x8025	Default: 0xF000

Bit(s)	Name	Description	Access
30.32805.15:0	RESERVED WATCHDOG_TIMER[15:0] (RXG)	For TI use only (Default 16'hF000) Watchdog timer value used to exit from respective 10G/10GKR/1GKX_MODE state in the mode control SM in case sync status is not achieved.	RW

Table 77: DST_ON_CHAR_CONTROL

Device Address: 0x1E	Register Address: 0x802A	Default: 0x02FD	
Bit(s)	**Name**	**Description**	**Access**
30.32810.9:0	DST_ON_CHAR[9:0] (XG)	Applicable only in 1GKX and 10G modes. 10 bit data pattern to trigger ON condition if matched on transmit side (Default 10'h2FD)	RW

Table 78: DST_OFF_CHAR_CONTROL

Device Address: 0x1E	Register Address: 0x802B	Default: 0x02FD	
Bit(s)	**Name**	**Description**	**Access**
30.32811.9:0	DST_OFF_CHAR[9:0] (XG)	Applicable only in 1GKX and 10G modes. 10 bit data pattern to trigger OFF condition if matched on transmit side (Default 10'h2FD)	RW

Table 79: DST_STUFF_CHAR_CONTROL

Device Address: 0x1E	Register Address: 0x802C	Default: 0x0207	
Bit(s)	**Name**	**Description**	**Access**
30.32812.9:0	DST_STUFF_CHAR[9:0] (G)	Applicable only in 10G mode. 10 bit data pattern to stuff the output of data switch on transmit side (Default 10'h207)	RW

Table 80: DSR_ON_CHAR_CONTROL

Device Address: 0x1E	Register Address: 0x802D	Default: 0x02FD	
Bit(s)	**Name**	**Description**	**Access**
30.32813.9:0	DSR_ON_CHAR[9:0] (XG)	Applicable only in 1GKX and 10G modes. 10 bit data pattern to trigger ON condition if matched on receive side (Default 10'h2FD)	RW

Table 81: DSR_OFF_CHAR_CONTROL

Device Address: 0x1E	Register Address: 0x802E	Default: 0x02FD	
Bit(s)	**Name**	**Description**	**Access**
30.32814.9:0	DSR_OFF_CHAR[9:0] (XG)	Applicable only in 1GKX and 10G modes. 10 bit data pattern to trigger OFF condition if matched on receive side (Default 10'h2FD)	RW

Table 82: DSR_STUFF_CHAR_CONTROL

Device Address: 0x1E	Register Address: 0x802F	Default: 0x0207	
Bit(s)	**Name**	**Description**	**Access**
30.32815.9:0	DSR_STUFF_CHAR[9:0] (G)	Applicable only in 10G mode. 10 bit data pattern to stuff the output of data switch on receive side (Default 10'h207)	RW

Table 83: TI_RESERVED_STATUS (MISC_SERDES_STATUS)

Device Address: 0x1E	Register Address:0x8030	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.32816.13	RESERVED HS_ ADCGAINX2 STSRX[11] (RXG)	For TI use only. HS Serdes ADCGAINX2 setting status.	RO
30.32816.12	RESERVED HS_ ATTENUATOR STSRX[10] (RXG)	For TI use only. HS Serdes attenuator setting status.	
30.32816.11:9	RESERVED HS_RSVD_STATUS[2:0] STSRX[7:5] (RXG)	For TI use only. HS Serdes reserved status.	
30.32816.8	RESERVED HS_JOGSYNC STSRX[1] (RXG)	For TI use only. HS Serdes Jog sync indicator. When high, indicates comma alignment is achieved if comma detection is enabled.	
30.32816.7:4	RESERVED LS_ODDCG[3:0] (RXG)	For TI use only. LS Serdes Odd code group indicator [3] for Lane 3, [2] for Lane 2, [1] for Lane 1, [0] for Lane 0	
30.32816.3:0	RESERVED LS_SYNC[3:0] (RXG)	For TI use only. LS Serdes sync indicator [3] for Lane 3, [2] for Lane 2, [1] for Lane 1, [0] for Lane 0	

Table 84: TI_RESERVED_STATUS(VS_HS_SERDES_STATUS_1)

Device Address: 0x1E	Register Address:0x8031	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.32817.15:14	RESERVED HS_FINAL_AZCAL[1:0] (RXG)	For TI use only Final HS Serdes AZCAL control	RO
30.32817.13	RESERVED HS_FINAL_FIRUPT (RXG)	For TI use only Final HS Serdes Tx pre/post cursor filter update control	
30.32817.12:8	RESERVED HS_ FINAL_TWPOST1[4:0] (RXG)	For TI use only Final Adjacent post cursor1 Tap weight. Selects TAP settings for TX waveform.	
30.32817.7:4	RESERVED HS_ FINAL_TWPRE[3:0] (RXG)	For TI use only Final Pre cursor Tap weight. Selects TAP settings for TX waveform	
30.32817.3:0	RESERVED HS_ FINAL_TWPOST2[3:0] (RXG)	For TI use only Final Adjacent post cursor2 Tap weight. Selects TAP settings for TX waveform.	

Table 85: TI_RESERVED_STATUS(VS_HS_SERDES_STATUS_2)

Device Address: 0x1E	Register Address:0x8032	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.32818.11	RESERVED HS_ FINAL_ENRX (RXG)	For TI use only Final HS Serdes enable rx control value	RO
30.32818.10	RESERVED HS_ FINAL_ENTRACK (RXG)	For TI use only Final HS Serdes entrack value	
30.32818.9	RESERVED HS_ FINAL_EQHLD (RXG)	For TI use only Final HS Serdes EQHLD value	
30.32818.8:4	RESERVED HS_FINAL_TWCRF[4:0] (RXG)	For TI use only Final cursor reduction factor weights value.	
30.32818.3:0	RESERVED HS_ FINAL_SWING[3:0] (RXG)	For TI use only Final Swing control value.	

Table 86: TI_RESERVED_STATUS(VS_HS_SERDES_STATUS_3)

Device Address: 0x1E	Register Address:0x8033	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.32819.11:10	RESERVED HS_ FINAL_BUSWIDTH[1:0] (RXG)	For TI use only Final HS Serdes BUSWIDTH value	RO
30.32819.9:8	RESERVED HS_FINAL_RATE_TX[1:0] (RXG)	For TI use only Final HS Serdes TX RATE value	
30.32819.6:4	RESERVED HS_FINAL_RATE_RX[2:0] (RXG)	For TI use only Final HS Serdes RX RATE value.	
30.32819.3:0	RESERVED HS_ FINAL_PLL_MULT[3:0] (RXG)	For TI use only Final HS Serdes PLL Multiplier control value.	

Table 87: TI_RESERVED_STATUS(VS_LS_SERDES_STATUS)

Device Address: 0x1E	Register Address:0x8034	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.32820.9:8	RESERVED LS_FINAL_RATE_TX[1:0] (RXG)	For TI use only Final LS Serdes TX RATE value	RO
30.32820.5:4	RESERVED LS_FINAL_RATE_RX[1:0] (RXG)	For TI use only Final LS Serdes RX RATE value.	
30.32820.3:0	RESERVED LS_ FINAL_PLL_MULT[3:0] (RXG)	For TI use only Final LS Serdes PLL Multiplier control value.	

Table 88: TI_RESERVED_STATUS(MC_STATUS)

Device Address: 0x1E	Register Address:0x8035	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.32821.7	RESERVED MC_10GKR_LINK_STATUS (R)	For TI use only MC 10GKR link status.	RO
30.32821.6	RESERVED MC_1GKX_LINK_STATUS (X)	For TI use only MC 1GKX link status.	
30.32821.5	RESERVED MC_10G_LINK_STATUS (G)	For TI use only MC 10G link status.	
30.32821.4	RESERVED MC_LINK_STATUS (RXG)	For TI use only MC output link status.	
30.32821.3:0	RESERVED MC_STATE[3:0] (RXG)	For TI use only Mode sequence state.	

Table 89: LATENCY_MEASURE_CONTROL[5]

Device Address: 0x1E	Register Address:0x8040	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.32832.7:6	LATENCY_MEAS_STOP_SEL[1:0] (RXG)	Latency measurement stop point selection 00 = Selects LS RX as stop point (Default 2 'b00) 01 = Selects HS TX as stop point 1x = Selects external pin (PRTAD0) as stop point	RW
30.32832.5:4	LATENCY_MEAS_CLK_DIV[1:0] (RXG)	Latency measurement clock divide control. Valid only when bit 30.32832.2 is 0. Divides clock to needed resolution. Higher the divide value, lesser the latency measurement resolution. Divider value should be chosen such that the divided clock doesn't result in clock slower than the high speed byte clock. 00 = Divide by 1 (Default 2'b00) (Most Accurate Measurement) 01 = Divide by 2 10 = Divide by 4 11 = Divide by 8 (Longest Measurement Capability)	
30.32832.3:2	LATENCY_MEAS_START_SEL[1:0] (RXG)	Latency measurement start point selection 00 = Selects LS TX as start point (Default 2'b00) 01 = Selects HS RX as start point 1x = Selects external pin (PRTAD0) as start point	
30.32832.1	LATENCY_MEAS_EN (RXG)	Latency measurement enable 0 = Disable Latency measurement (Default 'b0) 1 = Enable Latency measurement	
30.32832.0	LATENCY_MEAS_CLK_SEL (RXG)	Latency measurement clock selection. 0 = Selects VCO clock as per Latency measurement table. Bits 30.32832.5:4 can be used to divide this clock to achieve needed resolution. (Default 1'b0) 1 = Selects respective channel recovered byte clock	

Table 90: LATENCY_COUNTER_2

Device Address: 0x1E	Register Address:0x8041	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**

[5] See Latency measurement procedure for more information

30.32833.15:12	LATENCY_MEAS_START_COMMA[3:0] (RXG)	Latency measurement start comma location status. “1” indicates start comma location found. If LS TX is selected as start point (30.32832.7 = 0), [3:0] indicates status for lane3, lane2, lane1, lane0. If HS RX is selected as start point (30.32832.7 = 1), [0] indicates status for data[9:0], [1] indicates status for data[19:10]. [3:2] is unused. Reading this register will clear Latency stopwatch status specified in LATENCY_COUNTER_1 & LATENCY_COUNTER_2 registers. Below sequence of reads needs to be performed for accurate and repeat stopwatch measurements. See Latency measurement procedure more information. READ 0x8041 READ 0x8042	RO/LH[6]
30.32833.11:8	LATENCY_MEAS_STOP_COMMA[3:0] (RXG)	Latency measurement stop comma location status. “1” indicates stop comma location found. If LS RX is selected as stop point (30.32832.6 = 0), [3:0] indicates status for lane3, lane2, lane1, lane0. If HS TX is selected as stop point (30.32832.6 = 1), [0] indicates status for data[9:0], [1] indicates status for data[19:10]. [3:2] is unused.	
30.32833.4	LATENCY_ MEAS_READY (RXG)	Latency measurement ready indicator 0 = Indicates latency measurement not complete. 1 = Indicates latency measurement is complete and value in latency measurement counter (LATENCY_MEAS_COUNT[19:0]) is ready to be read.	
30.32833.3:0	LATENCY_MEAS_COUNT[19:16] (RXG)	Bits[19:16] of 20 bit wide latency measurement counter. Latency measurement counter value represents the latency in number of clock cycles. Each clock cycle is half of the period of the measurement clock as determined by register 30.32832.5:4 and 30.32832.0. This counter will return 20’h00000 if it’s read before rx comma is received. If latency is more than 20’hFFFFF clock cycles then this counter returns 20’hFFFFF.	COR[6]

Table 91: LATENCY_COUNTER_1

Device Address: 0x1E	Register Address:0x8042	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.32834.15:0	LATENCY_MEAS_COUNT[15:0] (RXG)	Bits[15:0] of 20 bit wide latency measurement counter. Below sequence of reads needs to be performed for accurate and repeat stopwatch measurements. READ 0x8041 READ 0x8042	COR[6]

Table 92: TI_RESERVED_CONTROL (MISC_DEBUG_CONTROL)

Device Address: 0x1E	Register Address:0x8050	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**

[6] Latency measurement counter value resets to 20’h00000 when this register is read. Start and Stop Comma (30.32833.15:12 & 30.32833.11:8) and count valid (30.32833.4) bits are also cleared when this register is read

30.32848.3:0	RESERVED CH_DEBUG_SEL[3:0] (RXG)	For TI use only (Default 4'b0000) Debug Mux selection. Applicable only when 30.40960.4 (TOP_DEBUG_MUX_EN) is set. Selected signals sent out on {LOSB, LS_OK_OUT_B, LOSA, LS_OK_OUT_A}. Channel can be selected through 30.40960.5 (TOP_DEBUG_SEL) 0000 = {2'b00, los_overlay, ls_ok_out} 0001 = {qol_data_odd, qol_data_even, qol_strobe, qol_div2_clk} 0010 = {mc_seq_state} 0011 = {kx_invalid_char_ls_in, kx_invalid_char_ls_in,10g_rx_dec_err, 10g_tx_enc_err } 0100 = {kr_tp_err_live, kr_tp_state} 0101 = {1'b0, kr_rx_dec_state} 0110 = {kr_corr_err, kr_uncorr_err, kr_rx_dec_err, kr_tx_enc_err} 0111 = {kr_tx_xla_status, kr_tx_xla_state} 1000 = {ctc_ins_rx_1gkx, ctc_del_rx_1gkx, ctc_ins_tx_1gkx, ctc_del_tx_1gkx} 1001 = {ls_ln_decode_err[3:0]} 1010 = {dst_en_status} 1011 = {dsr_en_status} 1100 = {2'b00, tx_cl73_state} 1101 = {arb_state } 1110 = {1'b0, sm_train_state} 1111 = {at_state[3:0]} PRBS_PASS reflects AT_STATE[4] when 30.40960.4 (TOP_DEBUG_MUX_EN) is set and CH_DEBUG_SEL[3:0] is 4'b1111. All other selections reflect PRBS verification status as per 30.0.4:0 (PRBS_PASS_OVERLAY[4:0])	RW

Table 93: TRIGGER_LOAD_CONTROL

Device Address: 0x1E	Register Address:0x8100	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.33024.10:3	RESERVED MC_SM_OVERRIDE[10:3] (RXG)	For TI use only (Default 8'b00000000) Override controls for MC Sequence SM. 1 = Enable override value specified in MC_SM_OVERRIDE_VALUE (30.33025[10:3]) for respective bit 0 = Normal operation [3] – MC mode_10g override control [4] – MC mode_1gkx override control [5] – MC mode_10gkr override control [6] – MC mode_lt override control [7] – MC mode_aneg override control [8] – MC link status override control [9] – MC disable aneg clk override control [10] – MC disable lt clk override control	RW
30.33024.2	DEFAULT_TX_LOAD_TRIGGER (RXG)	Valid only when DEFAULT_TX_TRIGGER_EN is HIGH 1 = Trigger loading default HS TX setting values 0 = Normal operation (Default 1'b0) This bit needs to be written HIGH and then LOW to load the HS Tx default values. Applicable when Link training is enabled.	

30.33024.10:0	RESERVED MC_SM_OVERRIDE[1:0] (RXG)	For TI use only (Default 2'b00) Override controls for MC Sequence SM. 1 = Enable override value specified in MC_SM_OVERRIDE_VALUE (30.33025[1:0]) for respective bit 0 = Normal operation [0] – MC hw dp reset override control [1] – MC hw aneg reset override control	

Table 94: TRIGGER_EN_CONTROL

Device Address: 0x1E	Register Address:0x8101	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.33025.10:3	RESERVED MC_SM_OVERRIDE_VAL[10:3] (RXG)	For TI use only (Default 11'b000000000000) Override controls for MC Sequence SM. Applicable only if respective control bit in MC_SM_OVERRIDE[10:8] is set [0] – MC hw dp reset override value [1] – MC hw aneg reset override value [2] – MC hw lt reset override value [3] – MC mode_10g override value [4] – MC mode_1gkx override value [5] – MC mode_10gkr override value [6] – MC mode_lt override value [7] – MC mode_aneg override value [8] – MC link status override value [9] – MC disable aneg clk override value [10] – MC disable lt clk override value	RW
30.33025.2	DEFAULT_TX_TRIGGER_EN (RXG)	1 = Enable loading of Tx default values through DEFAULT_TX_LOAD_TRIGGER 0 = Normal operation (Default 1'b0)	
30.33025.1:0	RESERVED MC_SM_OVERRIDE_VAL[1:0] (RXG)	For TI use only (Default 2'b00) Override controls for MC Sequence SM. Applicable only if respective control bit in MC_SM_OVERRIDE[1:0] is set [0] – MC hw dp reset override value [1] – MC hw aneg reset override value	

Table 95: TI_RESERVED_CONTROL (DEEP_LOCAL_LPBK_HS_CONTROL)

Device Address: 0x1E	Register Address:0x8102	Default: 0xF280	
Bit(s)	**Name**	**Description**	**Access**
30.33026.15	RESERVED DEEP_LOC_LPBK_HS_EN (RXG)	For TI use only (Default 1'b1) HS Serdes value control during deep local loopback mode. 1 = Set HS serdes control values specified in 30.33026.14:0 as default when deep local loopback is enabled 0 = HS serdes control values are set through link training (if enabled) or through HS_SERDES_CONTROL_1/2 registers	RW
30.33026.14:12	RESERVED DEEP_LOC_HS_EQPRE[2:0] (RXG)	For TI use only (Default 3'b111) Applicable when DEEP_LOC_LPBK_HS_EN is set. Consists of HS EQPRE value during Deep local loopback.	
30.33026.11:10	RESERVED DEEP_LOC_HS_CDRFMULT[1:0] (RXG)	For TI use only (Default 2'b00) Applicable when DEEP_LOC_LPBK_HS_EN is set. Consists of HS CDRFMULT value during Deep local loopback.	
30.33026.9:8	RESERVED DEEP_LOC_HS_CDRTHR[1:0] (RXG)	For TI use only (Default 2'b10) Applicable when DEEP_LOC_LPBK_HS_EN is set. Consists of HS CDRTHR value during Deep local loopback.	

30.33026.7:6	RESERVED DEEP_LOC_HS_AGCCTRL[1:0] (RXG)	For TI use only (Default 2'b10) Applicable when DEEP_LOC_LPBK_HS_EN is set. Consists of HS AGCCTRL value during Deep local loopback.	
30.33026.5	RESERVED DEEP_LOC_HS_ENTRACK (RXG)	For TI use only (Default 1'b0) Applicable when DEEP_LOC_LPBK_HS_EN is set. Consists of HS ENTRACK value during Deep local loopback.	
30.33026.4	RESERVED DEEP_LOC_HS_H1CDRMODE (RXG)	For TI use only (Default 1'b0) Applicable when DEEP_LOC_LPBK_HS_EN is set. Consists of HS H1CDRMODE value during Deep local loopback.	
30.33026.3	RESERVED DEEP_LOC_PK_DISABLE (RXG)	For TI use only (Default 1'b0) Applicable when DEEP_LOC_LPBK_HS_EN is set. Consists of PK DISABLE value during Deep local loopback.	
30.33026.2	RESERVED DEEP_LOC_EQHLD (RXG)	For TI use only (Default 1'b0) Applicable when DEEP_LOC_LPBK_HS_EN is set. Consists of EQHLD value during Deep local loopback.	
30.33026.1:0	RESERVED DEEP_LOC_HS_AZCAL[1:0] (RXG)	For TI use only (Default 2'b00) Applicable when DEEP_LOC_LPBK_HS_EN is set. Consists of HS AZCAL value during Deep local loopback.	

Below registers can be accessed directly through Clause 45 and indirectly through Clause 22. Contains device specific debug control/status registers and not implemented per channel basis (i.e. same physical register accessed irrespective of channel addressed)

Table 96: TI_RESERVED_CONTROL (MISC_CONTROL)

Device Address: 0x1E	Register Address:0xA000	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.40960.11:8	RESERVED DEBUG_SPARE[3:0] (RXG)	For TI use only. (Default 4'b0000) Reserved spare control bits. For future debug purpose if required.	RW
30.40960.5	RESERVED TOP_DEBUG_SEL (RXG)	For TI use only. (Default 1'b0) Debug select bits to select internal status signals to be reflected on PRBS_PASS, LS_OK_OUT_* and LOS* pins. Valid only when TOP_DEBUG_MUX_EN is 1. 0 = PRBS_PASS, LS_OK_OUT_A/B and LOSA/B reflect status from Channel A 1 = PRBS_PASS, LS_OK_OUT_A/B and LOSA/B reflect status from Channel B	
30.40960.4	RESERVED TOP_DEBUG_MUX_EN (RXG)	For TI use only. (Default 1'b0) 0 = PRBS_PASS, LS_OK_OUT and LOS pins do not reflect internal debug status signals. 1 = Enable internal debug status signals to be reflected on PRBS_PASS, LS_OK_OUT and LOS pins	
30.40960.0	RESERVED EFUSE_AL_EN (RXG)	For TI use only. (Default 1'b0) When set, Re-enables EFUSE Auto load function. Needs to set back to LOW to complete Auto load function.	

Table 97: TI_RESERVED_STATUS (DIE_ID_7)

Device Address: 0x1E	Register Address: 0xA010	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.40976.15:0	RESERVED DIE_ID[127:112] (RXG)	For TI use only. Bits [127:112] of the Die ID. Unique TI DIE identifier.	RO

Table 98: TI_RESERVED_STATUS (DIE_ID_6)

Device Address: 0x1E	Register Address: 0xA011	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.40977.15:0	RESERVED DIE_ID[111:96] (RXG)	For TI use only. Bits [111:96] of the Die ID. Unique TI DIE identifier.	RO

Table 99: TI_RESERVED_STATUS (DIE_ID_5)

Device Address: 0x1E	Register Address: 0xA012	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**

30.40978.15:0	RESERVED DIE_ID[95:80] (RXG)	For TI use only. Bits [95:80] of the Die ID. Unique TI DIE identifier.	RO

Table 100: TI_RESERVED_STATUS (DIE_ID_4)

Device Address: 0x1E	Register Address: 0xA013	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.40979.15:0	RESERVED DIE_ID[79:64] (RXG)	For TI use only. Bits [79:64] of the Die ID. Unique TI DIE identifier.	RO

Table 101: TI_RESERVED_STATUS (DIE_ID_3)

Device Address: 0x1E	Register Address: 0xA014	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.40980.15:0	RESERVED DIE_ID[63:48] (RXG)	For TI use only. Bits [63:48] of the Die ID. Unique TI DIE identifier.	RO

Table 102: TI_RESERVED_STATUS (DIE_ID_2)

Device Address: 0x1E	Register Address: 0xA015	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.40981.15:0	RESERVED DIE_ID[47:32] (RXG)	For TI use only. Bits [47:32] of the Die ID. Unique TI DIE identifier.	RO

Table 103: TI_RESERVED_STATUS (DIE_ID_1)

Device Address: 0x1E	Register Address: 0xA016	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.40982.15:0	RESERVED DIE_ID[31:16] (RXG)	For TI use only. Bits [31:16] of the Die ID. Unique TI DIE identifier.	RO

Table 104: TI_RESERVED_STATUS (DIE_ID_0)

Device Address: 0x1E	Register Address: 0xA017	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.40983.15:0	RESERVED DIE_ID[15:0] (RXG)	For TI use only. Bits [15:0] of the Die ID. Unique TI DIE identifier.	RO

Table 105: TI_RESERVED_STATUS (MISC_STATUS)

Device Address: 0x1E	Register Address: 0xA018	Default: 0x0000

Bit(s)	Name	Description	Access
30.40984.9	RESERVED EFC_READY (RXG)	For TI use only. When high, indicates that EFUSE autoload operation has completed	RO
30.40984.8:4	RESERVED EFUSE_ERROR[4:0] (RXG)	For TI use only. Efuse error bus. Updated when EFC_READY goes high or when instruction is complete. Non-zero value indicates error condition.	
30.40984.3:0	RESERVED DEVICE_REV_ID[3:0] (RXG)	For TI use only. 4 bit device revision identifier.	

Table 106: TI_RESERVED_CONTROL (STCI_CFG_CONTROL)

Device Address: 0x01	Register Address:0xA116	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.41238.9	RESERVED STCI_CHAIN_CFG (RXG)	For TI use only. (Default 1'b0) Selects how the STCI chain is connected between 2 macros for the macro type selected through STCI_MAC_CFG 0 = STCI connected in parallel (All macros can be configured simultaneously) 1 = STCI connected serially (Macro A -> Macro B)	RW
30.41238.8	RESERVED STCI_MAC_CFG (RXG)	For TI use only. (Default 1'b0) Selects which macro to be accessed. 0 = Malfoy 1 = Copperfield	
30.41238.6	RESERVED STCI_CLK_ENABLE (RXG)	For TI use only. (Default 1'b0) STCI clock control in functional mode 0 = Disable STCI clock 1 = Enable STCI clock	
30.41238.5:4	RESERVED STCI_CFG[1:0] (RXG)	For TI use only. (Default 2'b00) STCI CFG control 0x = Reset STCI interface 10 = Shift 11 = Update/Capture Writing 10 to this register bits does not actually cause shifting of the STCI chain until writing to the register STCI_D occurs. Writing 11 to this register generates a rising edge on the SERDES STCICLK along with a 2'b11 on the SERDES STCICFG[1:0] port	
30.41238.3:0	RESERVED STCI_SHIFT_COUNT[3:0] (RXG)	For TI use only. The number of shifts performed on the register STCI_D and STCI_Q. 4'b0000 value results in shifting all 16 bits specified in registers STCI_D and STCI_Q (Default 4'b0000)	

Table 107: TI_RESERVED_CONTROL (STCI_D_CONTROL)

Device Address: 0x1E	Register Address:0xA117	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.41239.15:0	RESERVED STCI_D[15:0] (RXG)	For TI use only. Writing to this register causes the STCI_D[15:0] to be shifted into the SERDES STCI chain, LSB first, until the number of bits shifted equals to the value of STCI_SHIFT_COUNT[3:0] in the STCI_CFG_CONTROL register. The data shifted out of the SERDES STCI chain is stored in the register STCI_Q. Reading of this register returns the value of the register, and does not cause the STCI chain to be shifted. (Default 16'h0000)	RW

Table 108: (STCI_QA_STATUS)

Device Address: 0x01	Register Address:0xA118	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.41240.15:0	RESERVED STCI_QA[15:0] (RXG)	For TI use only. This register consists of the data shifted out of the Channel A STCI chain of SERDES macro selected through STCI_MAC_CFG. Writing to this register has no effect. Reading this register returns the bits shifted out of the SERDES STCI chain from the last shifting operation. The number of bits valid equals to the value of STCI_SHIFT_COUNT[3:0] in the STCI_CFG_CONTROL register. The first bit shifted out of the SERDES STCI chain is stored at the LSB of this register and the last bit shifted out is always stored at the MSB of this register (STCI_QA[0]). For example, if there are 14 bits shifted out, the first bit shifted out of the SERDES STCI chain is stored at STCI_QA[0], and the last bit is stored at STCI_QA[13].	RO

Table 109: (STCI_QB_STATUS)

Device Address: 0x01	Register Address:0xA119	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
30.41241.15:0	RESERVED STCI_QB[15:0] (RXG)	For TI use only. This register consists of the data shifted out of the Channel A STCI chain of SERDES macro selected through STCI_MAC_CFG. Writing to this register has no effect. Reading this register returns the bits shifted out of the SERDES STCI chain from the last shifting operation. The number of bits valid equals to the value of STCI_SHIFT_COUNT[3:0] in the STCI_CFG_CONTROL register. The first bit shifted out of the SERDES STCI chain is stored at the LSB of this register and the last bit shifted out is always stored at the MSB of this register (STCI_QA[0]). For example, if there are 14 bits shifted out, the first bit shifted out of the SERDES STCI chain is stored at STCI_QA[0], and the last bit is stored at STCI_QA[13].	RO

PMA/PMD REGISTERS

Below registers (except link training related) can be accessed only in Clause 45 mode and with device address field set to 0x01 (DA[4:0] = 5'b00001).

NOTE: Link training registers can also be accessed in Clause 22 mode using indirect address method and in Clause 45 mode with device address field set to 0x1E (DA[4:0] = 5'b11110). Link training registers are also applicable in 10G and 1GKX modes.

Table 110: PMA_CONTROL_1

Device Address: 0x01	Register Address: 0x0000	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
1.0.15	RESET (RX)	1 = Global reset. Resets datapath and MDIO registers of all channels. Equivalent to asserting RESET_N. 0 = Normal operation (Default 1'b0)	RW/SC[7]
1.0.11	POWERDOWN (RX)	1 = Enable power down mode 0 = Normal operation (Default 1'b0)	RW
1.0.0	LOOPBACK (RX)	1 = Enables loopback on HS side. LS data traverses through entire Tx datapath excluding HS serdes and will be available at LS output side Same as shallow local loopback. 0 = Normal operation (Default 1'b0)	RW

Table 111: PMA_STATUS_1

Device Address: 0x01	Register Address: 0x0001	Default: 0x0002	
Bit(s)	**Name**	**Description**	**Access**
1.1.7	FAULT (RX)	1 = Fault condition detected on either Tx or Rx side 0 = No fault condition detected This bit is cleared after Register 1.8 is read and no fault condition occurs after 1.8 is read.	RO
1.1.2	RX_LINK (RX)	1 = Receive link is up 0 = Receive link is down	RO/LL
1.1.1	LOW_POWER_ABILITY (RX)	Always reads 1. 1 = Supports low power mode 0 = Does not support low power mode	RO

Table 112: PMA_DEV_IDENTIFIER_1

Device Address: 0x01	Register Address: 0x0002	Default: 0x4000	
Bit(s)	**Name**	**Description**	**Access**
1.2.15:0	DEV_IDENTIFIER[31:16] (RX)	16 MSB of 32 bit unique device identifier. See Table 114: UNIQUE DEVICE IDENTIFIER for identifier code details.	RO

Table 113: PMA_DEV_IDENTIFIER_2

Device Address: 0x01	Register Address: 0x0003	Default: 0x5100

[7] After reset bit is set to one, it automatically sets itself back to zero on the next MDC clock cycle.

Bit(s)	Name	Description	Access
1.3.15:0	DEV_IDENTIFIER[15:0] (RX)	16 LSB of 32 bit unique device identifier. See Table 114: UNIQUE DEVICE IDENTIFIER for identifier code details	RO

Table 114: UNIQUE DEVICE IDENTIFIER[8]

Register address	Value	Description
1.2.15:0	16'b0100_0000_0000_0000	OUI[3-18]
1.3.15:10	6'b010100	OUI[19-24]
1.3.9:4	6'b010000	6-bit Manufacturer device model number
1.3.3:0	4'b0000	4-bit Manufacturer device revision number

Table 115: PMA_SPEED_ABILITY

Device Address: 0x01	Register Address: 0x0004	Default: 0x0011	
Bit(s)	**Name**	**Description**	**Access**
1.4.4	SPEED_1G (RX)	Always reads 1. 1 = Capable of operating at 1000 Mb/s 0 = Not capable of operating at 1000 Mb/s	RO
1.4.0	SPEED_10G (RX)	Always reads 1. 1 = Capable of operating at 10 Gb/s 0 = Not capable of operating at 10 Gb/s	

Table 116: PMA_DEV_PACKAGE_1

Device Address: 0x01	Register Address: 0x0005	Default: 0x000B	
Bit(s)	**Name**	**Description**	**Access**
1.5.3	PCS_ PRESENT (RX)	Always reads 1. 1 = PCS present in the package 0 = PCS not present in the package	RO
1.5.1	PMA_PMD_PRESENT (RX)	Always reads 1. 1 = PMA/PMD present in the package 0 = PMA/PMD not present in the package	
1.5.0	CL22_PRESENT (RX)	Always reads 1. 1 = Clause 22 registers present in the package 0 = Clause 22 registers not present in the package	

Table 117: PMA_DEV_PACKAGE_2

Device Address: 0x01	Register Address: 0x0006	Default: 0x4000	
Bit(s)	**Name**	**Description**	**Access**

[8] The identifier code is composed of bits 3-24 of 25-bit organizationally unique identifier (OUI) assigned to Texas Instruments by IEEE. The 6-bit Manufacturer device model number is unique to TLK10232. The 4-bit Manufacturer device revision number denotes the current revision of TLK10232.

1.6.15	VS_DEV2_PRESENT (RX)	Always reads 0. 1 = Vendor specific device 2 present in the package 0 = Vendor specific device 2 not present in the package	RO
1.6.14	VS_DEV1_PRESENT (RX)	Always reads 1. 1 = Vendor specific device 1 present in the package 0 = Vendor specific device 1 not present in the package	RO

Table 118: PMA_STATUS_2

Device Address: 0x01	Register Address: 0x0008	Default: 0xB000	
Bit(s)	**Name**	**Description**	**Access**
1.8.15:14	DEV_PRESENT (RX)	Always reads 2'b10 0x = No device responding at this address 10 = Device responding at this address 11 = No device responding at this address	RO
1.8.13	TX_FAULT_ABILITY (RX)	Always reads 1'b1. 1 = Able to detect fault condition on Tx path 0 = Not able to detect fault condition on Tx path	RO
1.8.12	RX_FAULT_ABILITY (RX)	Always reads 1'b1. 1 = Able to detect fault condition on Rx path 0 = Not able to detect fault condition on Rx path	RO
1.8.11	TX_FAULT (RX)	1 = Fault condition detected on transmit path 0 = No fault condition detected on transmit path	RO/LH
1.8.10	RX_FAULT (RX)	1 = Fault condition detected on receive path 0 = No fault condition detected on receive path	RO/LH
1.8.8	TX_DISABLE_ABILITY (RX)	Always reads 1'b0. 1 = Able to perform transmit disable function 0 = Not able to perform transmit disable function	RO

Table 119: PMA_RX_SIGNAL_DET_STATUS

Device Address: 0x01	Register Address: 0x000A	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
1.10.0	RX_SIGNAL_DET (RX)	1 = Signal detected on serial Rx pins 0 = Signal detected on serial Rx pins	RO

Table 120: PMA_EXTENDED_ABILITY

Device Address: 0x01	Register Address: 0x000B	Default: 0x0050	
Bit(s)	**Name**	**Description**	**Access**
1.11.6	KX_ABILITY (RX)	Always reads 1'b1 1 = Able to perform 1000BASE-KX 0 = Not able to perform 1000BASE-KX	RO
1.11.4	KR_ABILITY (RX)	Always reads 1'b1 1 = Able to perform 10GBASE-KR 0 = Not able to perform 10GBASE-KR	RO

Table 121: LT_TRAIN_CONTROL

Device Address: 0x01	Register Address: 0x0096	Default: 0x0002	
Bit(s)	**Name**	**Description**	**Access**
1.150.1 / 30.150.1	LT_TRAINING_ENABLE (RXG)	1 = Enable start-up protocol as per 10GKR standard(Default 1'b1) 0 = Disable start-up protocol This bit should be set to HIGH for autotrain mode to function correctly When set, requires override bits specified in VS_SERDES_CFG_OVERRIDE_CTRL register to be set in order for full control of SERDES macros through MDIO	RW
1.150.0 / 30.150.0	LT_RESTART_TRAINING (RXG)	1 = Reset link/auto train 0 = Normal operation (Default 1'b0) Since this is the last bit of the MDIO write transaction, when set, it gets cleared at the first mdio clock in the next transaction.	RW/SC

Table 122: LT_TRAIN_STATUS

Device Address: 0x01	Register Address: 0x0097	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
1.151.3 / 30.151.3	LT_TRAINING_FAIL (RXG)	1 = Training failure has been detected 0 = Training failure has not been detected	RO
1.151.2 / 30.151.2	LT_START_PROTOCOL (RXG)	1 = Start up protocol in progress 0 = Start up protocol complete	
1.151.1 / 30.151.1	LT_FRAME_LOCK (RXG)	1 = Training frame delineation detected 0 = Training frame delineation not detected	
1.151.0 / 30.151.0	LT_RX_STATUS (RXG)	1 = Receiver trained and ready to receive data 0 = Receiver training in progress	

Table 123: LT_LINK_PARTNER_CONTROL

Device Address: 0x01	Register Address: 0x0098	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
1.152.13 / 30.152.13	LT_LP_PRESET (RXG)	1 = KR preset coefficients 0 = Normal operation	RO
1.152.12 / 30.152.12	LT_LP_INITIALIZE (RXG)	1 = Initialize KR coefficients 0 = Normal operation	
1.152.9:8 / 30.152.9:8	LT_LP_COEFF_SWG (RXG)	Swing update 11 = Reserved 01 = Increment 10 = Decrement 00 = Hold	
1.152.7:6 / 30.152.7:6	LT_LP_COEFF_PS2 (RXG)	Post2 tap control update 11 = Reserved 01 = Increment 10 = Decrement 00 = Hold	

1.152.5:4 / 30.152.5:4	LT_LP_COEFF_P1 (RXG)	Coefficient K(+1) update 11 = Reserved 01 = Increment 10 = Decrement 00 = Hold	
1.152.3:2 / 30.152.3:2	LT_LP_COEFF_0 (RXG)	Coefficient K(0) update 11 = Reserved 01 = Increment 10 = Decrement 00 = Hold	
1.152.1:0 / 30.152.1:0	LT_LP_COEFF_M1 (RXG)	Coefficient K(-1) update 11 = Reserved 01 = Increment 10 = Decrement 00 = Hold (Default 2'b00)	

Table 124: LT_LINK_PARTNER_STATUS

Device Address: 0x01	**Register Address: 0x0099**	**Default: 0x0000**	
Bit(s)	**Name**	**Description**	**Access**
1.153.15 / 30.153.15	LT_LP_RX_READY (RXG)	1 = LP receiver has determined that training is complete and prepared to receive data 0 = LP receiver is requesting that training continue	RO
1.153.9:8 / 30.153.9:8	LT_LP_COEFF_SWG_STAT (RXG)	Swing update 11 = Maximum 01 = Updated 10 = Minimum 00 = Not updated	
1.153.7:6 / 30.153.7:6	LT_LP_COEFF_PS2_STAT (RXG)	Post2 tap control update 11 = Maximum 01 = Updated 10 = Minimum 00 = Not updated	
1.153.5:4 / 30.153.5:4	LT_LP_COEFF_P1_STAT (RXG)	Plus 1 update 11 = Maximum 01 = Updated 10 = Minimum 00 = Not updated	
1.153.3:2 / 30.153.3:2	LT_LP_COEFF_0_STAT (RXG)	0 update 11 = Maximum 01 = Updated 10 = Minimum 00 = Not updated	
1.153.1:0 / 30.153.1:0	LT_LP_COEFF_M1_STAT (RXG)	Minus 1 update 11 = Maximum 01 = Updated 10 = Minimum 00 = Not updated	

Table 125: LT_LOCAL_DEVICE_CONTROL[9]

Device Address: 0x01	**Register Address: 0x009A**	**Default: 0x0000**	
Bit(s)	**Name**	**Description**	**Access**

[9] This register values reflects muxed version of the controls coming from search algorithm

1.154.15 / 30.154.15	RESERVED AP_LD_RX_TRAINED (RXG)	For TI use only (Default 1'b0) 1 = Set to communicate that manual link training is completed 0 = Normal operation (Default 1'b0)	RO/RW[10]
1.154.13 / 30.154.13	LT_LD_PRESET (RXG)	1 = KR preset coefficients 0 = Normal operation (Default 1'b0)	RO/RW[11]
1.154.12 / 30.154.12	LT_ LD_INITIALIZE (RXG)	1 = Initialize KR coefficients 0 = Normal operation (Default 1'b0)	
1.154.9:8 / 30.154.9:8	LT_LD_COEFF_SWG (RXG)	Swing update 11 = Reserved 01 = Increment 10 = Decrement 00 = Hold (Default 2'b00)	
1.154.7:6 / 30.154.7:6	LT_LD_COEFF_PS2 (RXG)	Post2 tap control update 11 = Reserved 01 = Increment 10 = Decrement 00 = Hold (Default 2'b00)	
1.154.5:4 / 30.154.5:4	LT_ LD_COEFF_P1 (RXG)	Coefficient K(+1) update 11 = Reserved 01 = Increment 10 = Decrement 00 = Hold (Default 2'b00)	
1.154.3:2 / 30.154.3:2	LT_ LD_COEFF_0 (RXG)	Coefficient K(0) update 11 = Reserved 01 = Increment 10 = Decrement 00 = Hold (Default 2'b00)	
1.154.1:0 / 30.154.1:0	LT_ LD_COEFF_M1 (RXG)	Coefficient K(-1) update 11 = Reserved 01 = Increment 10 = Decrement 00 = Hold (Default 2'b00)	

Table 126: LT_LOCAL_DEVICE_STATUS

Device Address: 0x01	Register Address: 0x009B	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
1.155.15 / 30.155.15	LT_ LD_RX_READY (RXG)	1 = LD receiver has determined that training is complete and prepared to receive data 0 = LD receiver is requesting that training continue	RO
1.155.5:4 / 30.155.4	LT_ LD_COEFF_P1_STAT (RXG)	Plus 1 update 11 = Maximum 01 = Updated 10 = Minimum 00 = Not updated	
1.155.3:2 / 30.155.3:2	LT_ LD_COEFF_0_STAT (RXG)	0 update 11 = Maximum 01 = Updated 10 = Minimum 00 = Not updated	

[10] These bits are RW during manual search mode
[11] These bits are RW during manual search mode

1.155.1:0 / 30.155.1:0	LT_ LD_COEFF_M1_STAT (RXG)	Minus 1 update 11 = Maximum 01 = Updated 10 = Minimum 00 = Not updated	

Table 127: KX_STATUS

Device Address: 0x01	Register Address: 0x00A1	Default: 0x3000	
Bit(s)	**Name**	**Description**	**Access**
1.161.13	KX_TX_FAULT_ABILITY (X)	Always reads 1. 1 = Has ability to detect a fault condition on transmit path 0 = Does not have ability to detect a fault condition on transmit path	RO
1.161.12	KX_RX_FAULT_ABILITY (X)	Always reads 1. 1 = Has ability to detect a fault condition on receive path 0 = Does not have ability to detect a fault condition on receive path	RO
1.161.11	KX_TX_FAULT (X)	1 = Fault condition detected on transmit path 0 = No fault condition detected on transmit path	RO/LH
1.161.10	KX_RX_FAULT (X)	1 = Fault condition detected on receive path 0 = No fault condition detected on receive path	RO/LH
1.161.0	KX_RX_SIGNAL_DETECT (X)	1 = Signal detected 0 = Signal not detected	RO

Table 128: KR_FEC_ABILITY

Device Address: 0x01	Register Address: 0x00AA	Default: 0x0003	
Bit(s)	**Name**	**Description**	**Access**
1.170.1	KR_FEC_ERR_ABILITY (R)	Always reads 1. 1 = Device supports 10GBASE-R FEC error indication to PCS 0 = Device does not support 10GBASE-R FEC function error indication tx PCS	RO
1.170.0	KR_FEC_ABILITY (R)	Always reads 1. 1 = Device supports 10GBASE-R FEC function 0 = Device does not support 10GBASE-R FEC function	

Table 129: KR_FEC_CONTROL

Device Address: 0x01	Register Address: 0x00AB	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
1.171.1	KR_FEC_ERR_IND_EN (R)	1 = Enable FEC decoder to indicate errors to PCS 0 = Disable FEC decoder error indication to PCS (Default 1'b0)	RW
1.171.0	KR_FEC_EN (R)	1 = Enable 10GBASE-R FEC function 0 = Disable 10GBASE-R FEC function (Default 1'b0)	

Table 130: KR_FEC_C_COUNT_1[12]

Device Address: 0x01	Register Address: 0x00AC	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
1.172.15:0	KR_FEC_C_COUNT[15:0] (R)	Lower 16 bits of FEC corrected blocks counter	COR

Table 131: KR_FEC_C_COUNT_2

Device Address: 0x01	Register Address: 0x00AD	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
1.173.15:0	KR_FEC_C_COUNT[31:16] (R)	Upper 16 bits of FEC corrected blocks counter	COR

Table 132: KR_FEC_UC_COUNT_1[13]

Device Address: 0x01	Register Address: 0x00AE	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
1.174.15:0	KR_FEC_UC_COUNT[15:0] (R)	Lower 16 bits of FEC Uncorrected blocks counter	COR

Table 133: KR_FEC_UC_COUNT_2

Device Address: 0x01	Register Address: 0x00AF	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
1.175.15:0	KR_FEC_UC_COUNT[31:16] (R)	Upper 16 bits of FEC Uncorrected blocks counter	COR

Table 134: TI_RESERVED_CONTROL(KR_VS_FEC_CONTROL_1)

Device Address: 0x01	Register Address: 0x8000	Default: 0x4800	
Bit(s)	**Name**	**Description**	**Access**
1.32768.15:12	RESERVED KR_RX_FEC_VALID[3:0] (R)	For TI use only (Default 4'b0100) Number of valid parity count required to assert FEC Block lock (Default 4'b0100)	RW
1.32768.11:8	RESERVED KR_RX_FEC_INVALID[3:0] (R)	For TI use only (Default 4'b1000) Number of invalid parity count required to de-assert FEC Block lock (Default 4'b1000)	

[12] To get correct 32 bit counter value of KR_FEC_C_COUNT, Register 1.172 should be read first followed by Register 1.173

[13] To get correct 32 bit counter value of KR_FEC_UC_COUNT, Register 1.174 should be read first followed by Register 1.175

1.32768.5	RESERVED KR_ FEC_SLIP_EN (R)	For TI use only (Default 1'b0) 1 = Enable FEC slip by 1 position 0 = Disable FEC slip (Default 1'b0)	RW/SC
1.32768.4	RESERVED KR_ FEC_FREEZE_EN (R)	For TI use only (Default 1'b0) 1 = Enable FEC freeze 0 = Disable FEC freeze (Default 1'b0)	RW
1.32768.1	RESERVED KR_RX_FEC_PN_2112_GEN_DIS (R)	For TI use only (Default 1'b0) 1 = Disable RX FEC PN-2112 pseudo noise sequence generation 0 = Enable RX FEC PN-2112 pseudo noise sequence generation (Default 1'b0)	
1.32768.0	RESERVED KR_TX_FEC_PN_2112_GEN_DIS (R)	For TI use only (Default 1'b0) 1 = Disable TX FEC PN-2112 pseudo noise sequence generation 0 = Enable TX FEC PN-2112 pseudo noise sequence generation (Default 1'b0)	

Table 135: KR_VS_FIFO_CONTROL_1

Device Address: 0x01	Register Address:0x8001	Default: 0xCC4C	
Bit(s)	**Name**	**Description**	**Access**
1.32769.15	RESERVED AUTO_XMIT_IDLE (R)	1 = Transmit idle pattern onto LS side during Auto negotiation or link training (Default 1'b1) 0 = Normal operation	RW
1.32769.14:12	RX_FIFO_DEPTH[2:0] (R)	Rx CTC FIFO depth selection 1xx = 32 deep (Default 3'b100) 011 = 24 deep 010 = 16 deep 001 = 12 deep 000 = 8 deep (No CTC function)	
1.32769.11:10	RX_CTC_WMK_SEL[1:0] (R)	Water mark selection for receive CTC Works in conjunction with RX_FIFO_DEPTH_SEL setting (Default 2'b11)	
1.32769.9	RX_Q_CNT_IPG (R)	0 = Normal operation. (Default 1'b0) 1 = Sequence columns are counted as IPG.	
1.32769.8	RX_CTC_Q_DROP_EN (R)	0 = Normal operation. (Default 1'b0) 1 = Enable Q column drop in RX CTC.	
1.32769.7	XMIT_IDLE (R)	1 = Transmit idle pattern onto LS side 0 = Normal operation (Default 1'b0)	
1.32769.6:4	TX_FIFO_DEPTH[2:0] (R)	Tx CTC FIFO depth selection 1xx = 32 deep (Default 3'b100) 011 = 24 deep 010 = 16 deep 001 = 12 deep 000 = 8 deep (No CTC function)	
1.32769.3:2	TX_CTC_WMK_SEL[1:0] (R)	Water mark selection for transmit CTC Works in conjunction with TX_FIFO_DEPTH_SEL setting (Default 2'b11)	

Depth ->	32	24	16	12/8
11	High	High	High	NA
10	Mid-high	Mid	High	
01	Mid	Low	Low	
00	Low	Low	Low	

Depth ->	32	24	16	12/8
11	High	High	High	NA
10	Mid-high	Mid	High	
01	Mid	Low	Low	
00	Low	Low	Low	

1.32769.1	TX_Q_CNT_IPG (R)	0 = Normal operation. (Default 1'b0) 1 = Sequence columns are counted as IPG.	
1.32769.0	TX_CTC_Q_DROP_EN (R)	0 = Normal operation. (Default 1'b0) 1 = Enable Q column drop in TX CTC.	

Table 136: KR_VS_TP_GEN_CONTROL

Device Address: 0x01	Register Address:0x8002	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
1.32770.5:4	RX_TPG_HLM_TEST_SEL[1:0] (R)	00 = High Frequency test pattern(Default 2'b00) 01 = Low Frequency test pattern 10 = Mixed Frequency test pattern 11 = Normal operation See Test pattern procedures for more information.	RW
1.32770.3	RX_TPG_CRPAT_TEST_EN (R)	0 = Normal operation. (Default 1'b0) 1 = Enables XAUI CRPAT test pattern generation See Test pattern procedures for more information.	
1.32770.2	RX_TPG_CJPAT_TEST_EN (R)	0 = Normal operation. (Default 1'b0) 1 = Enables CJPAT test pattern generation See Test pattern procedures for more information.	
1.32770.1	RX_TPG_10GFC_TEST_EN (R)	0 = Normal operation. (Default 1'b0) 1 = Enables 10 GFC CJPAT test pattern generation See Test pattern procedures for more information.	
1.32770.0	RX_TPG_HLM_TEST_EN (R)	0 = Normal operation. (Default 1'b0) 1 = Enables H/L/M test pattern generation See Test pattern procedures for more information.	

Table 137: KR_VS_TP_VER_CONTROL

Device Address: 0x01	Register Address:0x8003	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
1.32771.13:12	TX_TPV_HLM_TEST_SEL[1:0] (R)	00 = High Frequency test pattern(Default 2'b00) 01 = Low Frequency test pattern 10 = Mixed Frequency test pattern 11 = Normal operation See Test pattern procedures for more information.	RW
1.32771.11	TX_TPV_CRPAT_TEST_EN (R)	0 = Normal operation. (Default 1'b0) 1 = Enables CRPAT test pattern verification See Test pattern procedures for more information.	
1.32771.10	TX_TPV_CJPAT_TEST_EN (R)	0 = Normal operation. (Default 1'b0) 1 = Enables CJPAT test pattern verification See Test pattern procedures for more information.	
1.32771.9	TX_TPV_10GFC_TEST_EN (R)	0 = Normal operation. (Default 1'b0) 1 = Enables 10 GFC CJPAT test pattern verification See Test pattern procedures for more information.	
1.32771.8	TX_TPV_HLM_TEST_EN (R)	0 = Normal operation. (Default 1'b0) 1 = Enables H/L/M test pattern verification See Test pattern procedures for more information.	
1.32771.5:4	RESERVED RX_TPV_HLM_TEST_SEL[1:0] (R)	For TI use only(Default 2'b00) 00 = High operation. (Default 2'b00) 01 = Low Frequency test pattern 10 = Mixed Frequency test pattern 11 = Normal operation	

1.32771.3	RESERVED RX_TPV_CRPAT_TEST_EN (R)	For TI use only(Default 1'b0) 0 = Normal operation. (Default 1'b0) 1 = Enables CRPAT test pattern verification	
1.32771.2	RESERVED RX_TPV_CJPAT_TEST_EN (R)	For TI use only(Default 1'b0) 0 = Normal operation. (Default 1'b0) 1 = Enables CJPAT test pattern verification	
1.32771.1	RESERVED RX_TPV_10GFC_TEST_EN (R)	For TI use only(Default 1'b0) 0 = Normal operation. (Default 1'b0) 1 = Enables 10 GFC CJPAT test pattern verification	
1.32771.0	RESERVED RX_TPV_HLM_TEST_EN (R)	For TI use only(Default 1'b0) Low frequency pattern will not work since HS decoder treats FC as invalid character. 0 = Normal operation. (Default 1'b0) 1 = Enables H/L/M test pattern verification	

Table 138: KR_VS_CTC_ERR_CODE_LN0

Device Address: 0x01	Register Address: 0x8005	Default: 0xCE00	
Bit(s)	**Name**	**Description**	**Access**
1.32773.15:7	KR_CTC_ERR_CODE_LN0 (R)	Applicable in 10G-KR mode only. XGMII code to be transmitted in case of error condition. This applies to both TX and RX data paths. The msb is the control bit; remaining 8 bits constitute the error code. The default value for lane 0 corresponds to 8'h9C with the control bit being 1'b1. The default values for lanes 0~3 correspond to ||LF||	RW

Table 139: KR_VS_CTC_ERR_CODE_LN1

Device Address: 0x01	Register Address: 0x8006	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
1.32774.15:7	KR_CTC_ERR_CODE_LN1 (R)	Applicable in 10G-KR mode only. XGMII code to be transmitted in case of error condition. This applies to both TX and RX data paths. The msb is the control bit; remaining 8 bits constitute the error code. The default value for lane 1 corresponds to 8'h00 with the control bit being 1'b0. The default values for lanes 0~3 correspond to ||LF|	RW

Table 140: KR_VS_CTC_ERR_CODE_LN2

Device Address: 0x01	Register Address: 0x8007	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
1.32775.15:7	KR_CTC_ERR_CODE_LN2 (R)	Applicable in 10G-KR mode only. XGMII code to be transmitted in case of error condition. This applies to both TX and RX data paths. The msb is the control bit; remaining 8 bits constitute the error code. The default value for lane 2 corresponds to 8'h00 with the control bit being 1'b0. The default values for lanes 0~3 correspond to ||LF|	RW

Table 141: KR_VS_CTC_ERR_CODE_LN3

Device Address: 0x01	Register Address: 0x8008	Default: 0x0080	
Bit(s)	**Name**	**Description**	**Access**

1.32776.15:7	KR_CTC_ERR_CODE_LN3 (R)	Applicable in 10G-KR mode only. Error code to be transmitted in case of error condition. This applies to both TX and RX data paths. The msb is the control bit; remaining 8 bits constitute the error code. The default value for lane 3 corresponds to 8'h01 with the control bit being 1'b0. The default values for lanes 0~3 correspond to ||LF|	RW

Table 142: KR_VS_LN0_EOP_ERROR_COUNTER

Device Address: 0x01	Register Address: 0x8010	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
1.32784.15:0	KR_LN0_EOP_ERR_COUNT (R)	Lane 0 End of packet Error counter. Valid in 10GKR mode only End of packet error is detected when Terminate character is in lane 0 and one or both of the following holds: • Terminate character is not followed by /K/ characters in lanes 1, 2 and 3 • The column following the terminate column is neither ||K|| nor ||A||. Counter value cleared to 16'h0000 when read.	COR

Table 143: KR_VS_LN1_EOP_ERROR_COUNTER

Device Address: 0x01	Register Address: 0x8011	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
1.32785.15:0	KR_LN1_EOP_ERR_COUNT (R)	Lane 1 End of packet Error counter. Valid in 10GKR mode only End of packet error is detected when Terminate character is in lane 1 and one or both of the following holds: • Terminate character is not followed by /K/ characters in lanes 2 and 3 • The column following the terminate column is neither ||K|| nor ||A||. Counter value cleared to 16'h0000 when read.	COR

Table 144: KR_VS_LN2_EOP_ERROR_COUNTER

Device Address: 0x01	Register Address: 0x8012	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
1.32786.15:0	KR_LN2_EOP_ERR_COUNT (R)	Lane 2 End of packet Error counter. Valid in 10GKR mode only End of packet error is detected when Terminate character is in lane 2 and one or both of the following holds: • Terminate character is not followed by /K/ characters in lane 3 • The column following the terminate column is neither ||K|| nor ||A||. Counter value cleared to 16'h0000 when read.	COR

Table 145: KR_VS_LN3_EOP_ERROR_COUNTER

Device Address: 0x01	Register Address: 0x8013	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
1.32787.15:0	KR_LN3_EOP_ERR_COUNT (R)	Lane 3 End of packet Error counter. Valid in 10GKR mode only End of packet error is detected when Terminate character is in lane 3 and the column following the terminate column is neither ||K|| nor ||A||. Counter value cleared to 16'h0000 when read.	COR

Table 146: KR_VS_TX_CTC_DROP_COUNT

Device Address: 0x01	Register Address: 0x8014	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
1.32788.15:0	TX_CTC_DROP_COUNT (R)	Counter for number of idle drops in the transmit CTC.	COR

Table 147: KR_VS_TX_CTC_INSERT_COUNT

Device Address: 0x01	Register Address: 0x8015	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
1.32789.15:0	TX_CTC_INS_COUNT (R)	Counter for number of idle inserts in the transmit CTC.	COR

Table 148: KR_VS_RX_CTC_DROP_COUNT

Device Address: 0x01	Register Address: 0x8016	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
1.32790.15:0	RX_CTC_DROP_COUNT (R)	Counter for number of idle drops in the receive CTC.	COR

Table 149: KR_VS_RX_CTC_INSERT_COUNT

Device Address: 0x01	Register Address: 0x8017	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
1.32791.15:0	RX_CTC_INS_COUNT (R)	Counter for number of idle inserts in the receive CTC.	COR

Table 150: KR_VS_STATUS_1

Device Address: 0x01	Register Address: 0x8018	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
1.32792. 15	TX_TPV_TP_SYNC (R)	0 = Test pattern sync is not achieved on Tx side 1 = Test pattern sync is achieved on Tx side	RO
1.32792. 11	RESERVED RX_TPV_TP_SYNC (R)	For TI use only 0 = Test pattern sync is not achieved on Rx side 1 = Test pattern sync is achieved on Rx side	
1.32792. 5	INVALID_S_COL_ERR (R)	1 = Indicates invalid start (S) column error detected	RO/LH

1.32792. 4	INVALID_T_COL_ERR (R)	1 = Indicates invalid terminate (T) column error detected	
1.32792. 3	INVALID_XGMII_LN3 (R)	1 = Indicates invalid XGMII character detected in Lane 3	
1.32792. 2	INVALID_XGMII_LN2 (R)	1 = Indicates invalid XGMII character detected in Lane 2	
1.32792. 1	INVALID_XGMII_LN1 (R)	1 = Indicates invalid XGMII character detected in Lane 1	
1.32792. 0	INVALID_XGMII_LN0 (R)	1 = Indicates invalid XGMII character detected in Lane 0	

Table 151: KR_VS_TX_CRCJ_ERR_COUNT_1[14]

Device Address: 0x01	Register Address: 0x8019	Default: 0xFFFF	
Bit(s)	**Name**	**Description**	**Access**
1.32793.15:0	TX_TPV_CR_CJ_ERR_COUNT[31:16] (R)	Error Counter for CR/CJ test pattern verification on Tx side. MSB's [31:16]	COR

Table 152: KR_VS_TX_CRCJ_ERR_COUNT_2

Device Address: 0x01	Register Address: 0x801A	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
1.32794.15:0	TX_TPV_CR_CJ_ERR_COUNT[15:0] (R)	Error Counter for CR/CJ test pattern verification on Tx side LSB's [15:0]	COR

Table 153: KR_VS_TX_LN0_HLM_ERR_COUNT

Device Address: 0x01	Register Address: 0x801B	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
1.32795.15:0	TX_TPV_LN0_ERR_COUNT[15:0] (R)	Error Counter for H/L/M test pattern verification on Lane 0 of Tx side	COR

Table 154: KR_VS_TX_LN1_HLM_ERR_COUNT

Device Address: 0x01	Register Address: 0x801C	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**

[14] User has to make sure that register 0x8019 is read first and then register 0x801A. If user reads register 0x801A before reading register 0x8019, then the count value read through register 0x8019 may not be correct

1.32796.15:0	TX_TPV_LN1_ERR_COUNT[15:0] (R)	Error Counter for H/L/M test pattern verification on Lane 1 of Tx side	COR

Table 155: KR_VS_TX_LN2_HLM_ERR_COUNT

Device Address: 0x01	Register Address: 0x801D	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
1.32797.15:0	TX_TPV_LN2_ERR_COUNT[15:0] (R)	Error Counter for H/L/M test pattern verification on Lane 2 of Tx side	COR

Table 156: KR_VS_TX_LN3_HLM_ERR_COUNT

Device Address: 0x01	Register Address: 0x801E	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
1.32798.15:0	TX_TPV_LN3_ERR_COUNT[15:0] (R)	Error Counter for H/L/M test pattern verification on Lane 3 of Tx side	COR

Table 157: TI_RESERVED_STATUS(KR_VS_RX_LN0_HLM_ERR_COUNT)

Device Address: 0x01	Register Address: 0x801F	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
1.32799.15:0	RESERVED RX_TPV_LN0_ERR_COUNT[15:0] (R)	For TI use only Error Counter for H/L/M test pattern verification on Lane 0 of Rx side	COR

Table 158: TI_RESERVED_STATUS(KR_VS_RX_LN1_HLM_ERR_COUNT)

Device Address: 0x01	Register Address: 0x8020	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
1.32800.15:0	RESERVED RX_TPV_LN1_ERR_COUNT[15:0] (R)	For TI use only Error Counter for H/L/M test pattern verification on Lane 1 of Rx side	COR

Table 159: TI_RESERVED_STATUS(KR_VS_RX_LN2_HLM_ERR_COUNT)

Device Address: 0x01	Register Address: 0x8021	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
1.32801.15:0	RESERVED RX_TPV_LN2_ERR_COUNT[15:0] (R)	For TI use only Error Counter for H/L/M test pattern verification on Lane 2 of Rx side	COR

Table 160: TI_RESERVED_STATUS(KR_VS_RX_LN3_HLM_ERR_COUNT)

Device Address: 0x01	Register Address: 0x8022	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
1.32802.15:0	RESERVED RX_TPV_LN3_ERR_COUNT[15:0] (R)	For TI use only Error Counter for H/L/M test pattern verification on Lane 3 of Rx side	COR

Table 161: TI_RESERVED_STATUS(KR_VS_RX_CRCJ_ERR_COUNT_1) [15]

Device Address: 0x01	Register Address: 0x8023	Default: 0xFFFF	
Bit(s)	**Name**	**Description**	**Access**
1.32803.15:0	RESERVED RX_TPV_CR_CJ_ERR_COUNT[31:16] (R)	For TI use only Error Counter for CR/CJ test pattern verification on Rx side. MSB's [31:16]	COR

Table 162: TI_RESERVED_STATUS(KR_VS_RX_CRCJ_ERR_COUNT_2)

Device Address: 0x01	Register Address: 0x8024	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
1.32804.15:0	RESERVED RX_TPV_CR_CJ_ERR_COUNT[15:0] (R)	For TI use only Error Counter for CR/CJ test pattern verification on Rx side. LSB's [15:0]	COR

Table 163: TI_RESERVED_CONTROL(LT_VS_CONTROL_1)

Device Address: 0x01	Register Address: 0x9000	Default: 0x0249	
Bit(s)	**Name**	**Description**	**Access**
1.36864.9:4 / 30.36864.9:4	RESERVED AP_LIMIT_INIT_X[5:0] (RXG)	For TI use only (Default 6'b100100) External limit for controlling v2 keep out region	RW
1.36864.3 / 30.36864.3	RESERVED AT_AUTODIS_MAXWAIT (RXG)	For TI use only (Default 1'b1) Valid only when autotrain is enabled. 1 = Autotrain continues even after timer value specified in AP_MAX_WAIT_TIMER expires 0 = Autotrain exits after timer value specified in AP_MAX_WAIT_TIMER expires	
1.36864.2 / 30.36864.2	RESERVED AP_USE_EXT_INIT (RXG)	For TI use only (Default 1'b0) 1 = Use ext_init_in[32:14] values as initial tap weight on INIT command 0 = Use internally defined tap weights	
1.36864.1 / 30.36864.1	RESERVED AP_CONST_VPK_MODE (RXG)	For TI use only (Default 1'b0) 1 = Main cursor forced to 0 0 = Main cursor can be reduced	

[15] User has to make sure that register 0x8023 is read first and then register 0x8024. If user reads register 0x8024 before reading register 0x8023, then the count value read through register 0x8023 may not be correct

1.36864.0 / 30.36864.0	RESERVED AP_LIMIT_MODE (RXG)	For TI use only (Default 1'b1) 1 = Disable ps2 tap ad swing requests 0 = Allow ps2 tap and swing requests	

Table 164: TI_RESERVED_CONTROL(LT_VS_CONTROL_2)

Device Address: 0x01	Register Address: 0x9001	Default: 0x0200	
Bit(s)	**Name**	**Description**	**Access**
1.36865.15 / 30.36865.15	RESERVED AP_FRAME_PRBSERR_EN (RXG)	For TI use only (Default 1'b0) 1 = Framing errors are treated as PRBS11 errors 0 = Framing errors are not treated as PRBS11 errors	RW
1.36865.14 / 30.36865.14	RESERVED AP_ SINGLE_STEP (RXG)	For TI use only (Default 1'b0) 1 = Autotrain pauses at strategic points to allow intermediate values to be read via MDIO 0 = Autotrain runs to complete without user intervention	
1.36865.13 / 30.36865.13	RESERVED AP_NEXT_STEP (RXG)	For TI use only (Default 1'b0) 1 = Pulse to continue from the paused state of autotrain 0 = Normal operation	RW/SC
1.36865.12 / 30.36865.12	RESERVED AP_RST_READ_POINTER (RXG)	For TI use only (Default 1'b0) 1 = Pulse to reset the pointers of autotrain results 0 = Normal operation	
1.36865.11:9 / 30.36865.11:9	RESERVED AP_SEARCH_MODE[2:0] (RXG)	For TI use only (Default 3'b001) 000 = Auto search, autotrain disabled 001 = Full region search, autotrain disabled 010 = Auto search, autotrain enabled 011 = Full region search, autotrain enabled 1xx = Manual search	RW
1.36865.8 / 30.36865.8	RESERVED AP_FIVE_EN (RXG)	For TI use only (Default 1'b0) 1 = Enable first pass 5x5 grid checks 0 = Enable first pass 3x3 grid checks	
1.36865.7:4 / 30.36865.7:4	RESERVED AP_RX_RESET_MASK[3:0] (RXG)	For TI use only (Default 4'b0000) Mask for controlling serdes RX reset after issuing INIT command	
1.36865.3:2 / 30.36865.3:2	RESERVED AP_PRBS_ERR_SEL[1:0] (RXG)	For TI use only (Default 2'b00) Number of PRBS11 errors allowed before prbs error status asserts (Default 2'b00) 00 = 1 Error 01 = 2 Errors 10 = 4 Errors 11 = 8 Errors	
1.36865.1 / 30.36865.1	RESERVED AP_CONTINUOUS_TRAIN (RXG)	For TI use only (Default 1'b0) 1 = Force continuous training 0 = Normal operation	
1.36865.0 / 30.36865.0	RESERVED AP_FULL_SEARCH (RXG)	For TI use only (Default 1'b0) 1 = Force BER across full pre/post cursor space 0 = Normal operation	

Table 165: TI_RESERVED_CONTROL(LT_VS_TRAIN_MAX_TIMER_CTRL _1)

Device Address: 0x01	Register Address: 0x9002	Default: 0x1335	
Bit(s)	**Name**	**Description**	**Access**
1.36866.12:0 / 30.36866.12:0	RESERVED AP_MAX_WAIT_TIMER[28:16] (RXG)	For TI use only (Default 13'h1335) [28:16] bits of Max wait timer used in train sm. Should be programmed with number of clock cycles to count 500ms. Default value for entire timer is 29'h13335_5E29 (Default 13'h1335)	RW

Table 166: TI_RESERVED_CONTROL(LT_VS_TRAIN_MAX_TIMER_CTRL _2)

Device Address: 0x01	Register Address: 0x9003	Default: 0x5E29	
Bit(s)	**Name**	**Description**	**Access**
1.36867.15:0 / 30.36867.15:0	RESERVED AP_MAX_WAIT_TIMER[15:0] (RXG)	For TI use only (Default 16'h5E29) [28:16] bits of Max wait timer used in train sm. Should be programmed with number of clock cycles to count 500ms. Default value for entire timer is 29'h13335_5E29 (Default 16'h5E29)	RW

Table 167: TI_RESERVED_CONTROL(LT_VS_TRAIN_WAIT_TIMER_CTRL _1)

Device Address: 0x01	Register Address: 0x9004	Default: 0x007F	
Bit(s)	**Name**	**Description**	**Access**
1.36868.6:0 / 30.36868.6:0	RESERVED AP_FRAME_COUNT[6:0] (RXG)	For TI use only (Default 7'h7F) Number of frames to be transmitted after local and remote RX are trained (Default 7'h7F)	RW

Table 168: TI_RESERVED_CONTROL(LT_VS_PRBS_PKT_COUNT_CTRL)

Device Address: 0x01	Register Address: 0x9005	Default: 0x1C00	
Bit(s)	**Name**	**Description**	**Access**
1.36869.15:0 / 30.36869.15:0	RESERVED AP_PRBS_PKT_COUNT[15:0] (RXG)	For TI use only (Default 16'h1C00) Number of packets to perform PRBS11 checks on per tap setting	RW

Table 169: TI_RESERVED_CONTROL(LT_VS_SETTLE_TIMER_CTRL)

Device Address: 0x01	Register Address: 0x9006	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
1.36870.15:0 / 30.36870.15:0	RESERVED AP_SETTLE_TIME[15:0] (RXG)	For TI use only (Default 16'h0000) Settle time for BER test in training packets	RW

Table 170: TI_RESERVED_CONTROL(AT_RX_SETTLE_TIMER)

Device Address: 0x01	Register Address: 0x9007	Default: 0x5120	
Bit(s)	**Name**	**Description**	**Access**
1.36871.15:0 / 30.36871.15:0	RESERVED AT_RX_SETTLE_TIME[15:0] (RXG)	For TI use only (Default 16'h5120) Wait timer used when changing Rx settings before requesting swing or link training.	RW

Table 171: TI_RESERVED_CONTROL(AT_VS_SWING_TIMER)

Device Address: 0x01	Register Address: 0x9008	Default: 0xC018	
Bit(s)	**Name**	**Description**	**Access**

1.36872.15:0 / 30.36872.15:0	RESERVED AT_SWING_TIME[15:0] (RXG)	For TI use only (Default 16'hC018) Wait timer used when adjusting swing.	RW

Table 172: TI_RESERVED_CONTROL(AT_VS_LT_TIMEOUT)

Device Address: 0x01	Register Address: 0x9009	Default: 0xE667	
Bit(s)	**Name**	**Description**	**Access**
1.36873.15:0 / 30.36873.15:0	RESERVED AT_LT_TIMEOUT[15:0] (RXG)	For TI use only (Default 16'hE667) Wait timer used when executing link training.	RW

Table 173: TI_RESERVED_CONTROL(AT_VS_CDR_PRBS_PKT_COUNT_CTRL)

Device Address: 0x01	Register Address: 0x900A	Default: 0x5E8F	
Bit(s)	**Name**	**Description**	**Access**
1.36874.15:0 / 30.36874.15:0	RESERVED AT_CDR_PRBS_PKT_CNT[15:0] (RXG)	For TI use only (Default 16'h5E8F) Packet count for BER test after link training during CDR optimization phase of autotrain learn mode	RW

Table 174: TI_RESERVED_CONTROL(AT_VS_FT_PRBS_PKT_COUNT_CTRL)

Device Address: 0x01	Register Address: 0x900B	Default: 0xAFAF	
Bit(s)	**Name**	**Description**	**Access**
1.36875.15:0 / 30.36875.15:0	RESERVED AT_FT_PRBS_PKT_CNT[15:0] (RXG)	For TI use only (Default 16'hAFAF) Packet count for BER test after link training during fine tuning phase of autotrain learn mode	RW

Table 175: TI_RESERVED_CONTROL(AT_VS_PRBS_PKT_COUNT_CTRL)

Device Address: 0x01	Register Address: 0x900C	Default: 0x0800	
Bit(s)	**Name**	**Description**	**Access**
1.36876.15:0 / 30.36876.15:0	RESERVED AT_PRBS_PKT_CNT[15:0] (RXG)	For TI use only (Default 16'h0800) Number of packets to perform PRBS11 checks on per tap setting	RW

Table 176: TI_RESERVED_CONTROL(AT_VS_FT_FAST_PKT_COUNT_CTRL)

Device Address: 0x01	Register Address: 0x900D	Default: 0x461A	
Bit(s)	**Name**	**Description**	**Access**
1.36877.15:0 / 30.36877.15:0	RESERVED AT_FT_FAST_PKT_CNT[15:0] (RXG)	For TI use only (Default 16'h461A) Packet count for BER test after link training during autotrain fast mode	RW

Table 177: TI_RESERVED_CONTROL(AT_VS_VALUE_CTRL_1)

Device Address: 0x01	Register Address: 0x900E	Default: 0x1723

Bit(s)	Name	Description	Access
1.36878.14:12: / 30.36878.14:12	RESERVED AT_MIN_EQPRE[2:0] (RXG)	For TI use only (Default 3'b001) Minimum value for HS EQPRE during autotrain learn mode	RW
1.36878.10:8: / 30.36878.10:8	RESERVED AT_MAX_EQPRE[2:0] (RXG)	For TI use only (Default 3'b111) Maximum value for HS EQPRE during autotrain learn mode	
1.36878.7:6 / 30.36878.7:6	RESERVED AT_MIN_CDRFMULT[1:0] (RXG)	For TI use only (Default 2'b00) Minimum value for HS CDRMULT during autotrain learn mode	
1.36878.5:4 / 30.36878.5:4	RESERVED AT_MAX_CDRFMULT[1:0] (RXG)	For TI use only (Default 2'b10) Maximum value for HS CDRMULT during autotrain learn mode	
1.36878.3:2 / 30.36878.3:2	RESERVED AT_MIN_CDRTHR[1:0] (RXG)	For TI use only (Default 2'b00) Minimum value for HS CDRTHR during autotrain learn mode	
1.36878.1:0 / 30.36878.1:0	RESERVED AT_MAX_CDRTHR[1:0] (RXG)	For TI use only (Default 2'b11) Maximum value for HS CDRTHR during autotrain learn mode	

Table 178: TI_RESERVED_CONTROL(AT_VS_VALUE_CTRL_2)

Device Address: 0x01	Register Address: 0x900F	Default: 0x7003	
Bit(s)	**Name**	**Description**	**Access**
1.36879.15:13 / 30.36879.15:13	RESERVED AT_SWING_RX_CNT[2:0] (RXG)	For TI use only (Default 3'b011) Value to control number of cycles between changes to HS Rx settings while attempting to adjust swing.	
1.36879.12:4 / 30.36879.12:4	RESERVED AT_ADCGAIN_TARGET[8:0] (RXG)	For TI use only (Default 9'b100000000) Target value for HS Serdes adcgain output when optimizing swing in autotrain learn mode	RW
1.36879.2:0 / 30.36879.2:0	RESERVED AT_MAX_SWING[2:0] (RXG)	For TI use only (Default 3'b011) Maximum HS SWING value to try during swing optimization.	

Table 179: TI_RESERVED_CONTROL(AT_VS_MASK_CTRL)

Device Address: 0x01	Register Address: 0x9010	Default: 0x0851	
Bit(s)	**Name**	**Description**	**Access**
1.36880.14:8 / 30.36880.14:8	RESERVED AT_REPEAT_COUNT[6:0] (RXG)	For TI use only (Default 7'h08) Number of times to repeat link training at a particular setting to establish repeatability.	RW
1.36880.7:0 / 30.36880.7:0	RESERVED AT_MASK[7:0] (RXG)	For TI use only (Default 8'h51) Mask to control which parameters are swept during autotrain normal mode.	

Table 180: TI_RESERVED_CONTROL(AT_VS_LEARN_CTRL)

Device Address: 0x01	Register Address: 0x9011	Default: 0x1EFF	
Bit(s)	**Name**	**Description**	**Access**
1.36881.12 / 30.36881.12	RESERVED AT_USE_MIN_CDRTHR (RXG)	For TI use only (Default 1'b1) 1 = Autotrain picks lowest HS CDRTHR value that had 0 errors 0 = Autotrain picks middle HS CDRTHR value that had 0 errors	RW

1.36881.11:9 / 30.36881.11:9	RESERVED AT_LEARN_CTL[1:0] (RXG)	For TI use only (Default 3'b111) Mask to control which autotrain learn mode phases are executed.	
1.36881.8 / 30.36881.8	RESERVED AT_LEARN_MODE (RXG)	For TI use only (Default 1'b0) 1 = Enable autotrain learn mode 0 = Disable autotrain learn mode	
1.36881.7:0 / 30.36881.7:0	RESERVED AT_LEARN_MASK[7:0] (RXG)	For TI use only (Default 8'hFF) Mask to control which parameters are swept during autotrain learn mode.	

Table 181: TI_RESERVED_STATUS (LT_VS_TRAIN_STATUS)

Device Address: 0x01	Register Address: 0x9020	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
1.36896.12:8 / 30.36896.12:8	RESERVED AT_STATE[4:0] (RXG)	For TI use only. Indicates autotrain SM state	RO
1.36896.5 / 30.36896.5	RESERVED AT_COMPLETE_STATUS (RXG)	For TI use only When High, indicates autotrain is failed	
1.36896.4:3 / 30.36896.4:3	RESERVED AT_RUN_STATUS[1:0] (RXG)	For TI use only Indicates autotrain run status 00 = Auto train is not run 01 = Auto train is running 10 = Auto train is paused 11 = Auto train is done	
1.36896.2:1 / 30.36896.2:1	RESERVED AT_PHASE_STATUS[1:0] (RXG)	For TI use only. Indicates autotrain phase status 00 = Swing Phase 01 = CDR Phase 10 = Fine tuning Phase 11 = Fast mode Phase	
1.36896.0 / 30.36896.0	RESERVED LT_FAIL_LH (RXG)	For TI use only Link training fail status. When high, indicates link training has failed. This bit is latched high version 1.151.3	RO/LH

Table 182: TI_RESERVED_STATUS (LT_VS_PRBS_ERROR_COUNTER)

Device Address: 0x01	Register Address: 0x9021	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
1.36897.15:0 / 30.36897.15:0	RESERVED AP_PRBS_ERR_COUNT[15:0] (RXG)	For TI use only PRBS11 error counter. Applicable in MDIO manual training mode	COR

Table 183: TI_RESERVED_STATUS(LT_VS_BER_ECOUNT_STATUS)

Device Address: 0x01	Register Address: 0x9022	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
1.36898.15:0 / 30.36898.15:0	RESERVED AP_BER_ECOUNT_DATA[15:0] (RXG)	For TI use only BER data for currently selected Post-cursor across all Pre-cursor settings	RO

Table 184: TI_RESERVED_STATUS(AT_FINAL_METRICS_STATUS)

Device Address: 0x01	Register Address: 0x9023	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
1.36899.15:0 / 30.36899.15:0	RESERVED AT_FINAL_METRICS[15:0] (RXG)	For TI use only Read returns metrics (count and best distance) associated with AT_FINAL_SETTINGS. This register must be read first before reading AT_FINAL_SETTINGS	RO

Table 185: TI_RESERVED_STATUS(AT_FINAL_SETTINGS_STATUS)

Device Address: 0x01	Register Address: 0x9024	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
1.36900.15:0 / 30.36900.15:0	RESERVED AT_FINAL_SETTINGS[15:0] (RXG)	For TI use only Read returns best 32 settings in sorted order. Insert pointer is rest to the best settings when AP_RST_READ_POINTER is set	RO

Table 186: TI_RESERVED_STATUS(AT_SWING_STATUS)

Device Address: 0x01	Register Address: 0x9025	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
1.36901.15:0 / 30.36901.15:0	RESERVED AT_SWING_STATUS[15:0] (RXG)	For TI use only Read returns results from swing phase.	RO

Table 187: TI_RESERVED_STATUS(AT_CDR1_STATUS)

Device Address: 0x01	Register Address: 0x9026	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
1.36902.15:0 / 30.36902.15:0	RESERVED AT_CDR1_STATUS[15:0] (RXG)	For TI use only Read returns results from CDR1 phase.	RO

Table 188: TI_RESERVED_STATUS(AT_CDR2_STATUS)

Device Address: 0x01	Register Address: 0x9027	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
1.36903.9:0 / 30.36903.9:0	RESERVED AT_CDR2_STATUS[9:0] (RXG)	For TI use only Read returns results from CDR2 phase.	RO

Table 189: TI_RESERVED_STATUS(AT_RANGE_DATA_1)

Device Address: 0x01	Register Address: 0x9028	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**

1.36904.11:0 / 30.36904.11:0	RESERVED AT_RANGE_DATA[27:16] (RXG)	For TI use only 11 MSB's of AT_RANGE_DATA[27:0] value.	RO

Table 190: TI_RESERVED_STATUS(AT_RANGE_DATA_0)

Device Address: 0x01	Register Address: 0x9029	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
1.36905.15:0 / 30.36905.15:0	RESERVED AT_RANGE_DATA[15:0] (RXG)	For TI use only 16 LSB's of AT_RANGE_DATA[27:0] value.	RO

PCS REGISTERS

Below registers can be accessed only in Clause 45 mode and with device address field set to 0x03 (DEVADD [4:0] = 5'b00011). Valid only when device is in 10GBASE-KR mode.

Table 191: PCS_CONTROL

Device Address: 0x03	Register Address: 0x0000	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
3.0.15	PCS_RESET (R)	1 = Resets datapath and MDIO registers of all channels. Equivalent to asserting RESET_N. 0 = Normal operation (Default 1'b0)	RW/SC
3.0.14	PCS_LOOPBACK (R)	1 = Enables PCS loopback Same as shallow local loopback in 10G-KR mode. 0 = Normal operation (Default 1'b0)	RW
3.0.11	PCS_LP_MODE (R)	1 = Enable power down mode 0 = Normal operation (Default 1'b0)	RW

Table 192: PCS_STATUS_1

Device Address: 0x03	Register Address: 0x0001	Default: 0x0002	
Bit(s)	**Name**	**Description**	**Access**
3.1.7	PCS_FAULT (R)	1 = Fault condition detected on either PCS TX or PCS RX 0 = No fault condition detected This bit is cleared after Register 3.8 is read and no fault condition occurs after 3.8 is read.	RO
3.1.2	PCS_RX_LINK (R)	1 = PCS receive link is up 0 = PCS receive link is down	RO/LL
3.1.1	PCS_LP_ABILITY (R)	Always reads 1. 1 = Supports low power mode 0 = Does not support low power mode	RO

Table 193: PCS_STATUS_2

Device Address: 0x03	Register Address: 0x0008	Default: 0x8001	
Bit(s)	**Name**	**Description**	**Access**
3.8.15:14	DEV_PRESENT (R)	Always reads 2'b10. 0x = No device responding at this address 10 = Device responding at this address 11 = No device responding at this address	RO
3.8.11	PCS_TX_FAULT (R)	1 = Fault condition detected on transmit path 0 = No fault condition detected on transmit path	RO/LH
3.8.10	PCS_RX_FAULT (R)	1 = Fault condition detected on receive path 0 = No fault condition detected on receive path	RO/LH
3.8.0	PCS_10GBASER_CAPABLE (R)	Always reads 1. 1 = PCS is able to support 10GBASE-R PCS type 0 = PCS not able to support 10GBASE-R PCS type	RO

Table 194: KR_PCS_STATUS_1

Device Address: 0x03	Register Address: 0x0020	Default: 0x0004	
Bit(s)	**Name**	**Description**	**Access**
3.32.12	PCS_RX_LINK_STATUS (R)	1 = 10GBASE-R PCS receive link up 0 = 10GBASE-R PCS receive link down	RO
3.32.2	PCS_PRBS31_ABILITY (R)	Always reads 1. 1 = PCS is able to support PRBS31 pattern testing 0 = PCS is not able to support PRBS31 testing	
3.32.1	PCS_HI_BER (R)	1 = High BER condition detected 0 = High BER condition not detected	
3.32.0	PCS_BLOCK_LOCK (R)	1 = PCS locked to receive blocks 0 = PCS not locked to receive blocks	

Table 195: KR_PCS_STATUS_2

Device Address: 0x03	Register Address: 0x0021	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
3.33.15	PCS_BLOCK_LOCK_LL (R)	1 = PCS locked to receive blocks 0 = PCS not locked to receive blocks	RO/LL
3.33.14	PCS_HI_BER_LH (R)	1 = High BER condition detected 0 = High BER condition not detected	RO/LH
3.33.13:8	PCS_BER_COUNT[5:0] (R)	Value indicating number of times BER state machine enters BER_BAD_SH state	COR
3.33.7:0	PCS_ERR_BLOCK_COUNT[7:0] (R)	Value indicating number of times RX decode state machine enters RX_E state in functional mode. Same value is also reflected in 30.16 and reading either register clears the counter value.	COR

Table 196: PCS_TP_SEED_A0

Device Address: 0x03	Register Address: 0x0022	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
3.34.15:0	PCS_TP_SEED_A[15:0] (R)	Test pattern seed A bits 15-0	RW

Table 197: PCS_TP_SEED_A1

Device Address: 0x03	Register Address: 0x0023	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**

3.35.15:0	PCS_TP_SEED_A[31:16] (R)	Test pattern seed A bits 31-16	RW

Table 198: PCS_TP_SEED_A2

Device Address: 0x03	Register Address: 0x0024	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
3.36.15:0	PCS_TP_SEED_A[47:32] (R)	Test pattern seed A bits 47-32	RW

Table 199: PCS_TP_SEED_A3

Device Address: 0x03	Register Address: 0x0025	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
3.37.9:0	PCS_TP_SEED_A[57:48] (R)	Test pattern seed A bits 57-48	RW

Table 200: PCS_TP_SEED_B0

Device Address: 0x03	Register Address: 0x0026	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
3.38.15:0	PCS_TP_SEED_B[15:0] (R)	Test pattern seed B bits 15-0	RW

Table 201: PCS_TP_SEED_B1

Device Address: 0x03	Register Address: 0x0027	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
3.39.15:0	PCS_TP_SEED_B[31:16] (R)	Test pattern seed B bits 31-16	RW

Table 202: PCS_TP_SEED_B2

Device Address: 0x03	Register Address: 0x0028	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
3.40.15:0	PCS_TP_SEED_B[47:32] (R)	Test pattern seed B bits 47-32	RW

Table 203: PCS_TP_SEED_B3

Device Address: 0x03	Register Address: 0x0029	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
3.41.9:0	PCS_TP_SEED_B[57:48] (R)	Test pattern seed B bits 57-48	RW

Table 204: PCS_TP_CONTROL

Device Address: 0x03	Register Address: 0x002A	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
3.42.5	PCS_PRBS31_RX_TP_EN (R)	1 = Enable PRBS31 test pattern verification on receive path 0 = Normal operation (Default 1'b0)	RW
3.42.4	PCS_PRBS31_TX_TP_EN (R)	1 = Enable PRBS31 test pattern generation on transmit path 0 = Normal operation (Default 1'b0)	
3.42.3	PCS_TX_TP_EN (R)	1 = Enable transmit test pattern generation 0 = Normal operation (Default 1'b0)	
3.42.2	PCS_RX_TP_EN (R)	1 = Enable receive test pattern verification 0 = Normal operation (Default 1'b0)	
3.42.1	PCS_TP_SEL (R)	1 = Square wave test pattern 0 = Pseudo random test pattern (Default 1'b0)	
3.42.0	PCS_DP_SEL (R)	1 = 0'S data pattern 0 = LF data pattern (Default 1'b0)	

Table 205: PCS_TP_ERR_COUNT

Device Address: 0x03	Register Address: 0x002B	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
3.43.15:0	PCS_TP_ERR_COUNT[15:0] (R)	Test pattern error counter. This counter reflects number of errors occurred during the test pattern mode selected through PCS_TP_CONTROL. In PRBS31 test pattern verification mode, counter value indicates the number of received bytes that have 1 or more bit errors.	COR

Table 206: PCS_VS_CONTROL

Device Address: 0x03	Register Address: 0x8000	Default: 0x00B0	
Bit(s)	**Name**	**Description**	**Access**

3.32768.7:4	PCS_SQWAVE_N (R)	Sets number of repeating 0's followed by repeating 1's during square wave test pattern generation mode (Default 4'1011)	RW
3.32768.3	RESERVED SPARE (R)	For TI use only (Default 1'b0)	RW
3.32768.2	PCS_RX_DEC_CTRL_CHAR (R)	PCS RX Decode control character selection. Determines what control characters are passed 0 = A/K/R control characters are changed to Idles. Reserved characters passed through (Default 1'b0) 1 = A/K/R control characters are passed through as is	RW
3.32768.1	PCS_DESCR_DISABLE (R)	De-scrambler control in 10GKR RX PCS 1 = Disable descrambler 0 = Enable descrambler (Default 1'b0)	RW
3.32768.0	PCS_SCR_DISABLE (R)	Scrambler control in 10GKR TX PCS 1 = Disable scrambler 0 = Enable scrambler (Default 1'b0)	RW

Table 207: PCS_VS_STATUS

Device Address: 0x03	Register Address: 0x8010	Default: 0x00FD

Bit(s)	Name	Description	Access
3.32784.13	UNCORR_ERR_STATUS (R)	1 = Uncorrectable block error found	RO/LH
3.32784.12	CORR_ERR_STATUS (R)	1 = Correctable block error found	RO/LH
3.32784.8	PCS_TP_ERR (R)	PCS test pattern verification status 1 = Error occurred during pseudo random test pattern verification Number of errors can be checked by reading PCS_TP_ERR_COUNT (3.43) register	RO/LH
3.32784.7:0	RESERVED PCS_ENC_ERR_COUNT[7:0] (R)	For TI use only. PCS encoder error counter. This counter increment whenever following error condition occurs in the PCS encoder in 10GKR datapath. a) Invalid control codes b) Invalid "O" code c) Non existent corresponding block format for defined XGMII characters	COR

AUTO-NEGOTIATION REGISTERS

Below registers can be accessed only in Clause 45 mode and with device address field set to 0x07 (DA[4:0] = 5'b00111)

Table 208: AN_CONTROL

Device Address: 0x07	Register Address: 0x0000	Default: 0x3000

Bit(s)	Name	Description	Access
7.0.15	AN_RESET (RX)	1 = Resets Auto Negotiation 0 = Normal operation (Default 1'b0)	RW/SC
7.0.13	RESERVED (RX)	For TI use only (Default 1'b1)	RW
7.0.12	AN_ENABLE (RX)	1 = Enable Auto Negotiation (Default 1'b1) 0 = Disable Auto Negotiation	RW
7.0.9	AN_RESTART (RX)	1 = Restart Auto Negotiation 0 = Normal operation (Default 1'b0)	RW/SC

Table 209: AN_STATUS

Device Address: 0x07	Register Address: 0x0001	Default: 0x0088

Bit(s)	Name	Description	Access
7.1.9	AN_PAR_DET_FAULT (RX)	1 = Fault has been detected via parallel detection function 0 = Fault has not been detected via parallel detection function	RO/LH
7.1.7	AN_EXP_NP_STATUS (RX)	1 = Extended next page is used 0 = Extended next page is not allowed	RO
7.1.6	AN_PAGE_RCVD (RX)	1 = A page has been received 0 = A page has not been received	RO/LH
7.1.5	AN_COMPLETE (RX)	1 = Auto Negotiation process is completed 0 = Auto Negotiation process not completed	RO
7.1.4	REMOTE_FAULT (RX)	1 = Remote fault detected by AN 0 = Remote fault not detected by AN	RO/LH
7.1.3	AN_ABILITY (RX)	Always reads 1. 1 = Device is able to perform Auto Negotiation 0 = Device not able to perform Auto Negotiation	RO
7.1.2	LINK_STATUS (RX)	1 = Link is up 0 = Link is down	RO/LL
7.1.0	AN_LP_ABILITY (RX)	1 = LP is able to perform Auto Negotiation 0 = LP not able to perform Auto Negotiation	RO

Table 210: AN_DEV_PACKAGE

Device Address: 0x07	Register Address: 0x0005	Default: 0x0080

Bit(s)	Name	Description	Access
7.5.7	AN_PRESENT (RX)	Always reads 1 1 = Auto Negotiation present in the package 0 = Auto Negotiation not present in the package	RO

Table 211: AN_ADVERTISEMENT_1

Device Address: 0x07	Register Address: 0x0010	Default: 0x1001	
Bit(s)	**Name**	**Description**	**Access**
7.16.15	AN_NEXT_PAGE (RX)	NP bit (D15) in base link codeword 1 = Next page available 0 = Next page not available (Default 1'b0)	RW
7.16.14	AN_ACKNOWLEDGE (RX)	Acknowledge bit (D14) in base link codeword. Always reads 0.	RO
7.16.13	AN_REMOTE_FAULT (RX)	RF bit (D13) in base link codeword 1 = Sets RF bit to 1 0 = Normal operation (Default 1'b0)	RW
7.16.12:10	AN_CAPABILITY[2:0] (RX)	Value to be set in D12:D10 bits of the base link codeword. Consists of abilities like PAUSE, ASM_DIR (Default 3'b100)	RW
7.16.9:5	AN_ECHO_NONCE[4:0] (RX)	Value to be set in D9:D5 bits of the base link codeword. Consists of Echo nonce value. Transmitted in base page only until local device and link Partner have exchanged unique Nonce values, at which time transmitted Echoed Nonce will change to Link Partner's Nonce value. Read value always reflects the value written, not the actual Echoed Nonce. (Default 5'b00000)	RW
7.16.4:0	AN_SELECTOR[4:0] (RX)	Value to be set in D4:D0 bits of the base link codeword. Consists of selector field value (Default 5'b00001)	RW

Table 212: AN_ADVERTISEMENT_2

Device Address: 0x07	Register Address: 0x0011	Default: 0x0080	
Bit(s)	**Name**	**Description**	**Access**
7.17.15:8	AN_ABILITY[10:3] (RX)	Value to be set in D31:D24 bits of the base link codeword. Consists of technology ability field bits [10:3] (Default 9'b000000000)	RW
7.17.7	AN_ABILITY[2] (RX)	Value to be set in D23 bits of the base link codeword. Consists of technology ability field bits [2]. When set, indicates device supports 10GBASE-KR (Default 1'b1)	
7.17.6	AN_ABILITY[1] (RX)	Value to be set in D22 bits of the base link codeword. Consists of technology ability field bits [1]. Always set to 0 (Default 1'b0)	
7.17.5	AN_ABILITY[0] (RX)	Value to be set in D21 bits of the base link codeword. Consists of technology ability field bit [0]. When set, indicates device supports 1000BASE-KX (Default 1'b0)	
7.17.4:0	AN_TRANS_NONCE_FIELD[4:0] (RX)	Not used. Transmitted Nonce field is generated by hardware random number generator. Read value always reflects value written, not the actual Transmitted Nonce (Default 5'b00000)	

Table 213: AN_ADVERTISEMENT_3

Device Address: 0x07	Register Address: 0x0012	Default: 0x4000	
Bit(s)	**Name**	**Description**	**Access**
7.18.15	AN_FEC_REQUESTED (RX)	Value to be set in D47 bits of the base link codeword. When set, indicates a request to enable FEC on the link (Default 1'b0)	RW
7.18.14	AN_FEC_ABILITY (RX)	Value to be set in D46 bits of the base link codeword. When set, indicates 10GBASE-KR has FEC ability (Default 1'b1)	
7.18.13:0	AN_ABILITY[24:11] (RX)	Value to be set in D45:D32 bits of the base link codeword. Consists of technology ability field bits [24:11] (Default 14'b00000000000000)	

Table 214: AN_LP_ADVERTISEMENT_1[16]

Device Address: 0x07	Register Address: 0x0013	Default: 0x0001	
Bit(s)	**Name**	**Description**	**Access**
7.19.15	AN_LP_NEXT_PAGE (RX)	NP bit (D15) in link partner base page 1 = Next page available in link partner 0 = Next page not available in link partner	RO
7.19.14	AN_LP_ACKNOWLEDGE (RX)	Acknowledge bit (D14) in link partner base page.	
7.19.13	AN_LP_REMOTE_FAULT (RX)	RF bit (D13) in link partner base page 1 = Remote fault detected in link partner 0 = Remote fault not detected in link partner	
7.19.12:10	AN_ LP_CAPABILITY (RX)	D12:D10 bits of the link partner base page. Consists of abilities like PAUSE, ASM_DIR	
7.19.9:5	AN_ LP_ECHO_NONCE (RX)	D9:D5 bits of the link partner base page. Consists of Echo nonce value	
7.19.4:0	AN_LP_SELECTOR[4:0] (RX)	D4:D0 bits of the link partner base page. Consists of selector field value Always reads 5'b00001	

Table 215: AN_LP_ADVERTISEMENT_2

Device Address: 0x07	Register Address: 0x0014	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
7.20.15:8	AN_ LP_ABILITY[10:3] (RX)	D31:D24 bits of the link partner base page. Consists of technology ability field bits [10:3]	RO
7.20.7	AN_LP_ABILITY[2] (RX)	D23 bits of the link partner base page. Consists of technology ability field bits [2]. When high, indicates link partner supports 10GBASE-KR	
7.20.6	AN_LP_ABILITY[1] (RX)	D22 bits of the link partner base page. Consists of technology ability field bits [1].	

[16] To get accurate AN_LP_ADVERTISEMENT read value, Register 7.19 should be read first before reading 7.20 and 7.21

7.20.5	AN_LP_ABILITY[0] (RX)	D21 bits of the link partner base page. Consists of technology ability field bit [0]. When high, indicates link partner supports 1000BASE-KX	
7.20.4:0	AN_LP_TRANS_NONCE_FIELD (RX)	D20:D16 bits of the link partner base page. Consists of transmitted nonce value	

Table 216: AN_LP_ADVERTISEMENT_3

Device Address: 0x07	Register Address: 0x0015	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
7.21.15	AN_LP_FEC_REQUESTED (RX)	D47 bits of the link partner base page. When high, indicates link partner request to enable FEC on the link	RO
7.21.14	AN_LP_FEC_ABILITY (RX)	D46 bits of the link partner base page. When high, indicates link partner has FEC ability	
7.21.13:0	AN_LP_ABILITY[24:11] (RX)	D45:D32 bits of the link partner base page. Consists of link partner technology ability field bits [24:11]	

Table 217: AN_XNP_TRANSMIT_1

Device Address: 0x07	Register Address: 0x0016	Default: 0x2000	
Bit(s)	**Name**	**Description**	**Access**
7.22.15	AN_XNP_NEXT_PAGE (RX)	NP bit (D15) in next page code word 1 = Next page available 0 = Next page not available (Default 1'b0)	RW
7.22.14	RESERVED (RX)	Always reads 0.	RO
7.22.13	AN_MP (RX)	Message page bit (D13) in next page code word 1 = Sets MP bit to 1 indicating next page is a message page (Default 1'b1) 0 = Sets MP bit to 0 indicating next page is unformatted next page	RW
7.22.12	AN_ACKNOWLEDGE_2 (RX)	Value to be set in D12 bit of the next page code word. When set, indicates device is able to act on the information defined in the message (Default 1'b0)	RW
7.22.11	AN_TOGGLE (RX)	Not used. Toggle value is generated by hardware. Read value always reflects value written, not the actual Toggle field (Default 1'b0)	RW
7.22.10:0	AN_CODE_FIELD (RX)	Value to be set in D10:D0 bits of the next page code word. Consists of Message/Unformatted code field value (Default 11'b00000000000)	RW

Table 218: AN_XNP_TRANSMIT_2

Device Address: 0x07	Register Address: 0x0017	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**

7.23.15:0	AN_MSG_CODE_1 (RX)	Value to be set in D31:D16 bits of the next page code word. Consists of Message/Unformatted code field value (Default 16'b0000000000000000)	RW

Table 219: AN_XNP_TRANSMIT_3

Device Address: 0x07	Register Address: 0x0018	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
7.24.15:0	AN_MSG_CODE_2 (RX)	Value to be set in D47:D32 bits of the next page code word. Consists of Message/Unformatted code field value (Default 16'b0000000000000000)	RW

Table 220: AN_LP_XNP_ABILITY_1[17]

Device Address: 0x07	Register Address: 0x0019	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
7.25.15	AN_LP_XNP_NEXT_PAGE (RX)	NP bit (D15) in next page code word 1 = Next page available 0 = Next page not available (Default 1'b0)	RO
7.25.14	AN_LP_XNP_ACKNOWLEDGE (RX)	Value in D14 bit of the next page code word. When set, indicates device is able to act on the information defined in the message (Default 1'b0)	
7.25.13	AN_LP_MP (RX)	Message page bit (D13) in next page code word 1 = Sets MP bit to 1 indicating next page is a message page 0 = Sets MP bit to 0 indicating next page is unformatted next page (Default 1'b0)	
7.25.12	AN_LP_ACKNOWLEDGE_2 (RX)	Value in D12 bit of the next page code word. When set, indicates device is able to act on the information defined in the message (Default 1'b0)	
7.25.11	AN_LP_TOGGLE (RX)	Value of D11 bit of the next page code word. Consists of Toggle field value(Default 1'b0)	
7.25.10:0	AN_ LP_CODE_FIELD (RX)	Value in D10:D0 bits of the next page code word. Consists of Message/Unformatted code field value (Default 11'b00000000000)	

Table 221: AN_LP_XNP_ABILITY_2

Device Address: 0x07	Register Address: 0x001A	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
7.26.15:0	AN_LP_MSG_CODE_1 (RX)	Value to be set in D31:D16 bits of the next page code word. Consists of Message/Unformatted code field value (Default 16'b0000000000000000)	RO

[17] To get accurate AN_LP_XNP_ABILITYT read value, Register 7.25 should be read first before reading 7.26 and 7.27

Table 222: AN_LP_XNP_ABILITY_3

Device Address: 0x07	Register Address: 0x001B	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
7.27.15:0	AN_LP_MSG_CODE_2 (RX)	Value to be set in D47:D32 bits of the next page code word. Consists of Message/Unformatted code field value (Default 16'b0000000000000000)	RO

Table 223: AN_BP_STATUS

Device Address: 0x07	Register Address: 0x0030	Default: 0x0001	
Bit(s)	**Name**	**Description**	**Access**
7.48.4	AN_10G_KR_FEC (RX)	1 = PMA/PMD is negotiated to perform 10GBASE-KR FEC	RO
7.48.3	AN_10G_KR (RX)	1 = PMA/PMD is negotiated to perform 10GBASE-KR	
7.48.1	AN_1G_KX (RX)	1 = PMA/PMD is negotiated to perform 1000BASE-KX	
7.48.0	AN_BP_AN_ABILITY (RX)	Always reads 1. 1 = Indicates 1000BASE-KX, 10GBASE-KR is implemented	

Table 224: AN_VS_CONTROL

Device Address: 0x07	Register Address: 0x8000	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
7.32768.1	RESERVED AN_SKIP_NONCE (RX)	For TI use only. (Default 1'b0) 1 = Skip nonce check. Should be set when data is looped back within the same channel (HS TX -> HS RX) either internally (deep local loopback) or externally 0 = Normal operation (Default 1'b0)	RW
7.32768.0	RESERVED AN_SIM_MODE_EN (RX)	For TI use only. (Default 1'b0) 1 = Enable mode to speed up simulation 0 = Normal operation (Default 1'b0)	