Schematic Review Form

Tejas Networks FPC402 Schematic Review

Pin #	Name	Info	Violations	*Description*
32	CAPL	Good		Connect a single 2.2-µF capacitor to GND
23	CTRL1	Good		Host-side control interface. These pins are used to implement I2C or SPI depending on the PROTOCOL_SEL pin configuration. I2C mode (PROTOCOL_SEL = Float or High): CTRL1: SCL – I2C Clock input / open-drain output CTRL2: SDA – I2C Data input / open-drain output CTRL3: SET_ADDR_N – input, address assignment enable. Also used to receive external LED clock. CTRL4: ADDR_DONE_N – output, address assignment complete. Also used to transmit LED clock. SPI mode (PROTOCOL_SEL = GND): CTRL1: SCK – Serial clock input CTRL2: SS_N – Active-low slave select input CTRL3: MOSI – Master output or slave input CTRL4: MISO – Master input or slave output
24	CTRL2	Good		Host-side control interface. These pins are used to implement I2C or SPI depending on the PROTOCOL_SEL pin configuration. I2C mode (PROTOCOL_SEL = Float or High): CTRL1: SCL – I2C Clock input / open-drain output CTRL2: SDA – I2C Data input / open-drain output CTRL3: SET_ADDR_N – input, address assignment enable. Also used to receive external LED

				clock. CTRL4: ADDR_DONE_N – output, address assignment complete. Also used to transmit LED clock. SPI mode (PROTOCOL_SEL = GND): CTRL1: SCK – Serial clock input CTRL2: SS_N – Active-low slave select input CTRL3: MOSI – Master output or slave input CTRL4: MISO – Master input or slave output
28	CTRL3	Good		Host-side control interface. These pins are used to implement I2C or SPI depending on the PROTOCOL_SEL pin configuration. I2C mode (PROTOCOL_SEL = Float or High): CTRL1: SCL – I2C Clock input / open-drain output CTRL2: SDA – I2C Data input / open-drain output CTRL3: SET_ADDR_N – input, address assignment enable. Also used to receive external LED clock. CTRL4: ADDR_DONE_N – output, address assignment complete. Also used to transmit LED clock. SPI mode (PROTOCOL_SEL = GND): CTRL1: SCK – Serial clock input CTRL2: SS_N – Active-low slave select input CTRL3: MOSI – Master output or slave input CTRL4: MISO – Master input or slave output
21	CTRL4		Given that CTRL4 is an output, I don't think it makes sense to short this to GND. This can be left floating.	Host-side control interface. These pins are used to implement I2C or SPI depending on the PROTOCOL_SEL pin configuration. I2C mode (PROTOCOL_SEL = Float or High): CTRL1: SCL – I2C Clock input / open-drain output CTRL2: SDA – I2C Data input / open-drain output

				CTRL3: SET_ADDR_N – input, address assignment enable. Also used to receive external LED clock. CTRL4: ADDR_DONE_N – output, address assignment complete. Also used to transmit LED clock. SPI mode (PROTOCOL_SEL = GND): CTRL1: SCK – Serial clock input CTRL2: SS_N – Active-low slave select input CTRL3: MOSI – Master output or slave input CTRL4: MISO – Master input or slave output
22	EN	Good, pulled high		Device enable. When EN = 0, the FPC402 is in a power-down state and does not respond to the host-side control bus, nor does it perform port-side I2C accesses. When EN=VDD2 or Float, the FPC402 is fully enabled and will respond to the host-side control bus provided VDD1 and VDD2 power has been stable for at least TPOR. VIH for this pin is referenced to VDD2. The minimum required assert and deassert time is 12.5 µs.
19, 8, 53, 42	GPIO[3:0]	Good		General-purpose I/O. Output high voltage (VOH) and input high voltage (VIH) are based on VDD1. Configured as input (high-Z) by default.
27, DAP	GND	Good		Ground reference. The GND pins must be connected through a low-resistance path to the board GND plane.
25	HOST_INT_N	Good		Open-drain 3.3-V tolerant active-low interrupt output. It asserts low to interrupt the host. The events which trigger an interrupt are programmable through registers. This pin can be connected in a wired-OR fashion with other FPC402s' interrupt pins. A single pullup resistor to

				VDD1 or VDD2 in the 2-kΩ to 5-kΩ range is adequate for the entire net.
10, 55, 50, 41	IN_A[3:0]	Good		Low-speed port status input A. Example usage: SFP: Mod_ABS[3:0] QSFP: ModPrsL[3:0]
12, 1, 47, 39	IN_B[3:0]	Good		Low-speed port status input B. Example usage: SFP: Tx_Fault[3:0] QSFP: IntL[3:0]
14, 3, 46, 37	IN_C[3:0]	Good		Low-speed port status input C. Example usage: SFP: Rx_LOS[3:0] QSFP: N/A
15, 4, 49, 36	MOD_SCL[3:0]	Good		I2C clock open-drain output to the module. External 2-kΩ to 5-kΩ pullup resistor is required. This pin is 3.3-V LVCMOS tolerant.
16, 5, 48, 35	MOD_SDA[3:0]	Good		I2C data input or open-drain output to the module. External 2-kΩ to 5-kΩ pullup resistor is required. This pin is 3.3-V LVCMOS tolerant.
11, 56, 44, 40	OUT_A[3:0]	Good		Low-speed port control output A. OUT_A is disabled by default (high-Z) and when enabled drives high logic unless reprogrammed. A 10-kΩ pullup or pulldown resistor is recommended to set a default logic value before this output is enabled. See Section 8.3.3 for more details. Example usage: SFP: Tx_Disable[3:0] QSFP: ResetL[3:0]
13, 2, 45, 38	OUT_B[3:0]	Good		Low-speed port control output B. Output is disabled by default (high-Z) and when enabled drives low logic unless reprogrammed. A 10-kΩ pullup or pulldown resistor is recommended to set a default logic value before this output is enabled. See Section 8.3.3 for more details. Example usage:

				SFP: RS[3:0] QSFP: LPMode[3:0]
17, 6, 51, 34	OUT_C[3:0]	Good		Low-speed port control output C. Can be used to drive port status LED. Special LED driving features are available on this output. This output is enabled and high logic by default at power up. See Section 8.3.2 for more details. Example usage: SFP: LED_GRN[3:0] QSFP: LED_GRN[3:0] This pin requires a series resistor with a value of at least 33 Ω. The LED current-limiting resistor can serve for this purpose.
18, 7, 52, 33	OUT_D[3:0]	Good		Low-speed port control output D. Can be used to drive port status LED. Special LED driving features are available on this output. This output is enabled and high logic by default at power up. See Section 8.3.2 for more details. Example usage: SFP: LED_YLW[3:0] QSFP: N/A This pin requires a series resistor with a value of at least 33 Ω. The LED current-limiting resistor can serve for this purpose.
31	PROTOCOL_SEL	Good		Used to select between I2C and SPI host-side control interface. Float or High: Inter-IC Control (I2C) GND: Serial Peripheral Interface (SPI)
30	SPI_LED_SYNC	Good		LED clock synchronization pin for SPI mode only. When using SPI as the host-side control interface (PROTOCOL_SEL=GND), connect all FPC402 SPI_LED_CLK pins together. This ensures LED synchronization across all FPC402 devices. When using I2C as the host-side control

				interface, this pin can be floating. LED synchronization is ensured by other means in I2C mode.
29	TEST_N	Good		TI test mode. Float or High: Normal operation GND: TI Test Mode
9, 43, 54	VDD1	Good		Main power supply, VDD1 = 3.3 V ± 5%. TI recommends connecting at least one 1-µF and one 0.1-µF decoupling capacitors per VDD1 pin as close to the pin as possible.
20, 26	VDD2	Good		Power supply for host-side interface I/Os (CTRL[4:1]). VDD2 can be 1.8 V to 3.3 V ± 5%. If the host-side interface operates at 3.3 V, then VDD1 and VDD2 can be connected to the same 3.3-V ± 5% supply. TI recommends connecting at least one 1-µF and one 0.1-µF decoupling capacitors per VDD2 pin as close to the pin as possible.

Comments