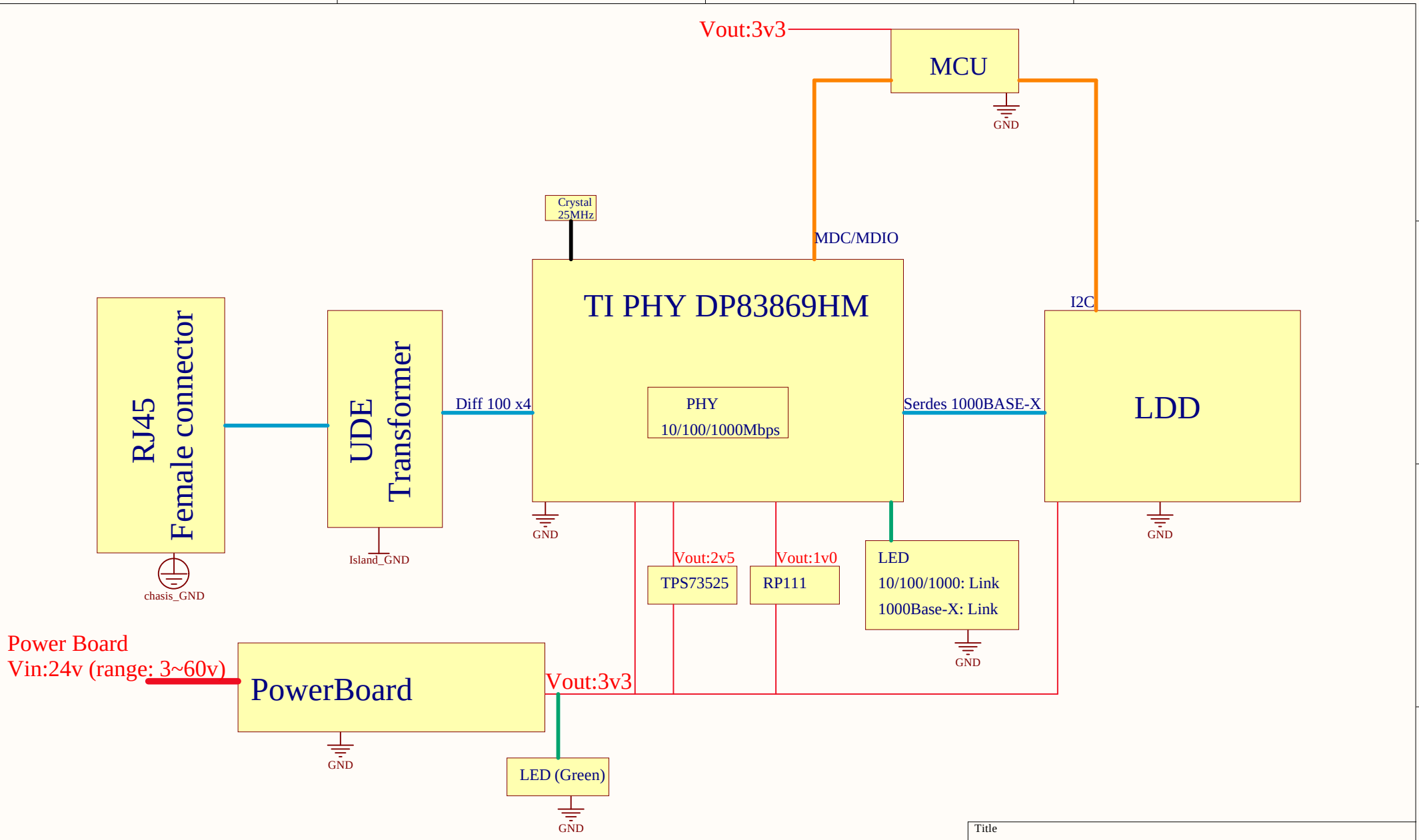

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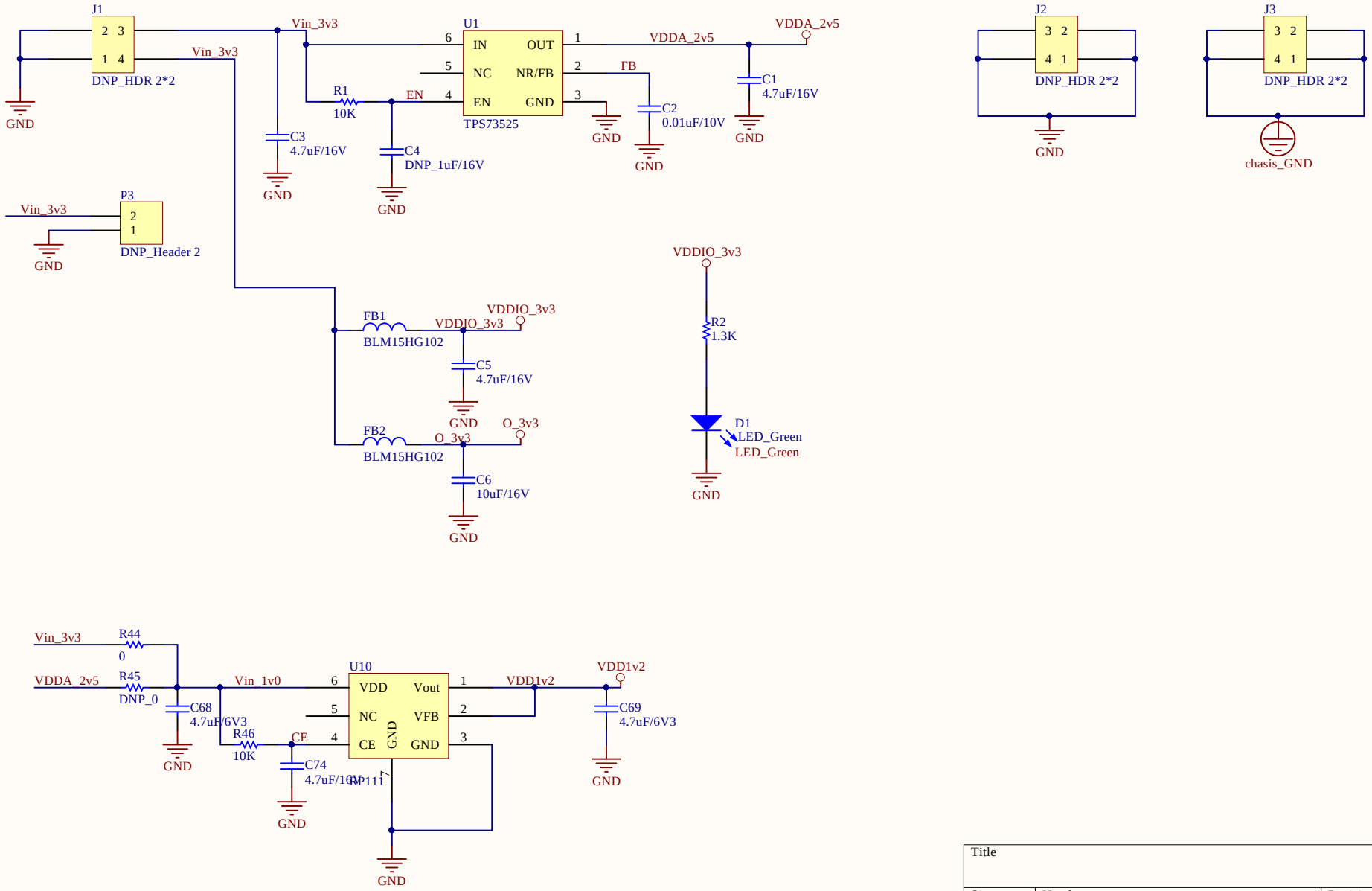

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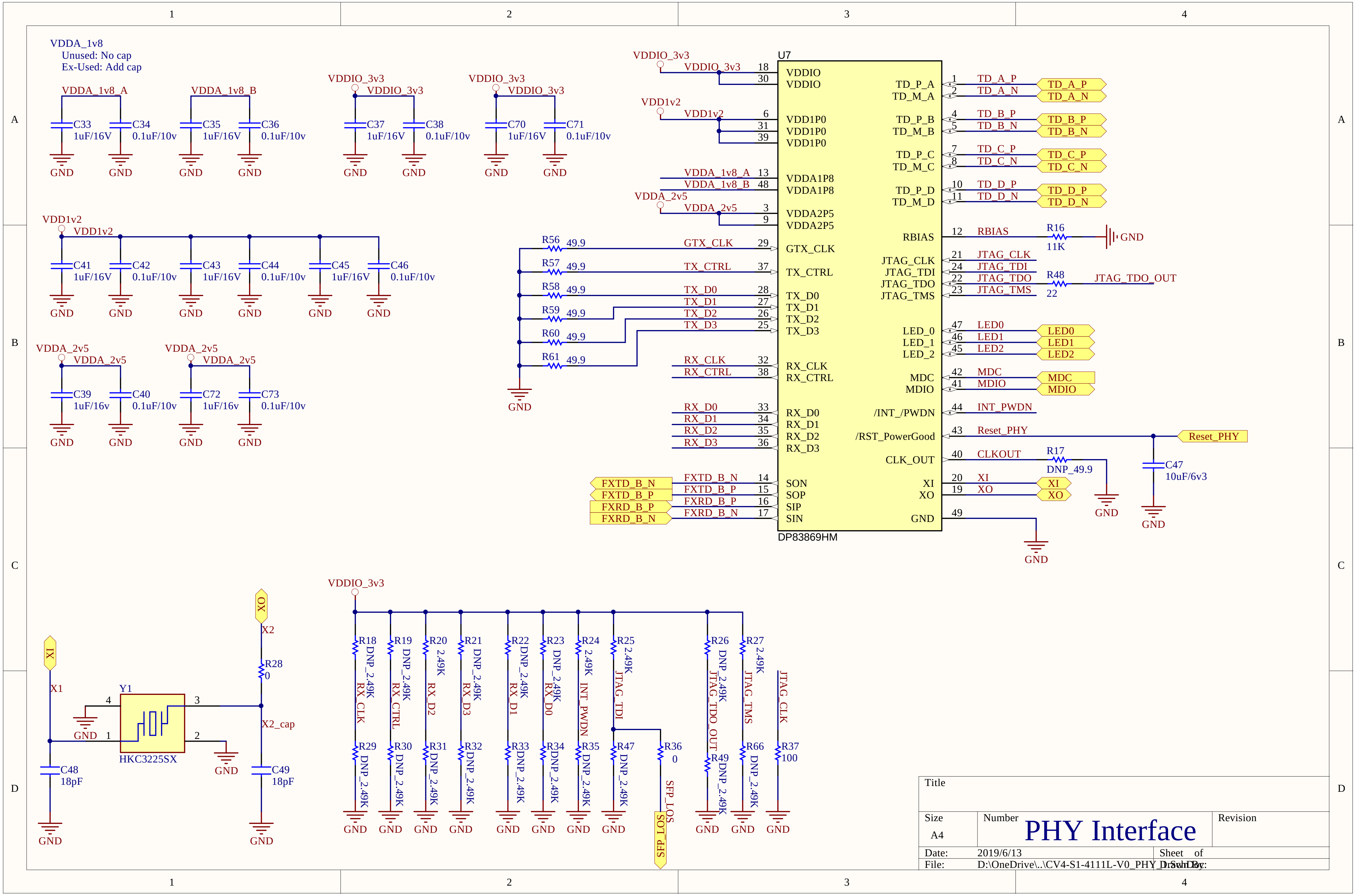

VDDA_1v8
Unused: No cap
Ex-Used: Add cap
VDDA_1v8_A
C33 1uF/16V
C34 0.1uF/10v
VDDA_1v8_B
C35 1uF/16V
C36 0.1uF/10v
VDDIO_3v3
C37 1uF/16V
C38 0.1uF/10v
C70 1uF/16V
C71 0.1uF/10v
VDD1v2
C41 1uF/16V
C42 0.1uF/10v
C43 1uF/16V
C44 0.1uF/10v
C45 1uF/16V
C46 0.1uF/10v
VDDA_2v5
C39 1uF/16v
C40 0.1uF/10v
C72 1uF/16v
C73 0.1uF/10v
GND
U7
DP83869HM
VDDIO
VDD1P0
VDDA1P8
VDDA2P5
GTX_CLK
TX_CTRL
TX_D0
TX_D1
TX_D2
TX_D3
RX_CLK
RX_CTRL
RX_D0
RX_D1
RX_D2
RX_D3
SON
SOP
SIP
SIN
TD_P_A
TD_M_A
TD_P_B
TD_M_B
TD_P_C
TD_M_C
TD_P_D
TD_M_D
RBIAS
JTAG_CLK
JTAG_TDI
JTAG_TDO
JTAG_TMS
LED_0
LED_1
LED_2
MDC
MDIO
/INT_/PWDN
/RST_PowerGood
CLK_OUT
XI
XO
TD_A_P
TD_A_N
TD_B_P
TD_B_N
TD_C_P
TD_C_N
TD_D_P
TD_D_N
R16 11K
R48 22
JTAG_TDO_OUT
LED0
LED1
LED2
INT_PWDN
Reset_PHY
CLKOUT
R17 DNP_49.9
C47 10uF/6v3
R56 49.9
R57 49.9
R58 49.9
R59 49.9
R60 49.9
R61 49.9
FXTD_B_N
FXTD_B_P
FXRD_B_P
FXRD_B_N
X1
X2
Y1
HKC3225SX
R28 0
X2_cap
C48 18pF
C49 18pF
R18 DNP_2.49K
R19 DNP_2.49K
R20 2.49K
R21 DNP_2.49K
R22 DNP_2.49K
R23 DNP_2.49K
R24 2.49K
R25 2.49K
R26 DNP_2.49K
R27 2.49K
R29 DNP_2.49K
R30 DNP_2.49K
R31 DNP_2.49K
R32 DNP_2.49K
R33 DNP_2.49K
R34 DNP_2.49K
R35 DNP_2.49K
R47 DNP_2.49K
R36 0
R49 DNP_2.49K
R66 DNP_2.49K
R37 100
SFP_LOS
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PHY Interface
Size A4
Number
Revision
Date: 2019/6/13
Sheet of
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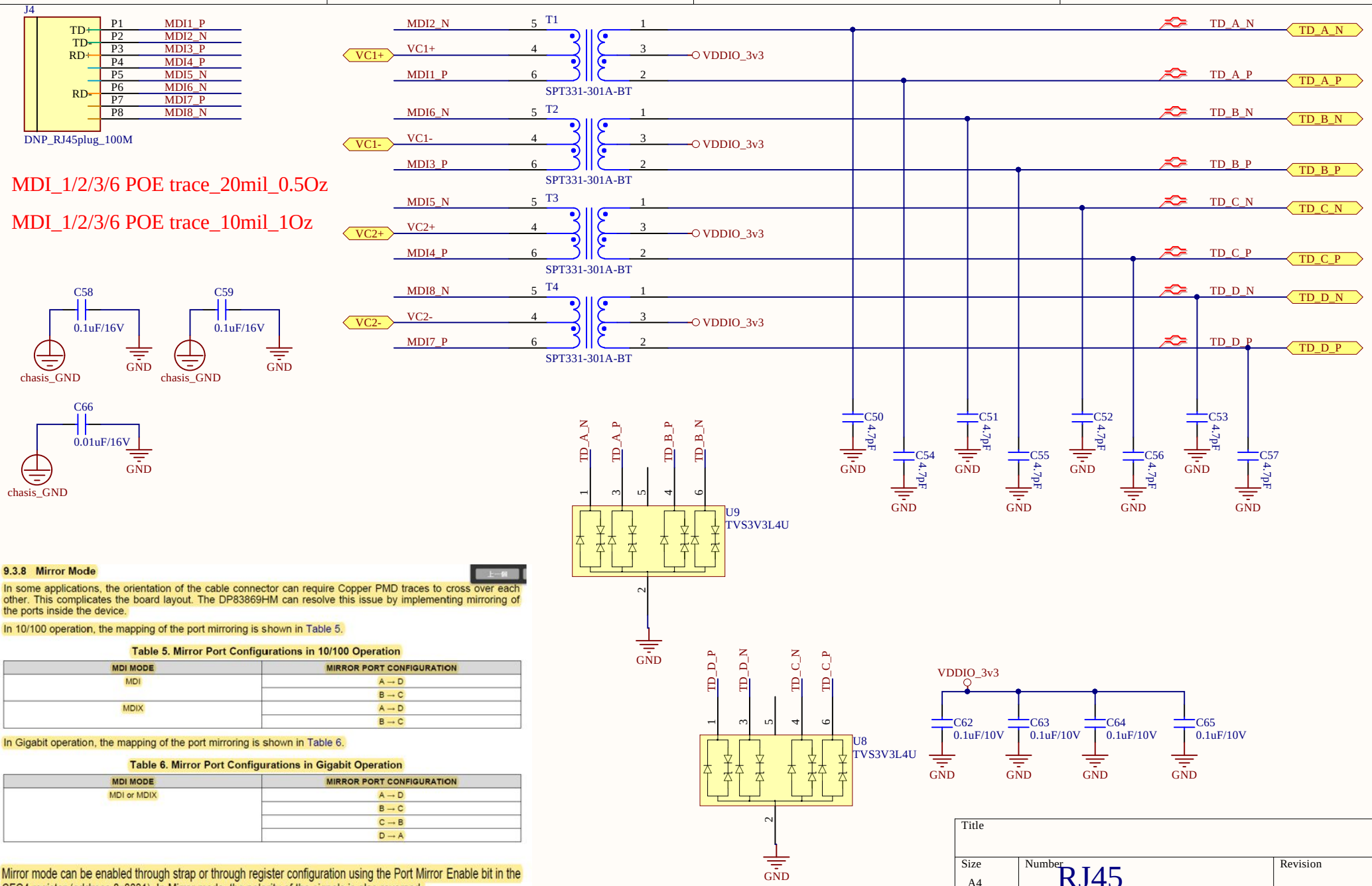

9.3.8 Mirror Mode

In some applications, the orientation of the cable connector can require Copper PMD traces to cross over each other. This complicates the board layout. The DP83869HM can resolve this issue by implementing mirroring of the ports inside the device.

In 10/100 operation, the mapping of the port mirroring is shown in Table 5.

Table 5. Mirror Port Configurations in 10/100 Operation

MDI MODE	MIRROR PORT CONFIGURATION
MDI	A → D
	B → C
MDIX	A → D
	B → C

In Gigabit operation, the mapping of the port mirroring is shown in Table 6.

Table 6. Mirror Port Configurations in Gigabit Operation

MDI MODE	MIRROR PORT CONFIGURATION
MDI or MDIX	A → D
	B → C
	C → B
	D → A

Mirror mode can be enabled through strap or through register configuration using the Port Mirror Enable bit in the CFG4 register (address 0x0031). In Mirror mode, the polarity of the signals is also reversed.

Title		
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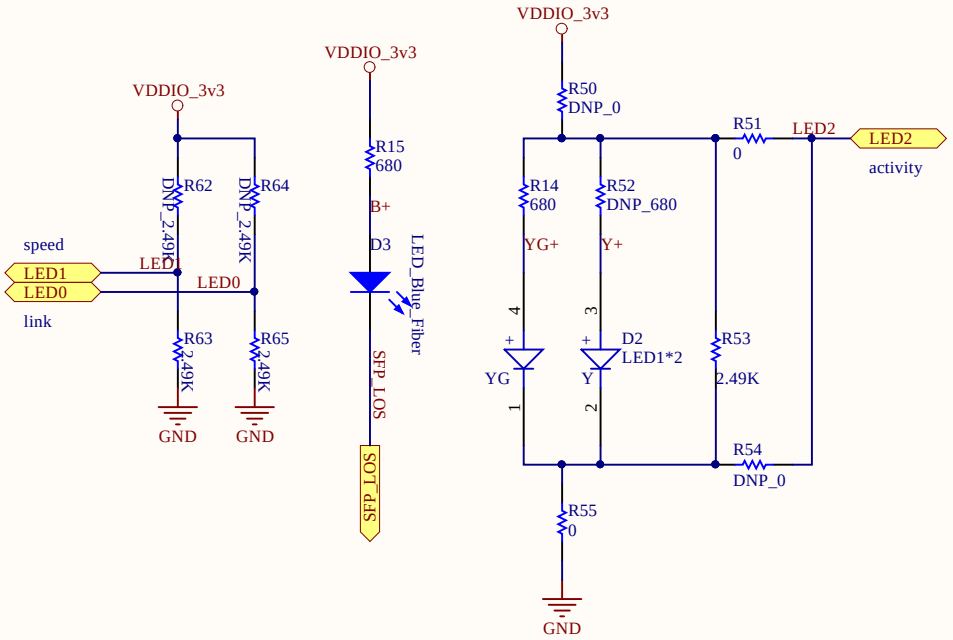

LED2:1011b_link OK + blink on TX/RX activity

9.6.1.23 LEDS_CFG1 Register (Address = 0x18) [reset = 0x6150]

LEDS_CFG1 is shown in Figure 47 and described in Table 44.

Return to Summary Table.

Figure 47. LEDS_CFG1 Register

15	14	13	12	11	10	9	8
LED_GPIO_SEL				LED_ACT_SEL			
R/W-4b0110				R/W-4b0001			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LED_SPD_SEL				LED_LNK_SEL			
R/W-4b0101				R/W-4b0000			

Table 44. LEDS_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	LED_GPIO_SEL	R/W	4b0000	Source of GPIO LED, same as bits 3:0
11-8	LED_ACT_SEL	R/W	4b0000	Source of ACTIVITY LED (LED 2) , same as bits 3:0
7-4	LED_SPD_SEL	R/W	4b0000	Source of SPEED LED (LED 1) , same as bits 3:0
3-0	LED_LNK_SEL	R/W	4b0000	Source of LINK LED (LED 0) 0000b = link OK 0001b = RX/TX activity 0010b = TX activity 0011b = RX activity 0100b = collision detected 0101b = 1000BT link is up 0110b = 100 BTX link is up 0111b = 10BT link is up 1000b = 10/100BT link is up 1001b = 100/1000BT link is up 1010b = full duplex 1011b = link OK + blink on TX/RX activity 1100b = EEE mode 1101b = RX_ER or TX_ER 1110b = RX_ER

		Pin name	strap name	Pin#	Default	ANEGSEL_1 LED_2	ANEGSEL_0 LED_1	
100 Mbps media converter	100 Base-FX	LED_1	ANEGSEL_0	46	0	0	0	Copper : Auto-negotiation (100/10 Advertised), Auto MDIX
		LED_2	ANEGSEL_1	45	0	1	1	Copper : Auto Negotiation (100 Advertised), Auto MDIX
		RX_CTRL	MIRROR_EN	38	0	0		Copper: Mirror Disable
						1		Copper: Mirror Enable
		RX_CLK	LINK_LOSS	32	0	0		Link Loss Pass Thru Enabled
						1		Link Loss Pass Thru Disabled
	100Mbps	JTAG_TDO/GPIO_1	OPMODE_0	22	2.49K pull-up to VDDIO			
		RX_D3	OPMODE_1	36	OPEN			
		RX_D2	OPMODE_2	35	2.49K pull-up to VDDIO			
	Register setting	1. Register 0x01DF will contain 0x0045 for 100 Mbps Media Converter mode.						
		2. Required register configuration for 100 Mbps Media Converter mode: - Write 0x1FFC to register 0x01EC (set bit [0] to 0)						

		Pin name	strap name	Pin#	Default			
1000 Mbps media converter		LED_0	ANEG_DIS	47	0	0		Fiber Auto Negotiation
						1		Fiber Force Mode
	1000 Base-X					ANEGSEL_1 LED_2	ANEGSEL_0 LED_1	
		LED_1	ANEGSEL_0	46	0	0	0	Copper : Auto-negotiation (1000/100 Advertised), Auto MDIX
		LED_2	ANEGSEL_1	45	0	1	1	Copper : Auto Negotiation (1000 Advertised), Auto MDIX
	1000Mbps	JTAG_TDO/GPIO_1	OPMODE_0	22	OPEN			
		RX_D3	OPMODE_1	36	OPEN			
		RX_D2	OPMODE_2	35	2.49K pull-up to VDDIO			
	Register setting	1. Register 0x01DF will contain 0x0044 for 1000 Mbps Media Converter mode.						
		2. Required register configuration for 1000 Mbps Media Converter mode: - Write 0x1FFC to register 0x01EC (set bit [0] to 0)						

Title			
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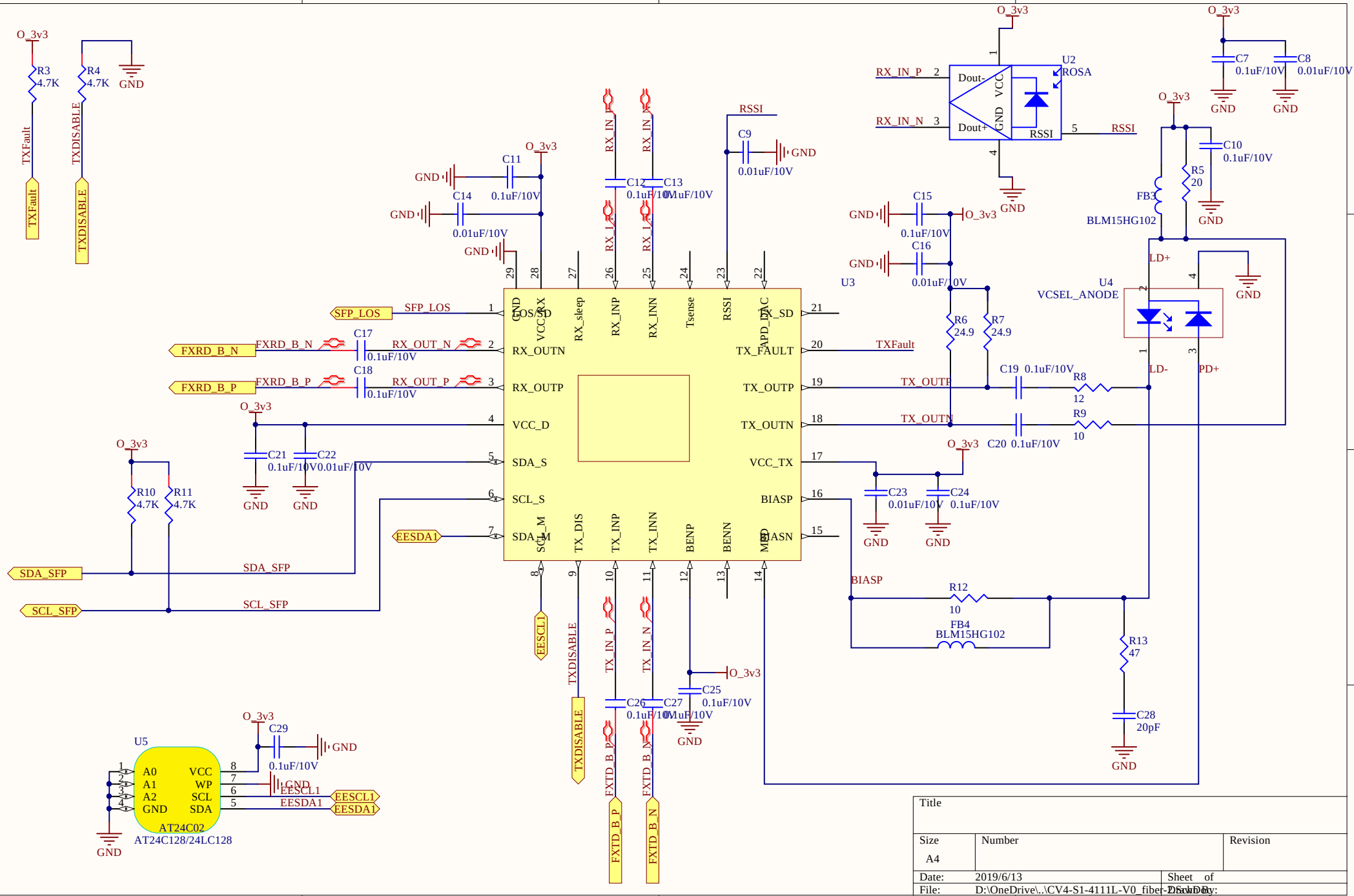
O_3v3
R3 4.7K
R4 4.7K
GND
TXFault
TXDISABLE
U2 ROSA
RX_IN_P
RX_IN_N
Dout-
Dout+
VCC
GND
RSSI
C7 0.1uF/10V
C8 0.01uF/10V
C9 0.01uF/10V
C10 0.1uF/10V
C11 0.1uF/10V
C12 0.1uF/10V
C13 0.1uF/10V
C14 0.01uF/10V
C15 0.1uF/10V
C16 0.01uF/10V
R5 20
FB3 BLM15HG102
U3
U4 VCSEL_ANODE
LD+
LD-
PD+
R6 24.9
R7 24.9
R8 12
R9 10
C19 0.1uF/10V
C20 0.1uF/10V
C21 0.1uF/10V
C22 0.01uF/10V
C23 0.01uF/10V
C24 0.1uF/10V
C25 0.1uF/10V
C26 0.1uF/10V
C27 0.1uF/10V
C28 20pF
R10 4.7K
R11 4.7K
R12 10
R13 47
FB4 BLM15HG102
SFP_LOS
FXRD_B_N
FXRD_B_P
RX_OUT_N
RX_OUT_P
TX_FAULT
TX_OUTP
TX_OUTN
SDA_SFP
SCL_SFP
EESDA1
EESCL1
TXDISABLE
FXTD_B_P
FXTD_B_N
BIASP
VCC_TX
U5
AT24C02
AT24C128/24LC128
A0
A1
A2
WP
SCL
SDA
EESCL1
EESDA1
Title
Size
A4
Number
Revision
Date: 2019/6/13
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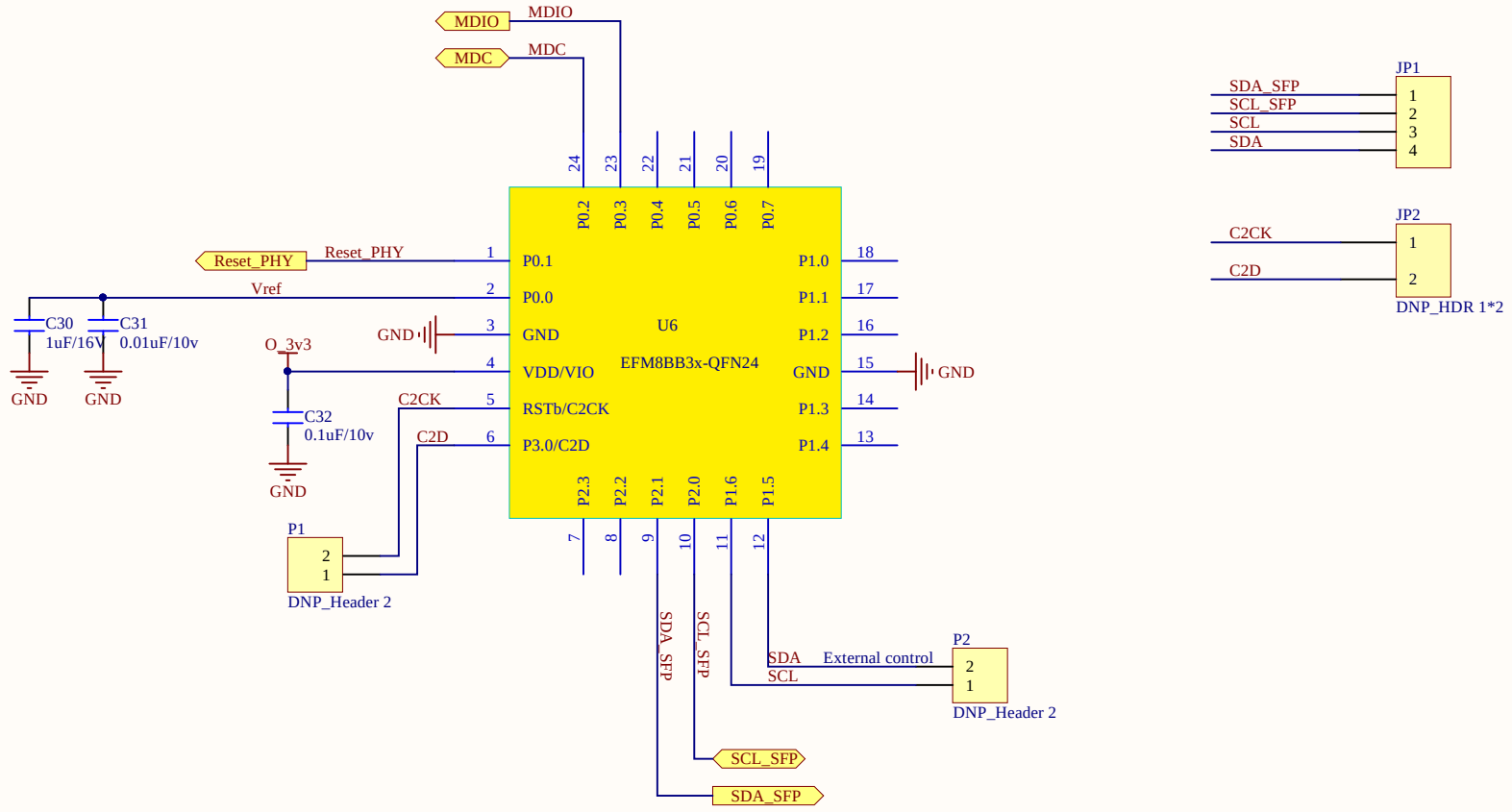

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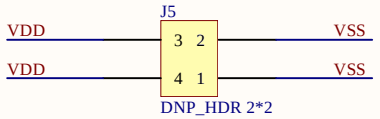

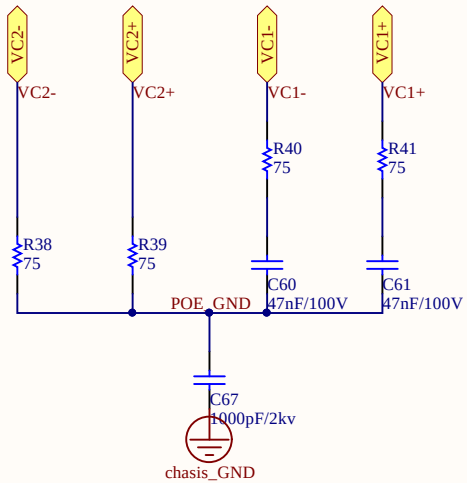

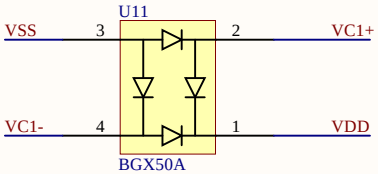

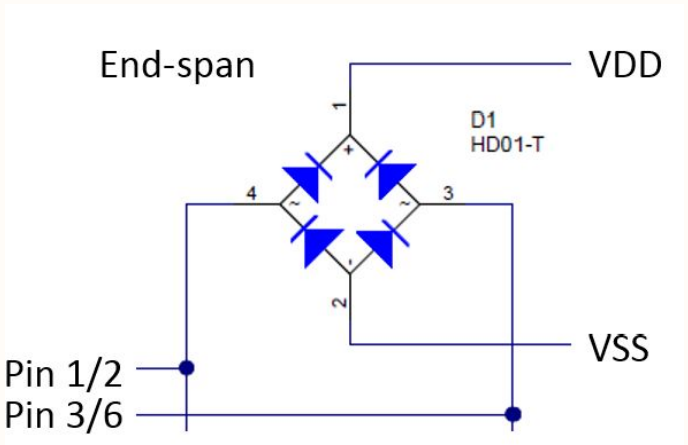

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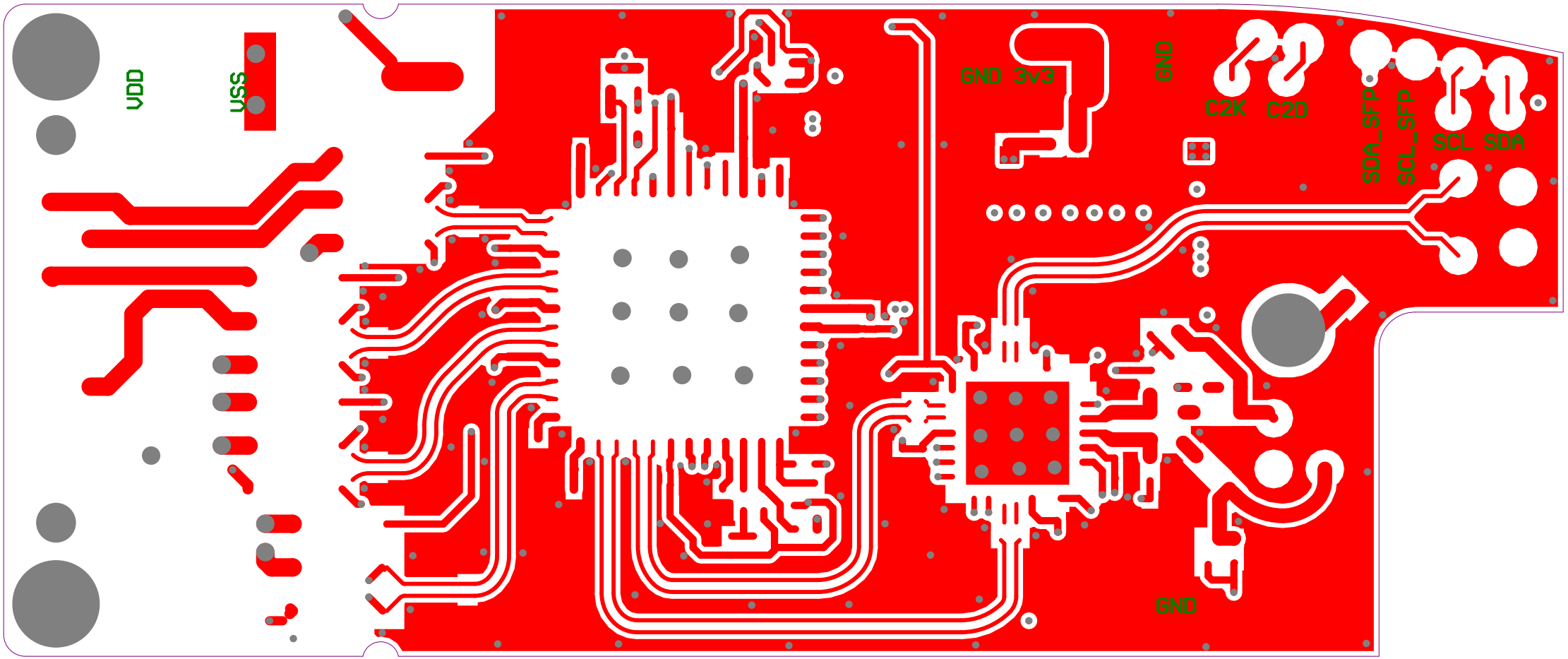
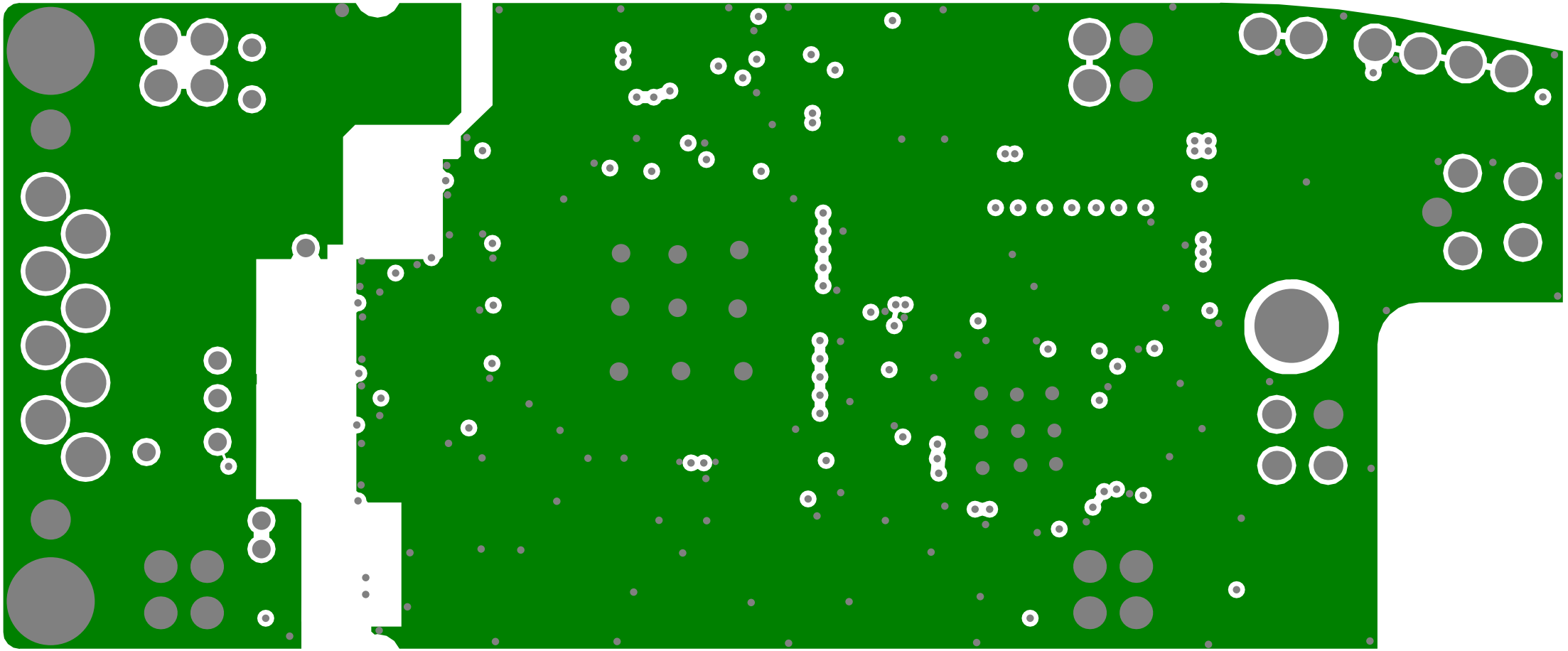
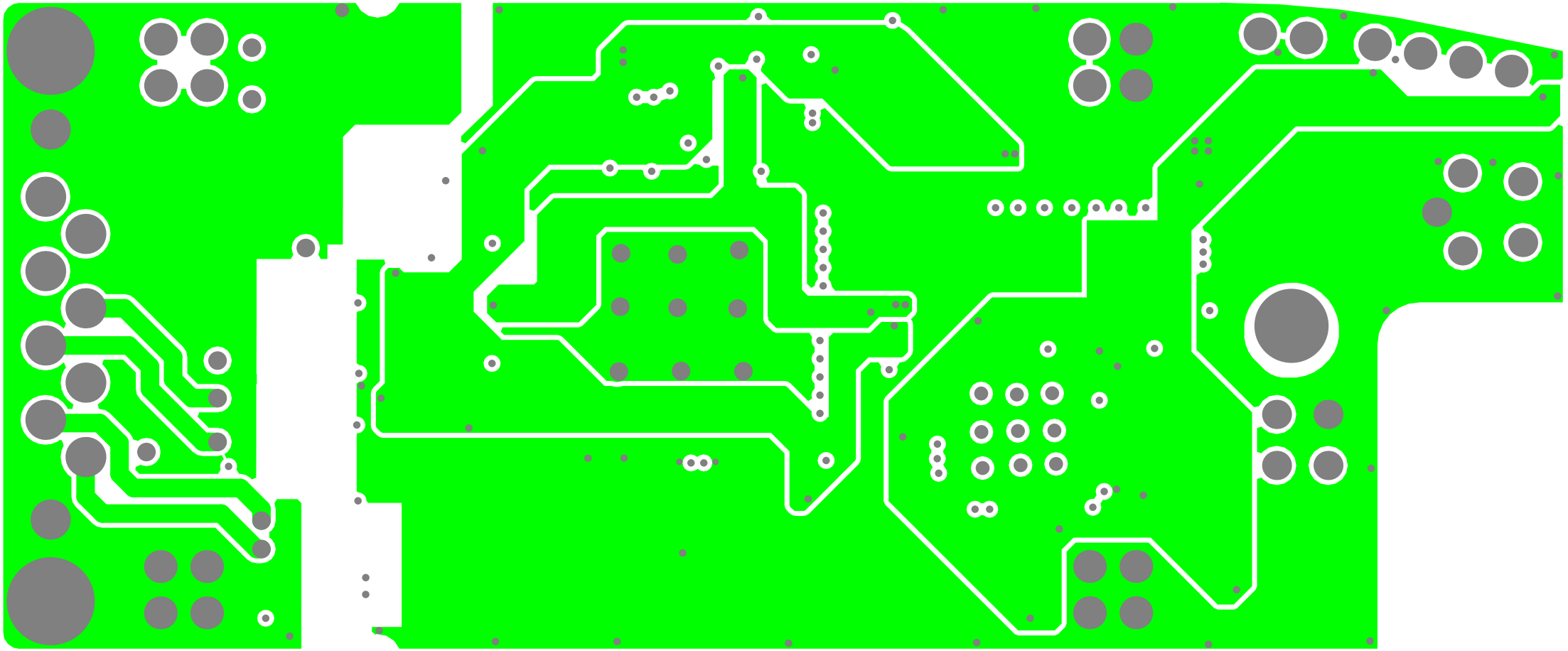
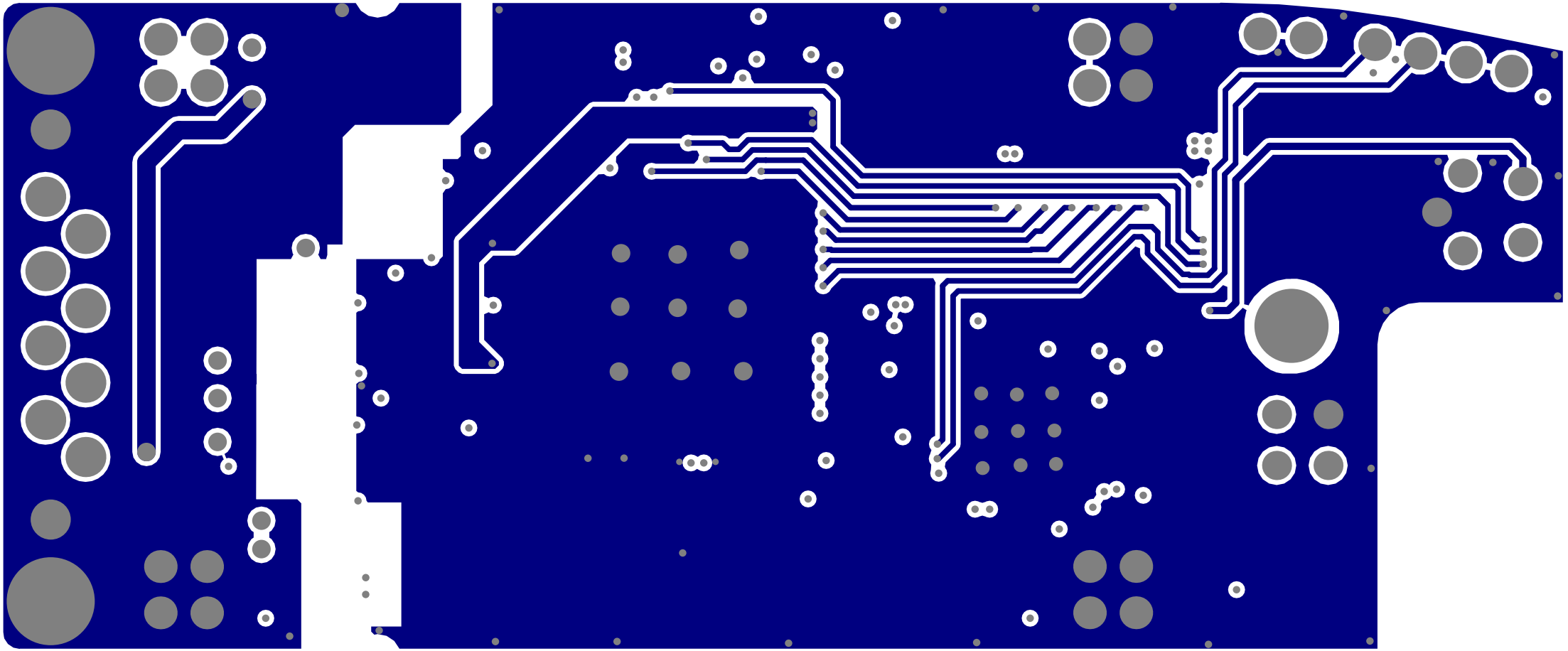
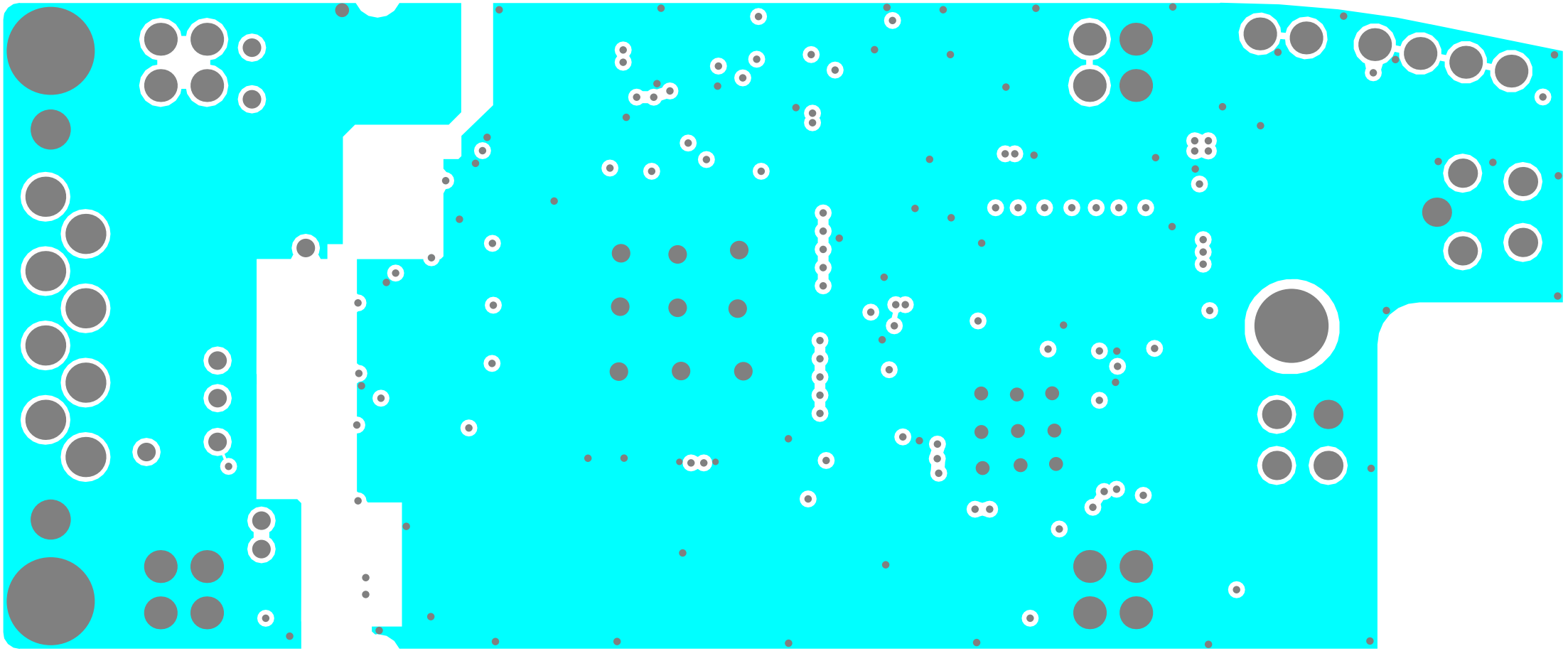
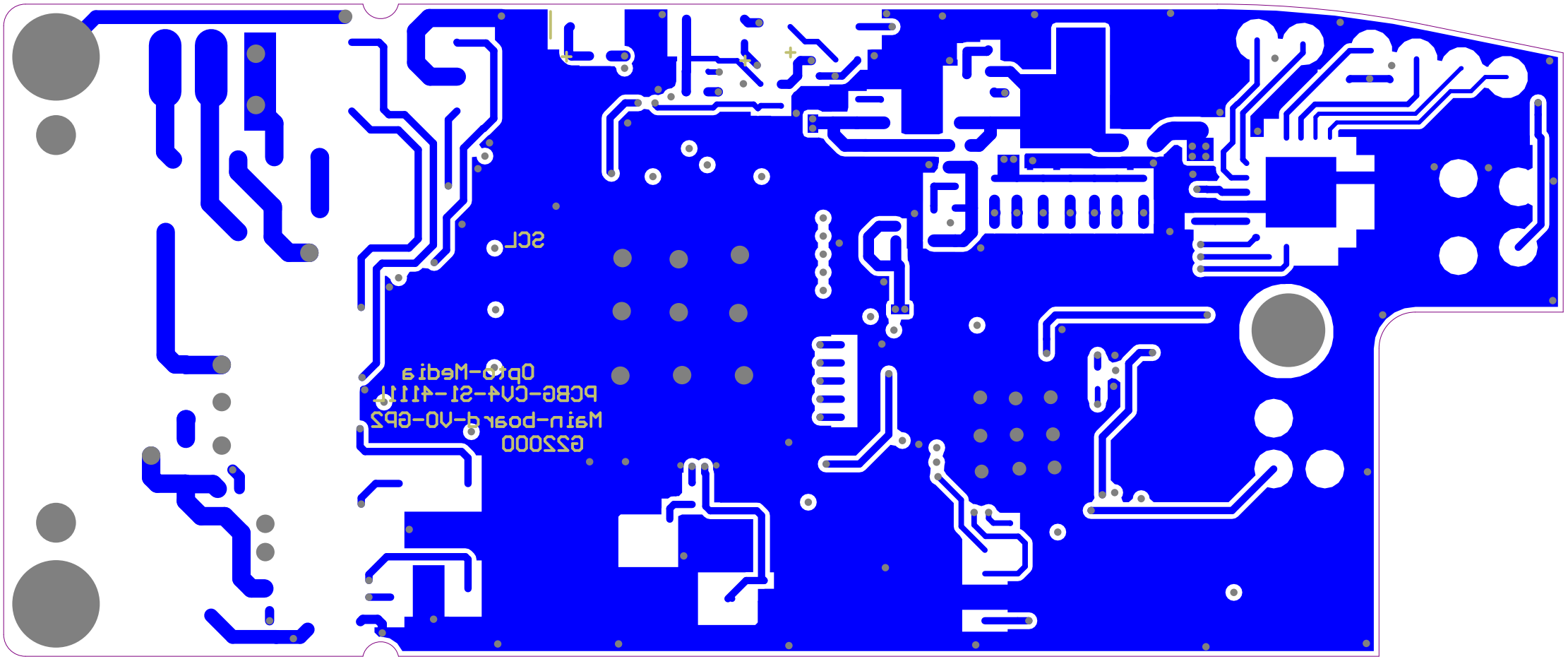

VDD
VSS
GND
3v3
GND
C2K
C2D
SDA_SFP
SCL_SFP
SCL
SDA
GND







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PCB6-CV4-SI-4111
Main-board-V0-6P2
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