DATA BOOK
PACKAGE OUTLINE

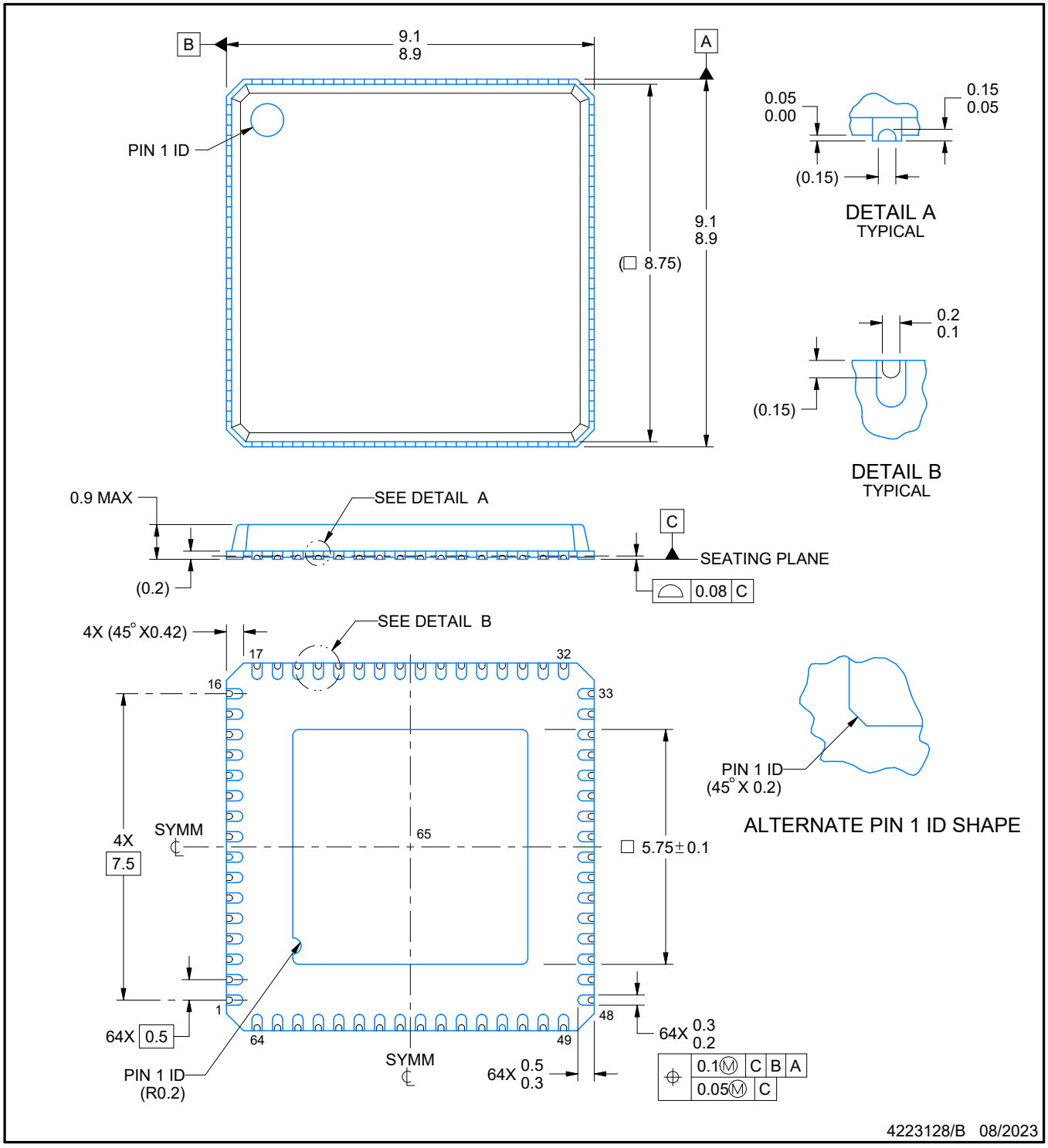
DRAFTER: K. SINCERBOX	DATE: 08/02/2016					DIMENSIONS IN MILLIMETERS	
DESIGNER:	DATE:	TEXAS INSTRUMENTS SEMICONDUCTOR OPERATIONS				CODE IDENTITY NUMBER 01295	
CHECKER: K. SINCERBOX	DATE: 08/31/2023						
ENGINEER: R. JAVIER	DATE: 08/31/2023	ePOD, RTD0064F / VQFN, 64 PIN, 0.5 MM PITCH					
APPROVED: K. SINCERBOX	DATE: 08/31/2023						
RELEASED: K. SINCERBOX	DATE: 08/31/2023						
TEMPLATE INFO: EDGE# 4218519	DATE: 04/07/2016	SCALE NTS	SIZE A	4223128		REV B	PAGE 1 OF 5

RTD0064F

PACKAGE OUTLINE

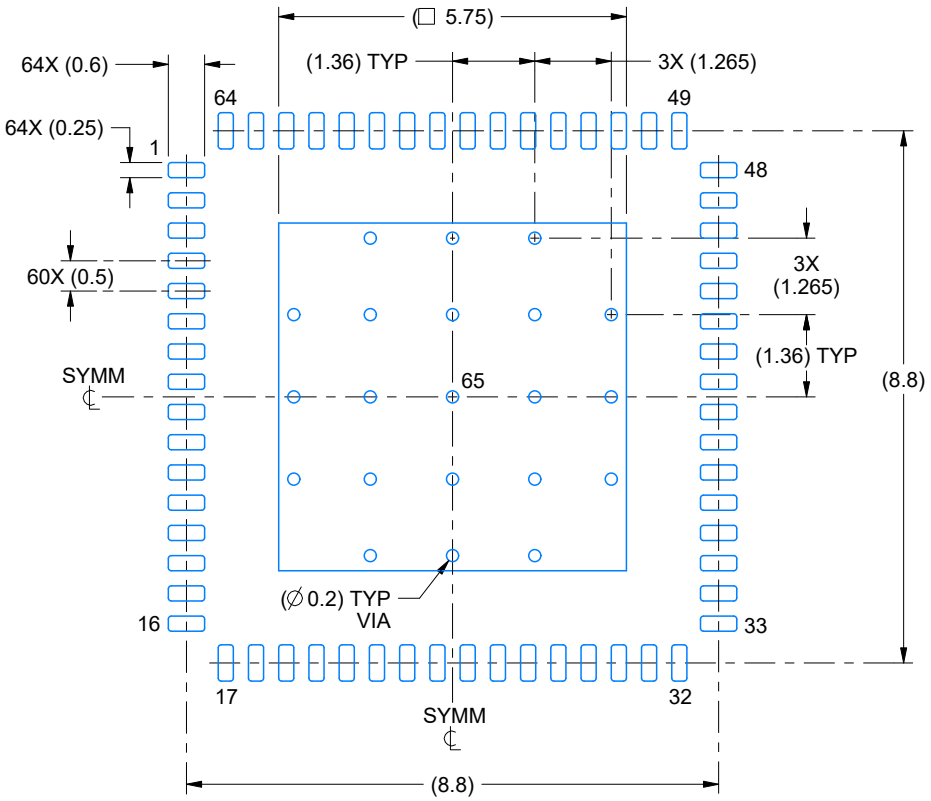
VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

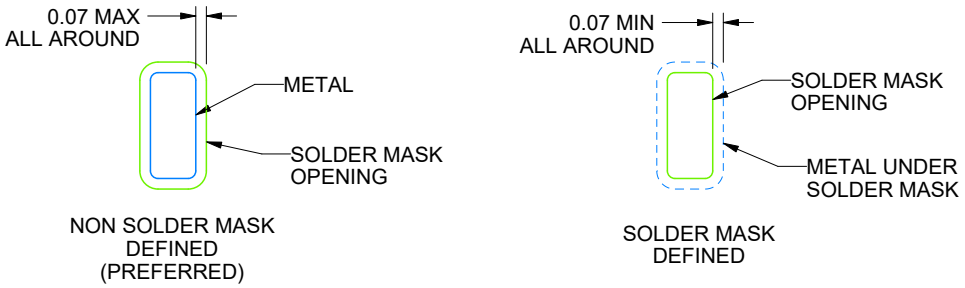


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

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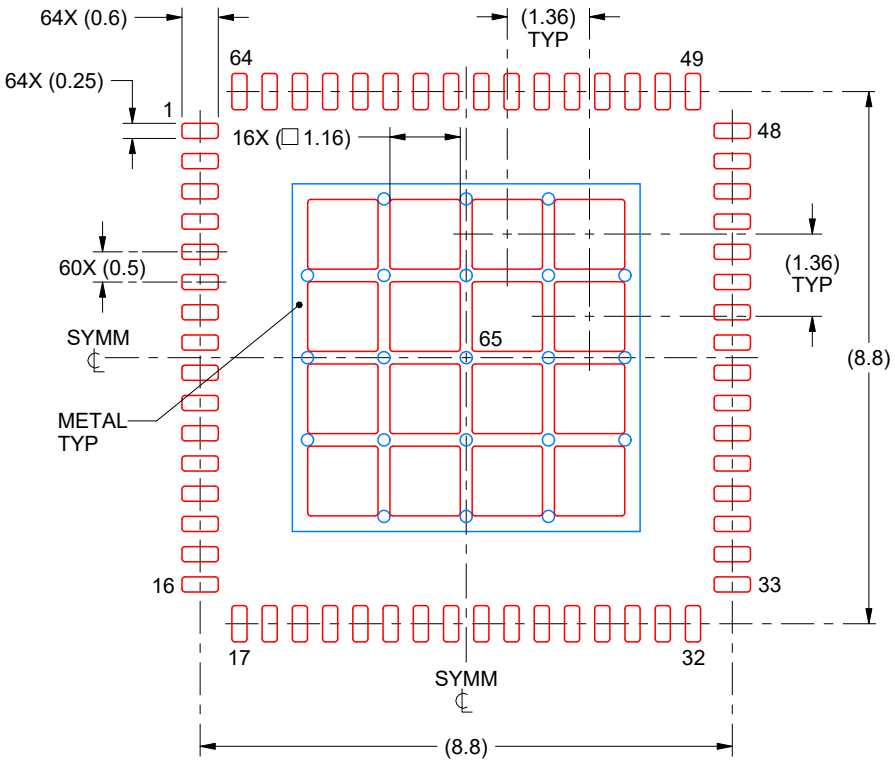
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 65:
65% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:8X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

REVISIONS

REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTER
A	RELEASE NEW DRAWING	2158960	08/02/2016	F.MORTAN / K. SINCERBOX
B	ADD ALTERNATE PIN 1 ID SHAPE DETAIL	2205528	08/31/2023	R. JAVIER / K. SINCERBOX