

REVISIONS

ECR	ECR NUMBER	DATE
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NOTES:

1. SILKSCREEN ALL JUMPERS AND HEADERS.
2. PLACE ALL PARTS ON A 0 OR 90 DEGREE ORIENTATION.
3. HIGH SPEED SERIAL DATA SHOULD BE ROUTED AS SINGLE-ENDED 50 OHM TRANSMISSION LINES. ROUTING DISTANCE SHOULD BE 3 INCHES OR LESS.
4. USE FR4-370 MATERIAL.
5. PLACE TI LOGO IN TOP SIDE METAL

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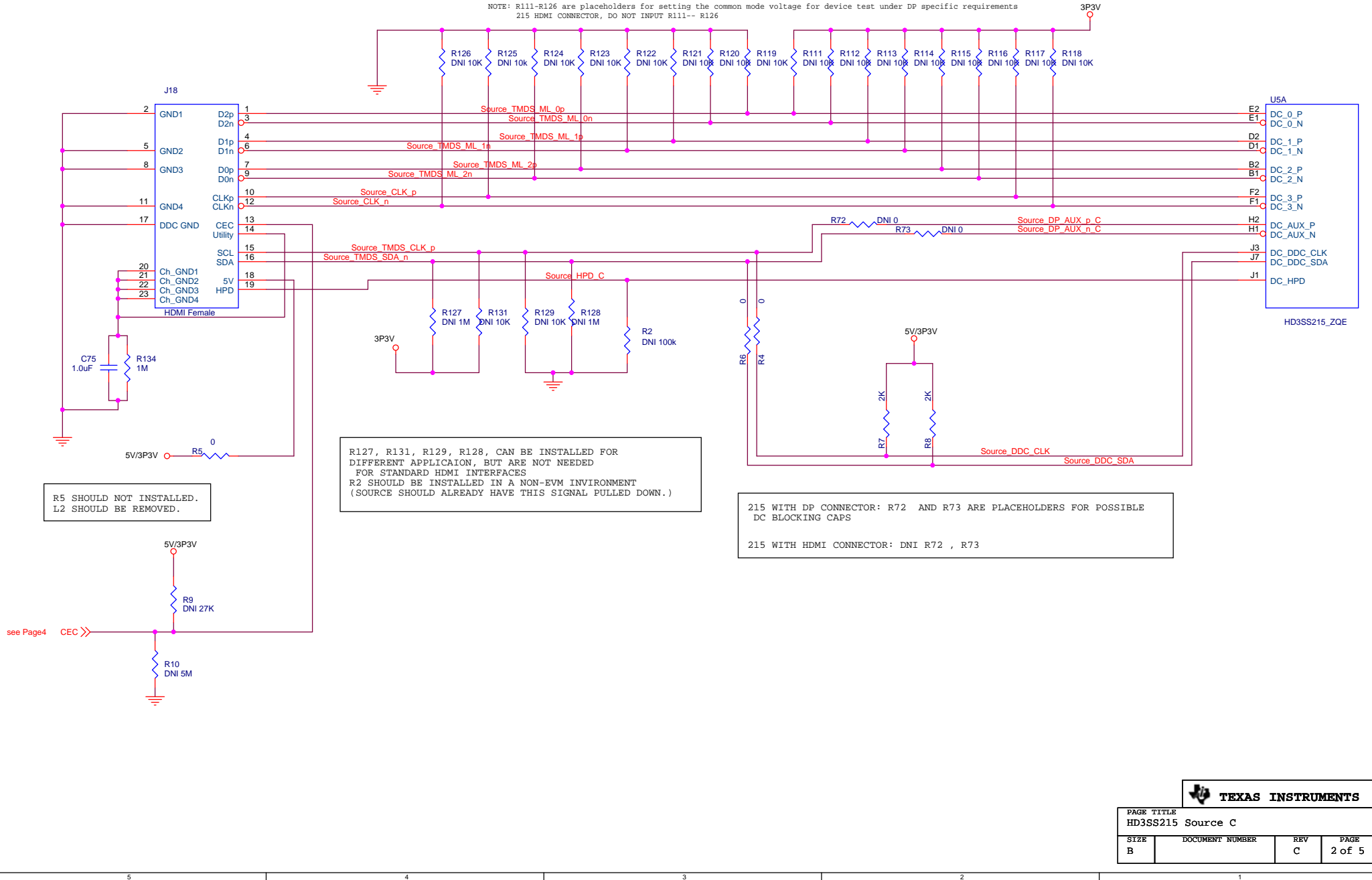


**TEXAS INSTRUMENTS**

SCHEMATIC TITLE  
 HD3SS21X\_1\_2MUX

ENGINEER	DATE	PAGE TITLE			
	11/08/13				
LAYOUT	DATE	SIZE	DOCUMENT NUMBER	REV	SHEET
		B		C	1 of 5
RELEASED	DATE				

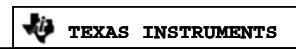
NOTE: R111-R126 are placeholders for setting the common mode voltage for device test under DP specific requirements  
 215 HDMI CONNECTOR, DO NOT INPUT R111-- R126



R5 SHOULD NOT INSTALLED.  
 L2 SHOULD BE REMOVED.

R127, R131, R129, R128, CAN BE INSTALLED FOR DIFFERENT APPLICAION, BUT ARE NOT NEEDED FOR STANDARD HDMI INTERFACES  
 R2 SHOULD BE INSTALLED IN A NON-EVM INVIROMENT (SOURCE SHOULD ALREADY HAVE THIS SIGNAL PULLED DOWN.)

215 WITH DP CONNECTOR: R72 AND R73 ARE PLACEHOLDERS FOR POSSIBLE DC BLOCKING CAPS  
 215 WITH HDMI CONNECTOR: DNI R72 , R73



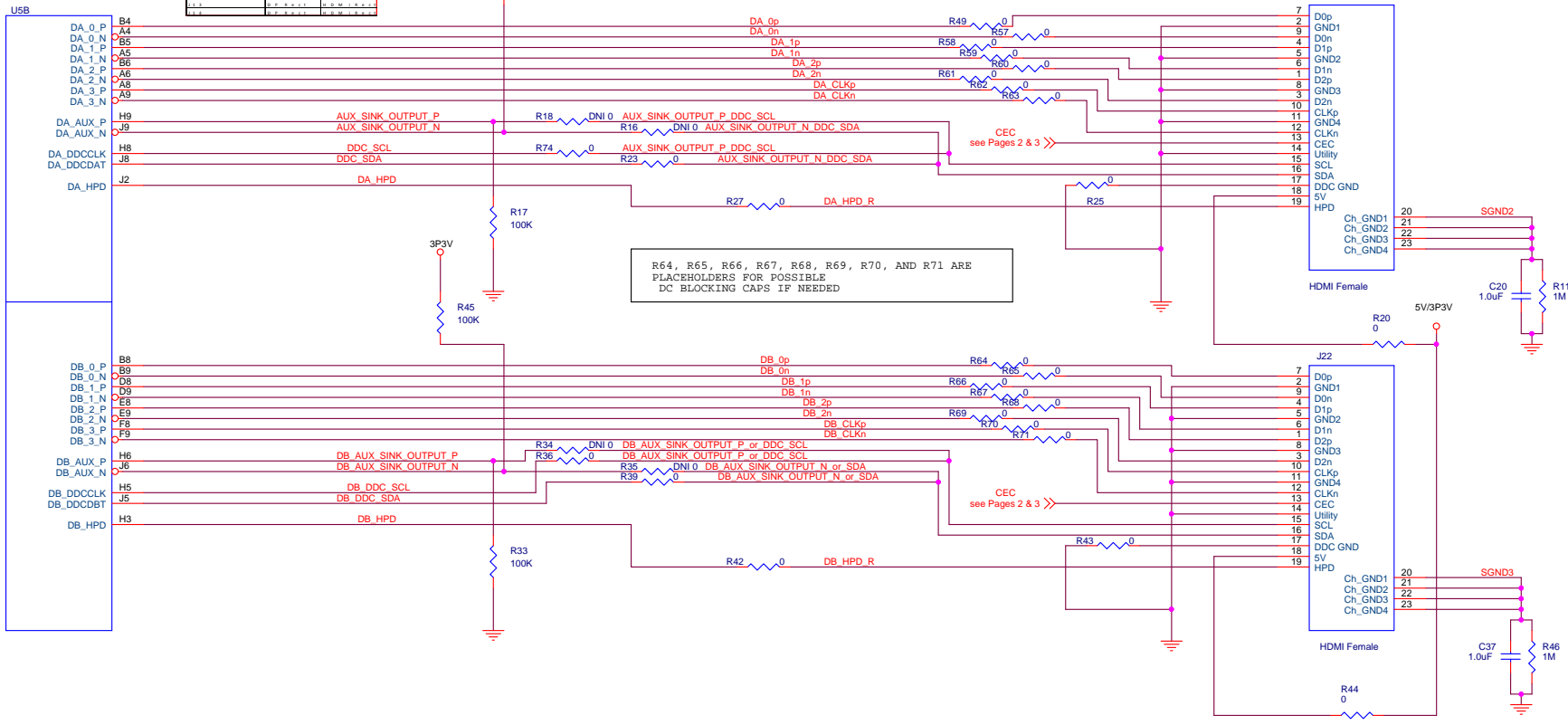
PAGE TITLE			
HD3SS215 Source C			
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U5B	DA_0_P	DA_0_N	DA_1_P	DA_1_N	DA_2_P	DA_2_N	DA_3_P	DA_3_N	DA_AUX_P	DA_AUX_N	DA_DDCCLK	DA_DDCDAT	DA_HPD
	B4	A4	B5	A5	B6	A6	B7	A7	H9	J9	H8	J8	J2
	B8	B9	D8	D9	E8	E9	F8	F9	H6	J6	H5	J5	H3

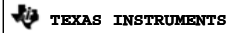
R49, R57, R58, R59, R60, R61, R62, AND R63 ARE  
PLACEHOLDERS FOR POSSIBLE  
DC BLOCKING CAPS IF NEEDED

R64, R65, R66, R67, R68, R69, R70, AND R71 ARE  
PLACEHOLDERS FOR POSSIBLE  
DC BLOCKING CAPS IF NEEDED

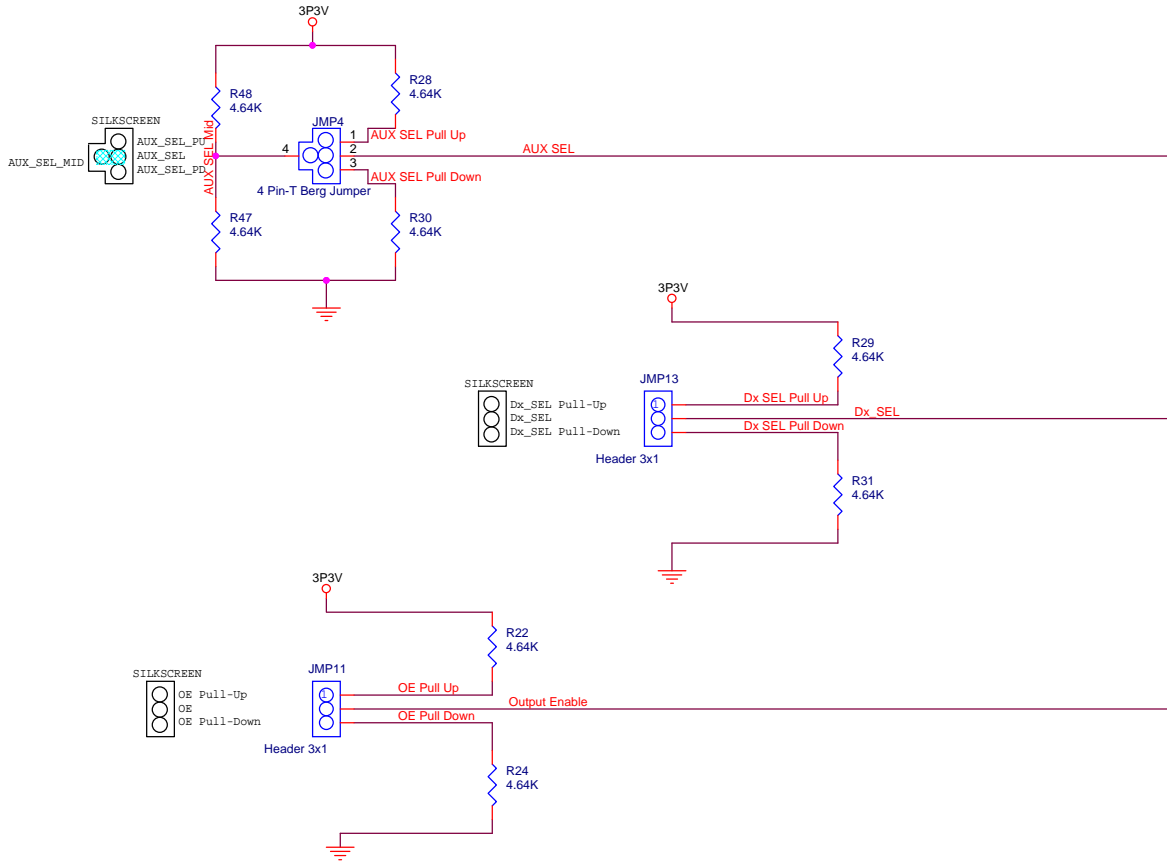
R44, R20 can be installed to provide 5V on DDC and CEC



HD3SS215\_ZOE



PAGE TITLE			
HD3SS215 Sink Port A and B			
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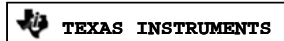
**Switch Control Logic**

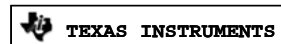
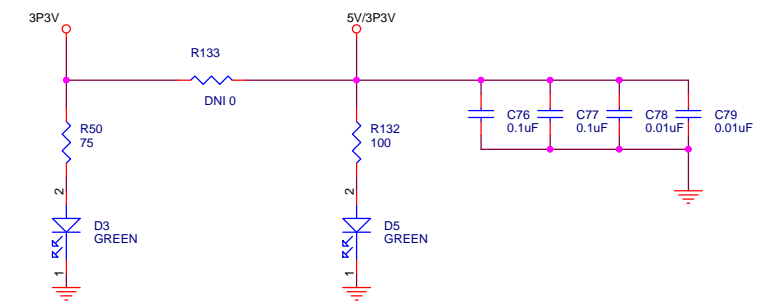
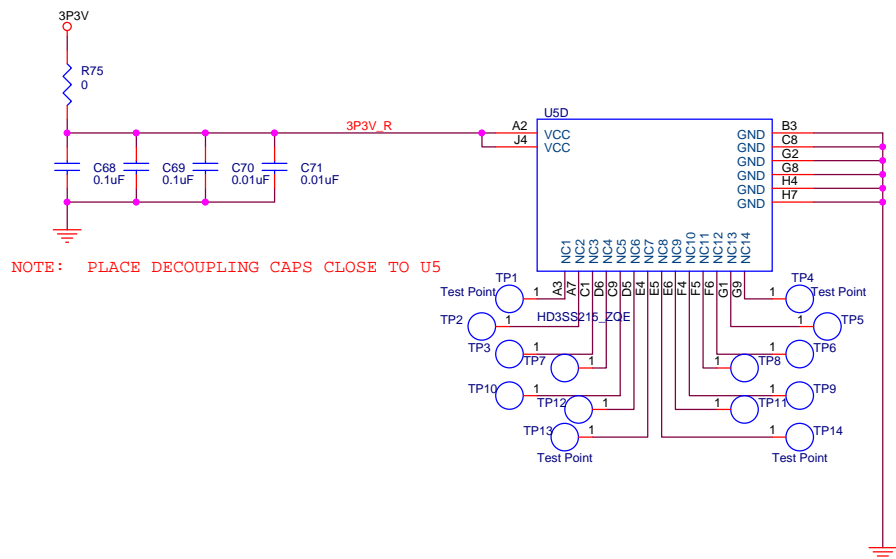
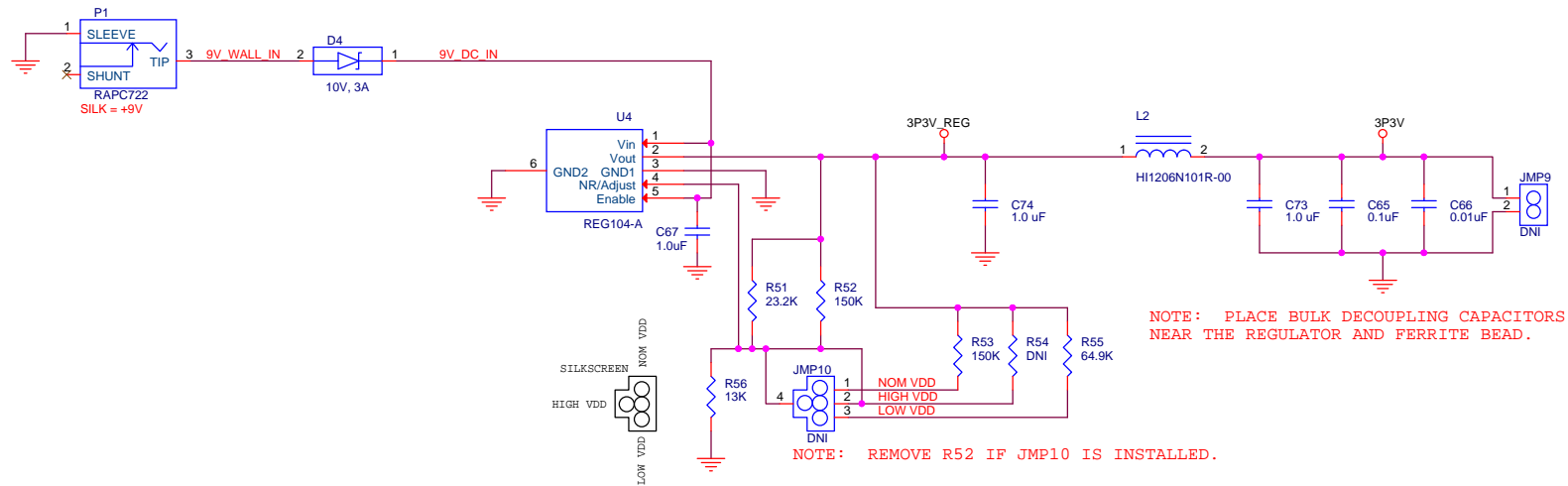
Control Lines	Switched I/O Pins			
	Dx_SEL	DCz(p) Pin z=0, 1, 2 or 3	DCz(n) Pin z=0, 1, 2 or 3	HPDC Pin
L	DAz(p)	DAz(n)	HPDA	CADA
H	DBz(p)	DBz(n)	HPDB	CADB

OE pin - For normal operation, drive OE high. Driving the OE pin low will disable the switch to  
 Note: The ports which are not selected by the Control Lines will be in High Impedance State.

**AUX/DDC Switch Control Logic**

Control Lines		Switched I/O Pins			
AUX_SEL	Dx_SEL		AUXA	AUXB	AUXC
L	L	213/215	To/From AUXC	Z	To/From AUXA
L	H	213/215	Z	To/From AUXC	To/From AUXB
H	L	213/215	Z	Z	To/From DDCA
H	H	213/215	Z	Z	To/From DDCB
M		213	To/From DDCC	Z	Z





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POWER			
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