Mailbox Mechanism

September 2019

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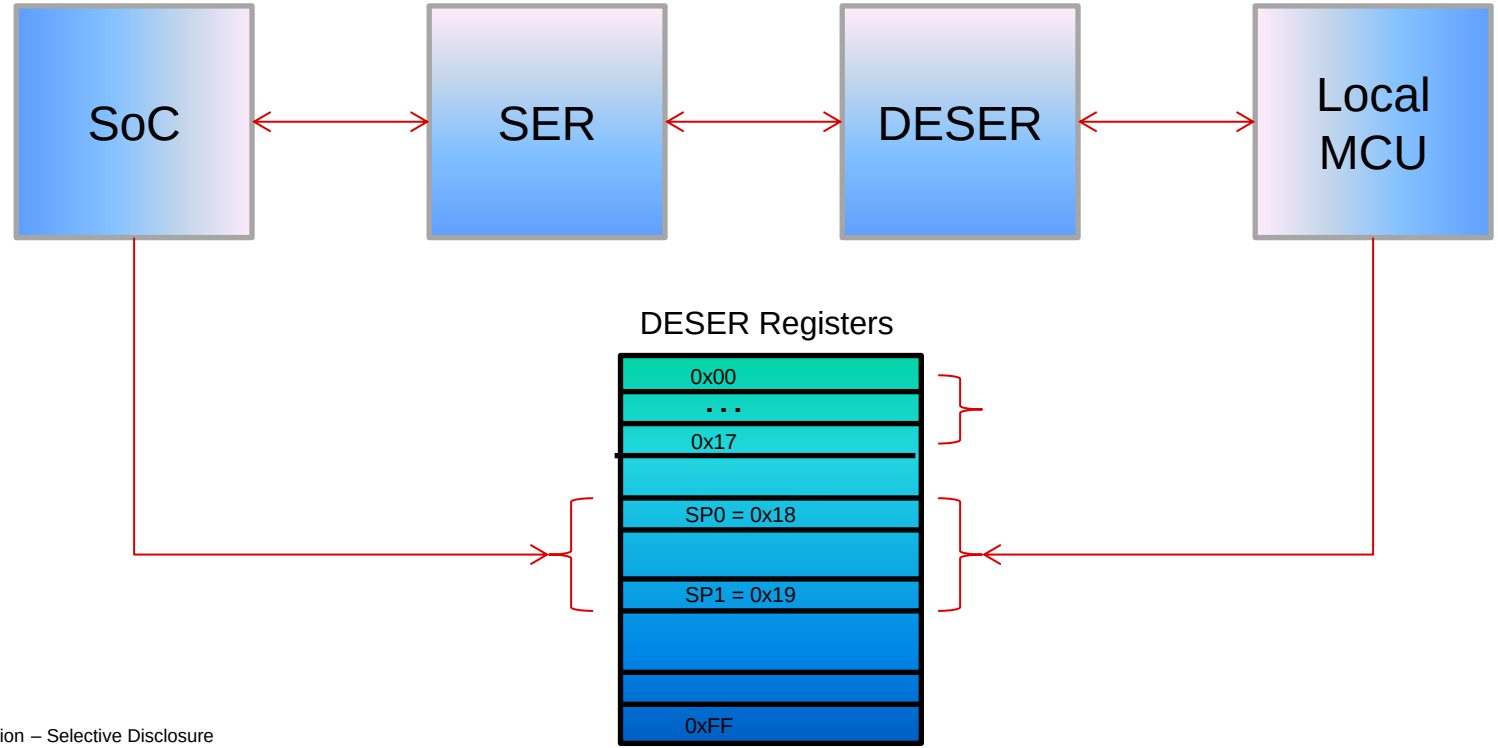
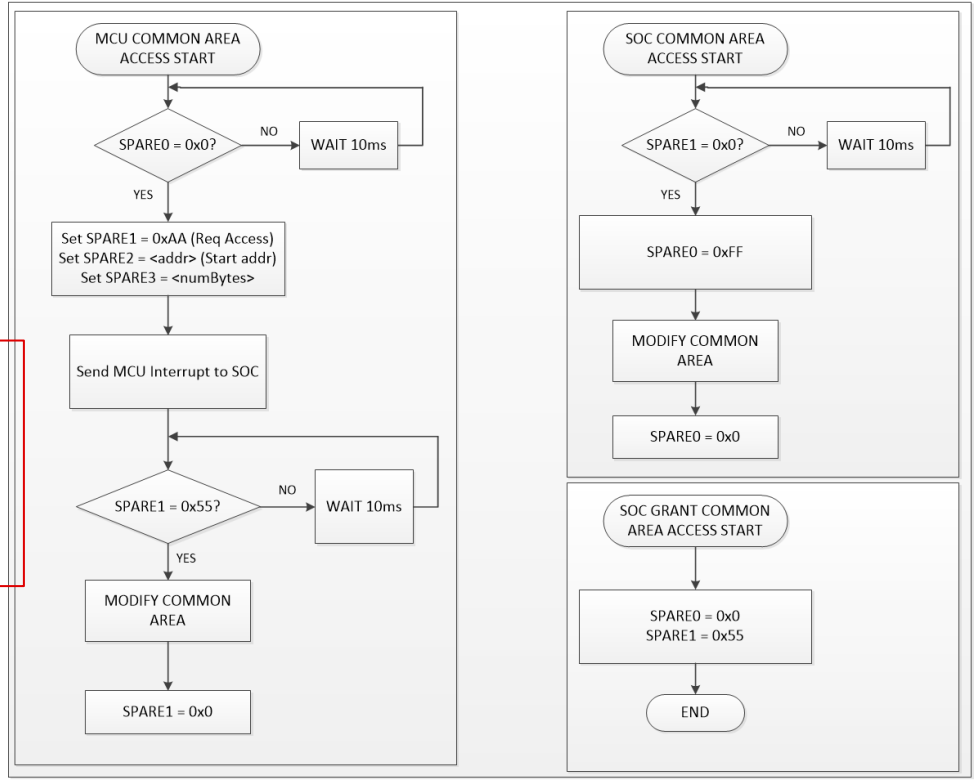


SOC and MCU writing to same Register

1. MCU checks SOC is not accessing common area (SPARE0 = 0x0)
2. MCU requests common area access (SPARE1 = 0xAA)
3. MCU accesses common area after getting SOC grant (SPARE1 = 0x55)



1. SOC checks MCU is not accessing common area (SPARE1 = 0x0)
2. SOC accesses common area after setting lock (SPARE0 = 0xFF)