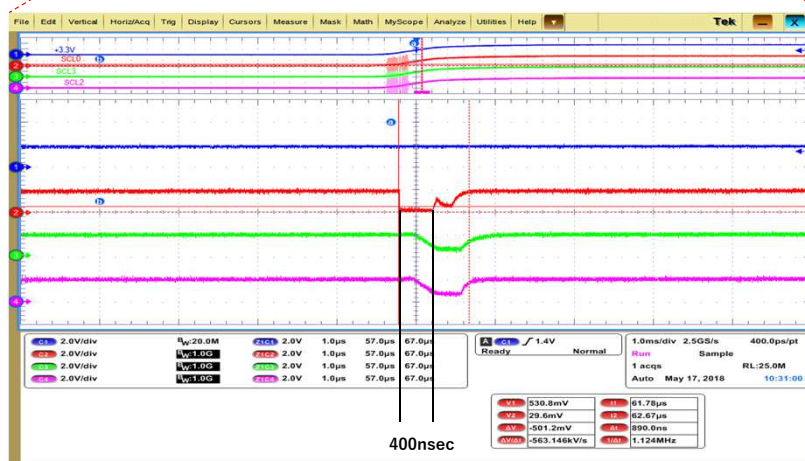
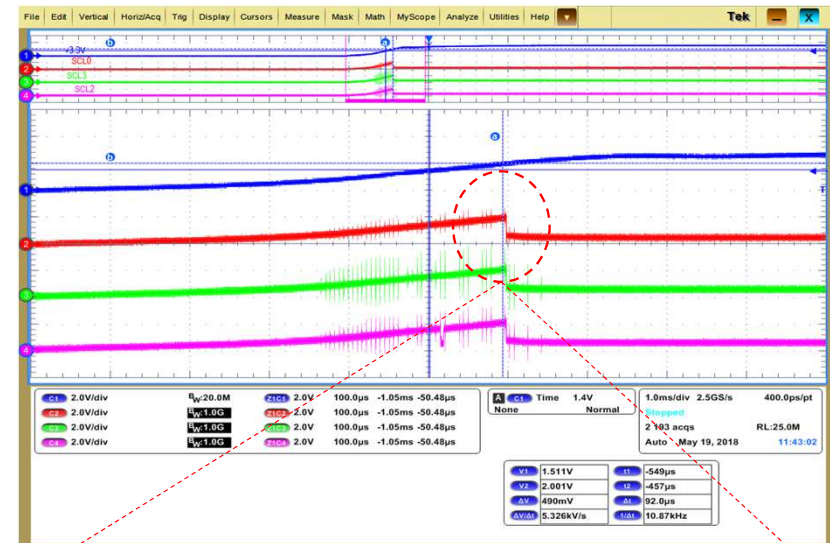
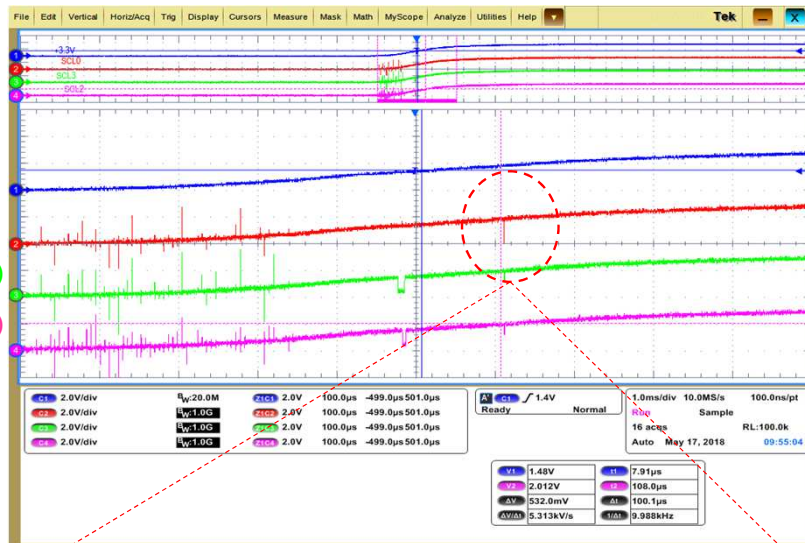


Vcc

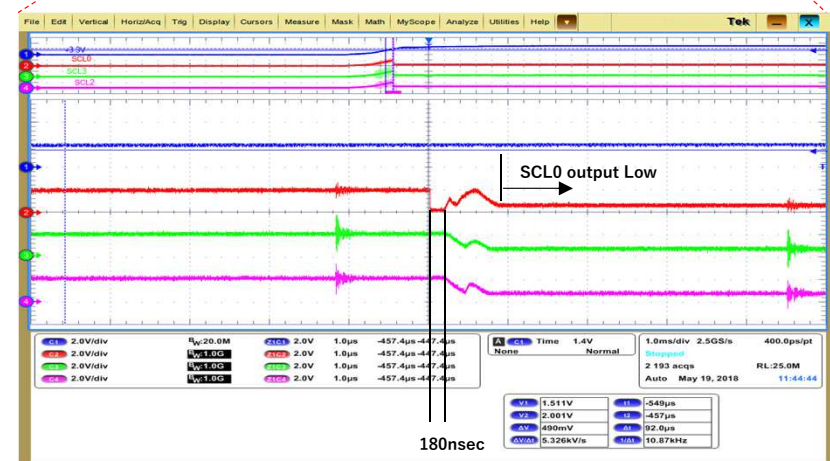
SCL0(input)

SCL2(output)

SCL3(output)



400nsec



180nsec

SCL0 output Low