DP83TD510E : Throughput Check

Test Setup

Packets sent

cable

510 :A

510 :B

Packets received
&
Packet errors checked

Configured in reverse loopback
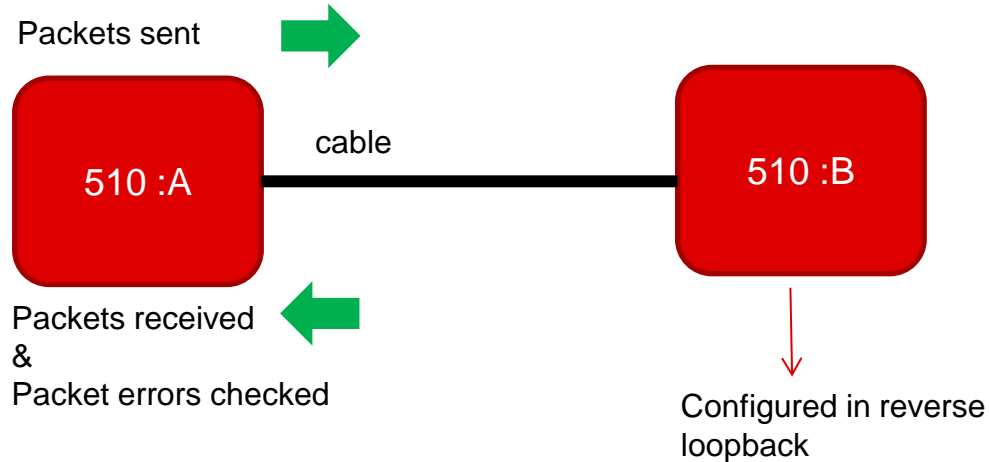
- While doing this test do not send any data from MAC side on any of the DUTs

TEXAS INSTRUMENTS

Test Procedure

- Setup the boards (A and B) and connect them through the desired cable length

- Enable reverse loop-back on board B.

- Enable packet generation and checker on another connected board (board A).

- Following parameters were monitored :
  - Link-status
  - Number of packets received
  - Number of packets received with errors.

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Test Results

Link is up

~1million packets

0 packets with errors

- Similar number of packets were sent multiple times and 0 packet errors were observed.

Test Scripts

Load on Board B

Reverse Loopback Enable

```
1   begin
2   0016 0110 //enable reverse loopback to send the data back on cable
3   end
```

Packet Gen Enable

Reg addresses   Values to be written

```
1   begin
2   001F 8000 //reset the part
3   0119 155F //enable packet generation towards cable and packet checker coming back from the cable
4   001F 4000 //soft reset
5   end
```

Load on Board A

Packet Checker

Registers being read

```
1   begin
2   0010        //x0010 should read 0x0001 for succesful link-up
3   011F 0001   //latches the packets received and error status
4   011F        //should read x0B00 for PRBS lock
5   011D        //
6   011E        //number of packets received is 32bits number with lower 16bits as value of 011D and higher 16bits as value of 011E
7   0121        //
8   0122        //number of errors received is 32bits number with lower 16bits as value of 0121 and higher 16bits as value of 0122
9   end
```

TEXAS INSTRUMENTS