

All PCI Signals should be length matched within 50 mils with the following exceptions: clk pins (see note below), nets: PCI_PRST, PCI_INTA#, PCI_INTB#, PCI_INTC#, PCI_INTD#, PCI_ACK64#, PCI_M66EN, and PCI_PME# are not synchronous and may be slightly longer.

PCI Clocks should be slightly longer than the longest trace on the PCI bus. Clocks should be length matched to each other within 10 mils. The PCI_FBCLK trace must be 2.5 inches (2500 mils) longer than the length of the other clock signals (this is for the total trace length which is the sum of the net between U1.F3 and R26 and the the net from R26 to U1.B11).

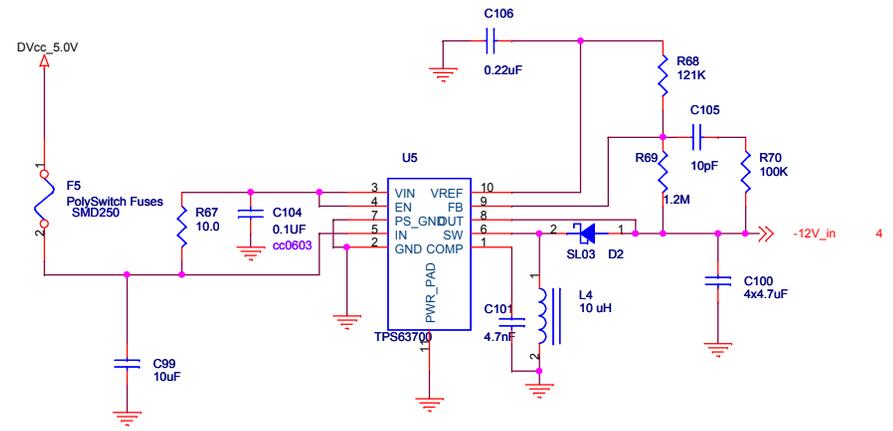
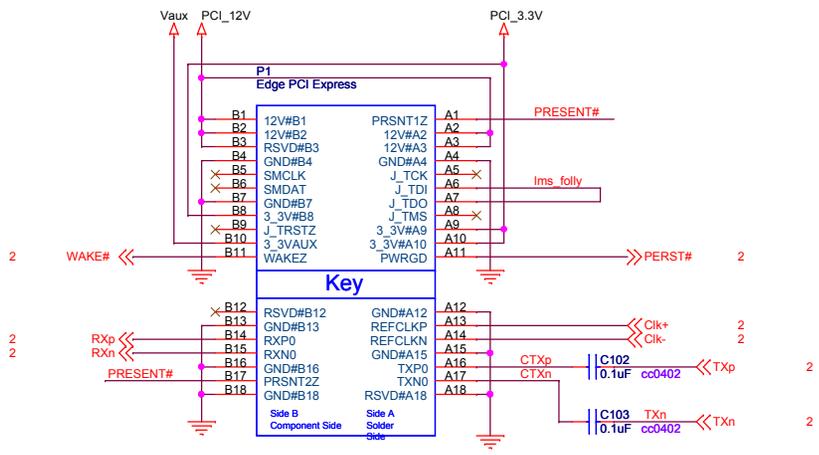
All 32 bit PCI slots must be placed so the slot can be put on the board as either a 3V or a 5V slot. All pins used as keying pins (A12, A13, A50, A51, B12, B13, B50, B51) should be put on the board and connected to the GND plane. Mounting holes must be placed on either side of the socket.

(CTXn + TXn) and (CTXp + TXp) are a 100 ohm differential impedance pair (50 ohm single ended) and must be length matched with 5 mils. i.e. CTXp must be within 5 mils of CTXn, TXp must be within 5 mils of TXn, and (CTXp + TXp) must be within 5 mils of (CTXn + TXn). The coupling capacitors must be placed as close to the PCI Express Edge connector as possible.

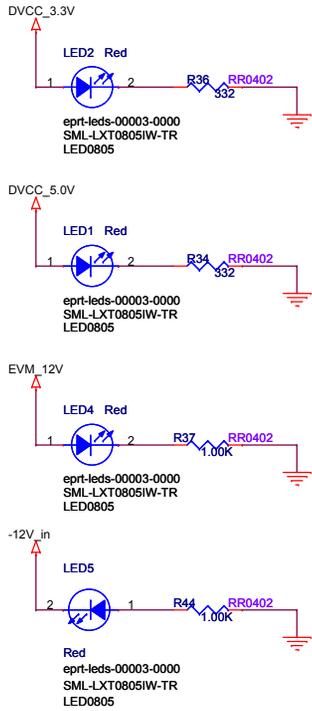
RXp and RXn are a 100 ohm differential impedance pair (50 ohm single ended) and must be length matched with 5 mils.

Card dimensions and design should match requirements for the standard half length PCI-Express card and should be designed to use the card retainer as detailed in the PCI Express Electromechanical specification rev 1.0a. Height may be increased to allow for placement of all components but width and thickness must be as required in the specification

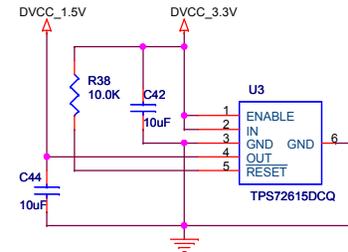
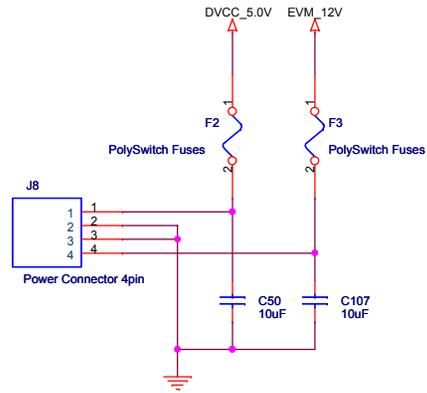
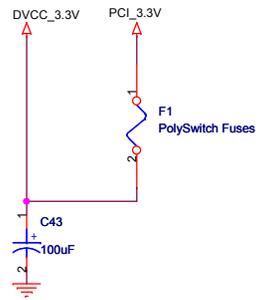
Title		
XIO2001 ZGU		
Size B	Document Number <Doc>	Rev C
Date:	Thursday, June 04, 2009	Sheet 1 of 4



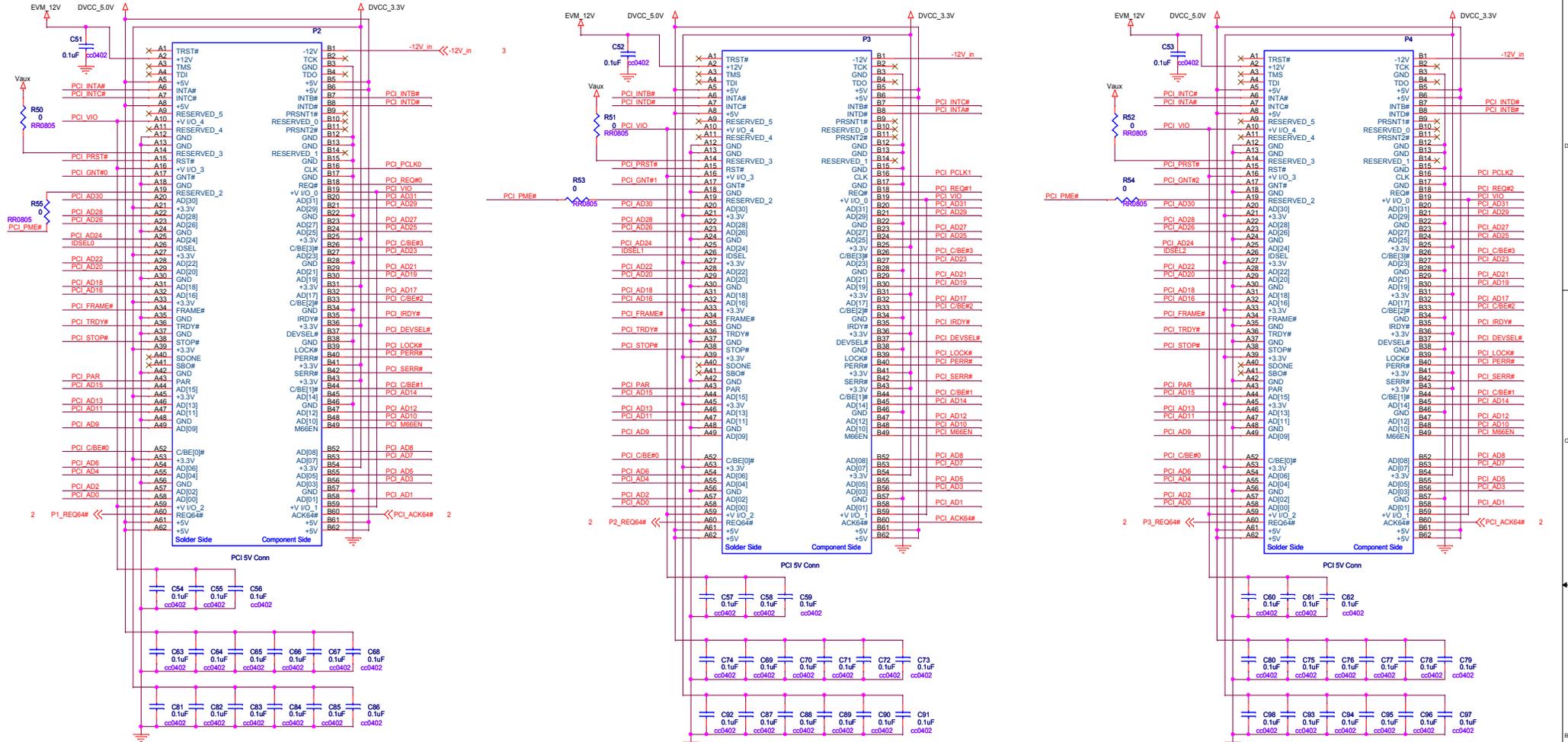
POWER LEDs



Power



Title		XIO2001ZGU	
Size B	Document Number	<Doc>	
Date:	Thursday, June 04, 2009	Sheet	3 of 4
			Rev C



- >>PCI_AD[31..0] 2
- >>PCI_CBE[3..0] 2
- >>PCI_REG[2..0] 2
- >>PCI_PCLK[2..0] 2
- >>PCI_FRAME# 2
- >>PCI_IRDY# 2
- >>PCI_TRDY# 2
- >>PCI_DEVSEL# 2
- >>PCI_STOP# 2
- >>PCI_PERR# 2
- >>PCI_SERR# 2
- >>PCI_PRST# 2
- >>PCI_MBSEN 2
- >>PCI_INTA# 2
- >>PCI_INTB# 2
- >>PCI_INTC# 2
- >>PCI_INTD# 2,3

PCI_AD16 R58 100 IDSEL0
 PCI_AD17 R59 100 IDSEL1
 PCI_AD18 R60 100 IDSEL2