Application Report
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FPD-Link IV Power-Over-Coax Design Guidelines

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Abstract

The purpose of this document is to outline design requirements and guidelines for implementing an FPD-Link IV ADAS system based around a Power-over-Coax (PoC) network. This document also provides several TI approved PoC networks for use with the DS90UB9702-Q1 and its compatible serializer devices such as the DS90UB971-Q1.

Table of Contents

1 Revision History

DATE	REVISION	NOTES	DESCRIPTION
April 2020	0.1	Initial Draft	
April 2020	0.2	Second Draft	
August 2020	0.3	Third Draft	
October 2020	0.4	Fourth Draft	
May 2023	0.5	Fifth Draft	Updated inductor descriptions in Section 7

2 Trademarks

3 Overview

Modern advanced driver assistance systems (ADAS) are commonplace in the industry and can rely on several kinds of sensors for general driver safety, driver assist features, and in some cases autonomous driving. The increasing amount of sensors added to vehicles can add complexity to the system implementation and may require multiple cables to transfer high-speed data and power. An ADAS system using FPD-Link SerDes chipsets eliminates the need to have a separate cable to deliver power from the deserializer board to the serializer and sensor. This is achieved by using Power-over-Coax (PoC) filters to separate DC power from the high speed FPD-Link signal, allowing power to be transferred over the same coax cable as the FPD-Link data.

When paired with a DS90UB971-Q1 serializer, the DS90UB9702-Q1 receives data from imagers supporting 8MP+ resolution and runs at a forward channel rate of 7.55Gbps. DC power is provided to the remote serializer and accompanying sensors using the same coaxial cable by utilizing PoC networks.

3.1 PoC Theory of Operation

The purpose of a Power over Coax network is to separate the high-speed data signal from the DC power signal. The high-speed signal content consists of a high-speed forward channel carrying video and control data to the deserializer and a lower speed back channel carrying control data to the serializer. Figure 1 below shows a high-level overview of how FPD-Link and DC power share a single coax cable. For proper separation the DC component of the FPD-Link signal must be completely blocked from entering the DOUT pins of the serializer and the RIN pins of the deserialzier. This is accomplished by placing AC Coupling capacitors in line with the FPD-Link signal path which blocks the DC signal and passes the forward and back channel signals. A simple capacitor will work for this since it has very low impedance over the forward and back channel frequency and is an open circuit at DC.

The second circuit, which is one that passes DC and doesn't interfere with the high-speed signal, is much more complicated. For this low pass filter circuit to not interfere with the high-speed signal it will need to have an impedance much larger than the characteristic impedance of the channel. For a 50Ω channel the low pass filter impedance should at least be 1kΩ over the required frequency band.

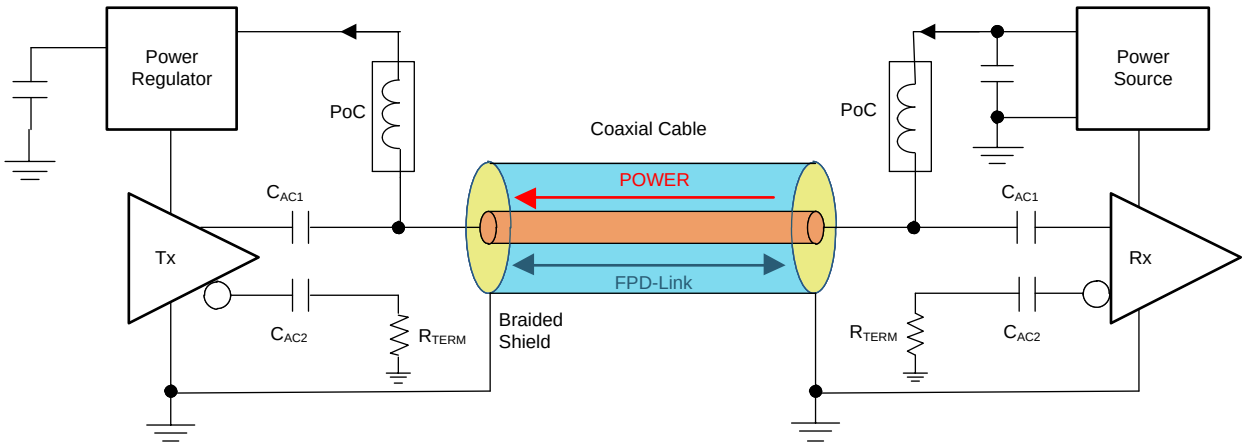

Figure 1 PoC Theory of Operation

3.1.1 Inductor Characteristics

An ideal inductor would be capable of blocking all AC frequencies and pass all DC power. However, inductors have characteristics that make them behave less like an inductor in extreme circumstances. Real world inductors behave more closely to the circuit shown in Figure 2 with parasitic capacitance and resistance components.

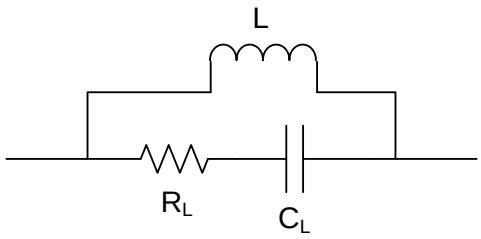

Figure 2 Real World Inductor

For this reason, there exists a self-resonant frequency (SRF) where the component's impedance peaks. Beyond this point the parasitic capacitance takes over and can lower its impedance. The SRF can be calculated using Equation 1 below where L is the inductance, C is the parasitic capacitance, and F is the resonant frequency, but typically this will be listed on the component's datasheet.

$$F = \frac{1}{\sqrt{LC}}$$

Equation 1 Self Resonant Frequency

The impedance of a 100uH inductor can be seen in Figure 3 as a function of frequency.

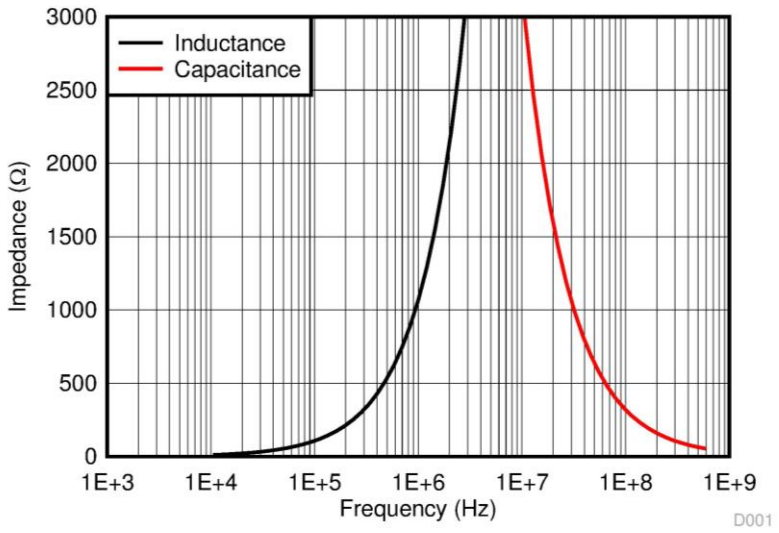

Figure 3 SRF Impedance Plot

Figure 3 shows that for a 100uH inductor the impedance rises above 1kΩ at about 1MHz and drops below 1kΩ above frequencies of about 30MHz. For this reason, a more complex low pass filter is required to raise the impedance over the entire frequency bandwidth relevant for FPD-Link bidirectional signaling.

To boost the impedance of the circuit to cover the frequency band required by FPD-Link communication the user can add several inductive components in series, each with different values. Using a 4.7uH inductor in series with a 100uH inductor will stretch the high impedance frequency band to higher frequencies. The 4.7uH inductor has a much higher SRF and will continue to behave as an inductor well past the frequency range of the 100uH inductor. Figure 4 below shows both the impedances of the 100uH inductor and 4.7uH inductor over a frequency of 1 kHz to 1 GHz. Additionally it shows the impedance of the two inductors when put in series and how the impedance of the series combination remains above 1kΩ over a much larger range.

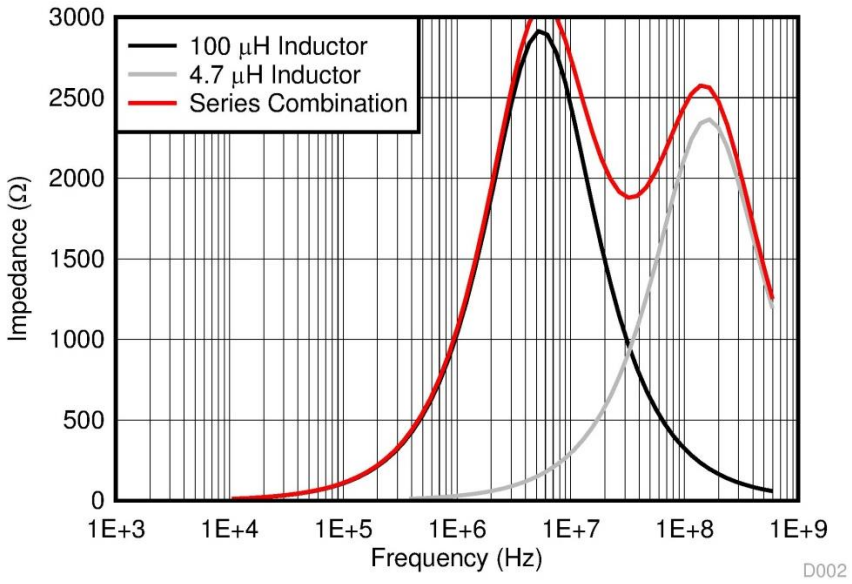

Figure 4 Impedance of Series Inductors

So by simply cascading inductors in series the user can build a wide-bandwidth inductor that can cover the frequency range of the back channel all the way to the frequency of the forward channel. Figure 5 below shows impedance graphed for individual inductors separated by one decade (100uH, 10uH, 1uH, 0.1uH), individually they do not provide an impedance of 1kΩ over a wide frequency range. But as Figure 6 shows, when they are combined they provide consistent impedance over a large frequency range.

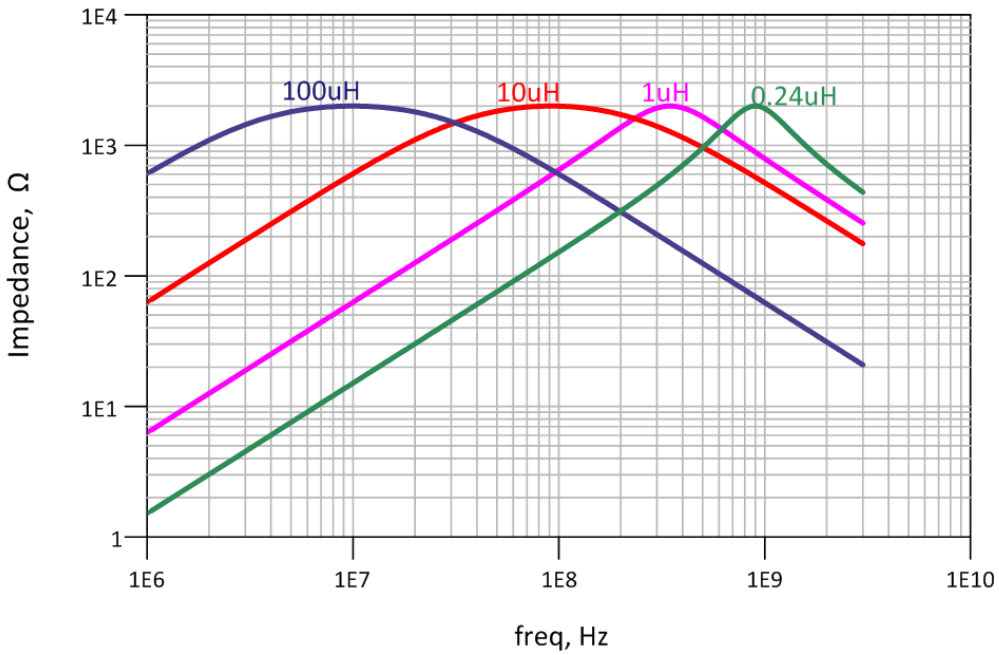

Figure 5 Impedance of Individual Inductors

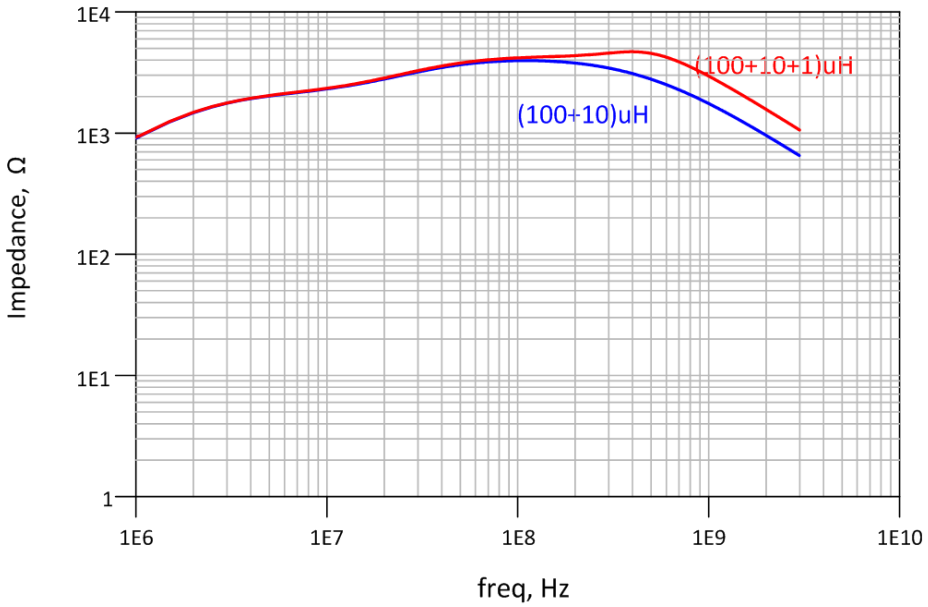

Figure 6 Impedance of Combined Inductors

Additionally non-ideal inductors also have a rated current that correlates to the amount of energy that can be stored in the magnetic field created by the inductor. This maximum current is referred to as the saturation current, and beyond this point the inductor ceases to behave like an ideal inductor. PoC networks when being designed need to account for these non-idealities to work properly.

3.1.2 Capacitor Characteristics

Figure 7 shows a breakdown of a non-ideal capacitor component. A capacitor has an accompanying parasitic resistance and inductance, and at very high frequencies the inductance takes over and the capacitor no longer behaves like a capacitor. If we look at the impedance of the capacitor vs frequency it will look similar to Figure 3 but flipped. There exists an area of lowest impedance at the resonant frequency and then it will begin to rise after that point.

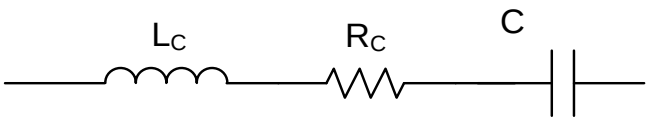

Figure 7 Real World Capacitor

Capacitors are used in the PoC network for decoupling the input of DC regulators on the serializer side of the link. Similarly to how the inductors are cascaded in series to create a wide bandwidth inductor, capacitors can be cascaded in parallel to create a wide bandwidth capacitor; a capacitor that will pass a larger frequency range and better decouple the DC regulators. Often times when choosing a decoupling capacitor, it can be treated as an ideal capacitor because noise from the DC regulators is much lower frequency than the signal frequency trying to be blocked.

$$Z = \frac{1}{2\pi f C}$$

Equation 2 Impedance of Capacitor

3.1.3 Inductors vs. Ferrite Beads

As the frequency of FPD-Link communications rise the need for more complex PoC networks follows. Ferrite beads can help greatly when dealing with extremely high frequencies. Ferrite beads are considered a special kind of inductor that has a very low inductance but are rated for frequencies in the MHz to GHZ range. Where standard coil inductors typically begin behaving

like a capacitor, a ferrite bead will continue to provide high impedance. Figure 8 below shows a real world ferrite bead that has an inductive component, capacitive component, and resistive components. The Ferrite bead is primarily inductive therefor L_{FB} is the most dominant portion of this model. Also the parasitic capacitance C_{Par} does not become significant until very high frequencies.

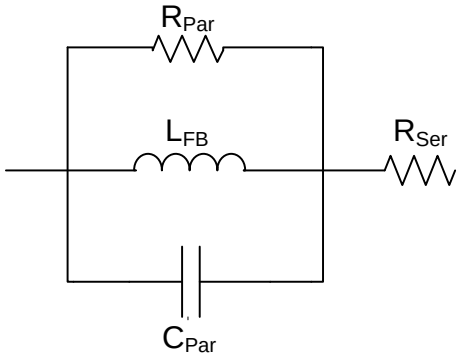

Figure 8 Real World Ferrite Beard

Adding ferrite beads to the PoC network may seem like an obvious solution for blocking high frequencies however it is important to know that at DC the ferrite bead will have a higher resistive component than a standard coil inductor. While the resistance is typically rather small (<1Ω) it can add up if multiple beads are put in series and ruin the current carrying capabilities of the PoC network.

4 Design Considerations

There are two main factors to consider when selecting a PoC network: device frequency range and power consumption of the serializer/imager board.

4.1 Bandwidth Considerations

In order to design a suitable PoC network, it is important to look at the frequency range that the network must be able to filter. For example, an FPD-Link IV system using the DS90UB971-Q1 and DS90UB9702-Q1 running in synchronous mode can support a forward channel rate of 7.55Gbps (3.775GHz) and a back-channel rate of 47.1875MHz. The PoC network must effectively filter a frequency range from half the back-channel frequency to the forward channel frequency.

Table 1 shows each serializer device compatible with the DS09UB9702-Q1, and their forward/back channel communication speeds when paired with the DS90UB9702-Q1.

Deserializer	Serializer	Mode	BC Frequency	FC Frequency
DS90UB9702-Q1	DS90UB913A-Q1	Non-Synchronous	2.5MHz	700MHz
	DS90UB933-Q1	Non-Synchronous	2.5MHz	933MHz
	DS90UB951-Q1	Non-Synchronous	10.25MHz	2.43GHZ
	DS90UB935-Q1	Synchronous	52.5MHz	2.1GHZ
		Non-Synchronous	10.25MHz	2.1GHZ
	DS90UB953-Q1	Synchronous	52.5MHz	2.1GHZ
		Non-Synchronous	10.25MHz	2.1GHZ
	DS90UB971-Q1	Synchronous	47.1875MHz	3.775GHz
		Non-Synchronous	10.25MHz	3.775GHz

Table 1 Serializer Frequency Ranges

4.2 Power Considerations

Each PoC network has a maximum current that it can support while maintaining required impedance based on the saturation characteristics of the components. Inductors as discussed in Section 3.1.1 do not behave in an ideal manner, they dissipate heat, pass very high frequencies and saturate when too much current is passed through. All components and cables have parasitic impedances that lead to IR drop throughout the entire circuit. It is important to know the maximum power the serializer board will draw and select a PoC network that can deliver that power for a given PoC voltage. The maximum power should be calculated as the worst-case scenario of power consumption on the serialzier side of the link. Highest power consumption refers to a period where the sensor is gathering active frame data and all other remote devices are operating. TI approves several different PoC networks capable of different levels of power delivery. The user will need to select a PoC network capable of supplying enough current for the sensor/serializer.

5 FPD-Link PoC Requirements

When incorporating a PoC network into a system the user must ensure that any PoC network chosen meets TI's channel specifications and PoC noise requirements in order to ensure robust operation across all component tolerances and operating conditions.

5.1 Channel Requirements

Channel requirements provide the return loss and insertion loss requirements that the PoC network must meet for error-free operation of the serializer/deserializer pair. The PoC network must comply with the return loss requirement to protect against degradation of the signal. Return loss refers the amount of reflections in the link seen by the transmitter. A network typically can fail the return loss requirement when there is an impedance mismatch in the channel. A network can also fail when inductors and ferrite beads have been chosen incorrectly. Return loss can be calculated using Equation 3 below.

$$\boldsymbol{Return\ Loss(dB) = 10\log_{10}\left(\frac{P_{out}}{P_{in}}\right)}$$

Equation 3 Return Loss

It is critical to follow the FPD-Link and PoC layout guidelines from the datasheet to ensure the return loss requirement is met. If a board has already been designed and does not meet return loss requirements then a TDR test may be useful to help locate the area of the board where impedance mismatches occur. The return loss requirement is given in Table 2; for robust operation of the system the return loss should be less than the listed values over the required frequency range of the system.

Frequency	PCB Budget	Total Budget	Cable Budget
1 – 100MHz	-20	-16	-22
.1 – 1GHz	-12 + 8*log(f)	-9 + 7*log(f)	-12 + 8*log(f)
1 – 2.5GHz	-12	-9	-12
2.5 – 4.2GHz	-12	-9	-12

Table 2 Return Loss Requirement (9702/971)

The network must also comply with insertion loss requirements for effective FPD-Link communication. Insertion loss refers to the amount of power the signal loses as it travels through the channel. Causes of insertion loss requirements not being met is typically due signal attenuation in the channel and can be calculated using Equation 4 below.

$$Insertion\ Loss(dB) = -10\log_{10}\left(\frac{P_{out}}{P_{in}}\right)$$

Equation 4 Insertion Loss

If meeting insertion loss requirements is an issue than the user needs to ensure again that all board layout and PoC guidelines provided by TI are being followed and high quality components are used in signal transmission and PoC. The insertion loss requirement can be seen in Table 3 below; for robust operation of the system the insertion loss must be greater than the values listed over the frequency range required by the system.

Frequency	PCB Budget	Total Budget	Cable Budget
1.05GHz	-0.3	7.1	-6.5
2.1GHz	-0.55	10.4	-9.3
4.2GHz	-0.85	15.4	-13.7

Table 3 Insertion Loss Requirement (9702/971)

6 PoC Noise

PoC networks should be designed with the integrity of the high-speed signal in mind and should not interfere with data transmission and for the DC signal to have as little noise as possible.

6.1 PoC Noise Requirements

There are two separate noise requirements in a PoC network used with the DS90UB9702-Q1. The first requirement is on the side of the serializer measured at the input of the voltage regulator (denoted Vpoc noise in Figure 9). The second requirement is on the deserializer side at R_{IN+} (denoted Rin+ noise in Figure 9).

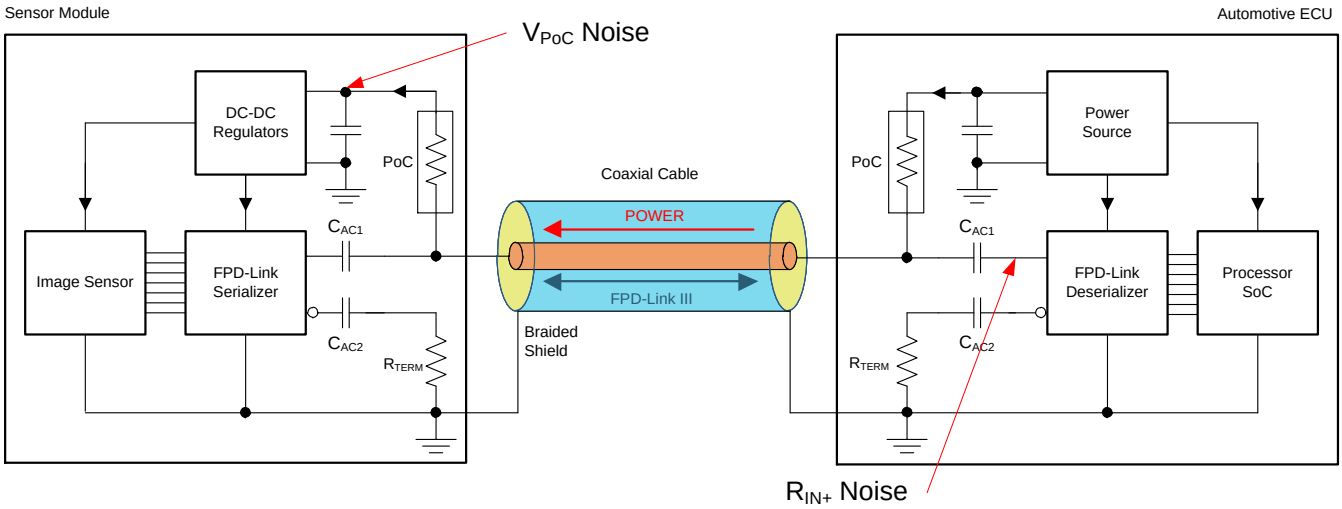

Figure 9 PoC Noise Measurement Nodes

6.2 Measuring V_{PoC} Noise and Pulse

V_{PoC} noise is the measurement of noise introduced into the system from serializer and sensor operation. Figure 10 shows a typical waveform measured from the input of the DC regulators. The supply noise is introduced from the switching of such DC buck regulators and the pulse is due to the switching of the sensor. During periods of blanking, the current draw from the sensor is significantly lower than during active periods, which causes the voltage to spike.

6.2.1 Requirements

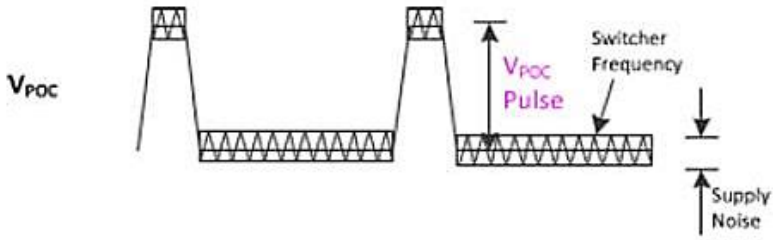

Figure 10 Vpoc Noise

- V_{PoC} supply noise must be less than 100mV peak-to-peak
- V_{PoC} pulse must be less than 500mV peak-to-peak (from image sensor blanking and valid periods)
- V_{PoC} pulse slew rate must be greater than 100us/V

6.2.2 Measurement Procedure

- Connect serializer to deserializer through coax
- Power entire system (Sensor, Serializer, Deserializer, etc.)
- Set oscilloscope bandwidth to 0 – 50MHz
- Probe V_{POC} at input of DC regulators on serializer board

- Subtract noise floor measurement from V_{POC} noise measurement

6.2.3 Example

Below is an example of V_{POC} noise being measured using a DS90UB9702-Q1 EVM and DS90UB971-Q1 image module. Figure 11 shows the serializer and sensor connected to the 9702-Q1EVM with a coax cable and FAKRA connector. The DS90UB9702-Q1EVM is configured for Power-over-Coax and is ready to be powered on.

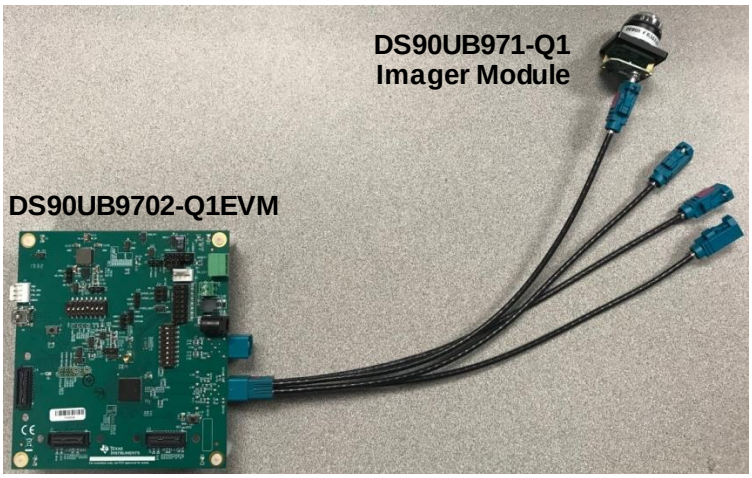

Figure 11 V_{POC} Noise Test Setup

Before measuring the V_{POC} noise, the noise floor must be tested. This example uses a Tektronix P6247 probe and that probe is shorted to ground and Figure 12 shows the measurement seen on the scope. The peak-to-peak voltage is measured at 7.7mV and since this noise is not cause by the system it can be subtracted out from any further noise measurements.

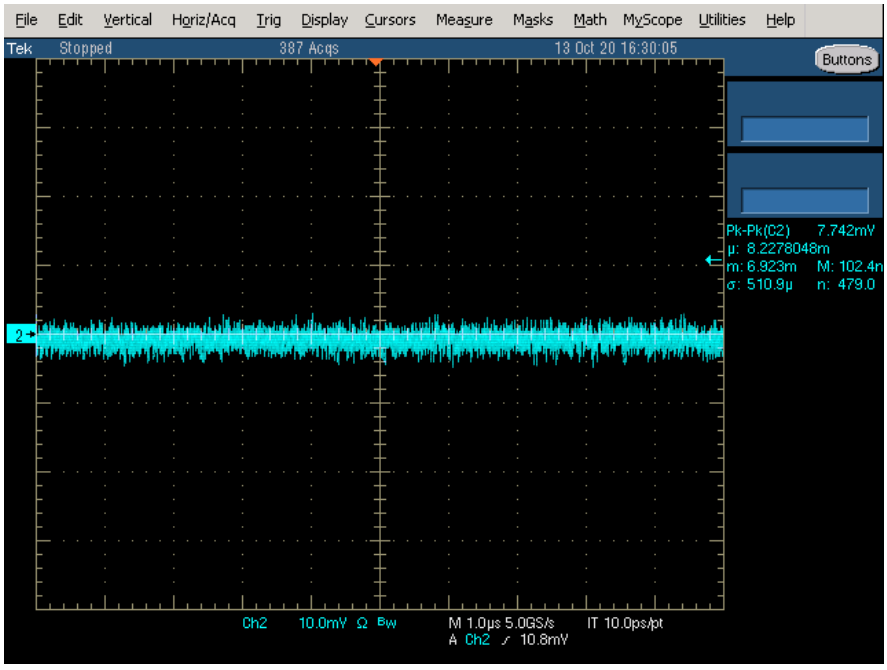

Figure 12 Noise Floor Measurement

After finding the noise floor the short can be opened and the probe can be used to measure V_{POC} noise. Figure 13 shows a close-up shot of the serializer board and where V_{POC} noise is measured at.

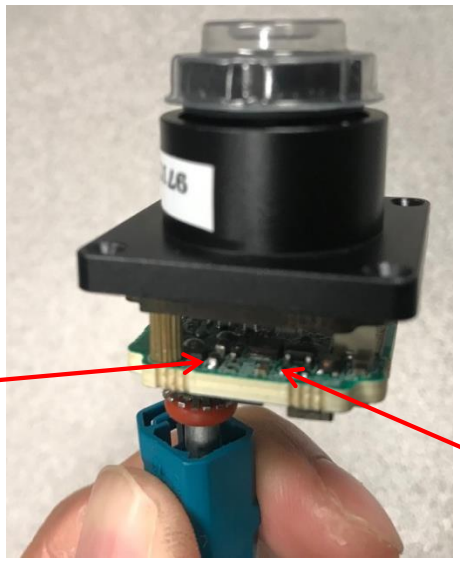

Figure 13 V_{PoC} Noise Probe Points

Figu[illegible]red at 52mVpp excluding the effect of the voltage spike during the sensors blanking period. After the noise floor is subtracted from the signal the total PoC noise is measured at 52mVpp, which is less than the 100mVpp requirement. Figure 14 also shows the voltage spikes during the blanking period of the sensor. In this example the spike is around a 164mVpp which meets the requirement of being less than 500mVpp.

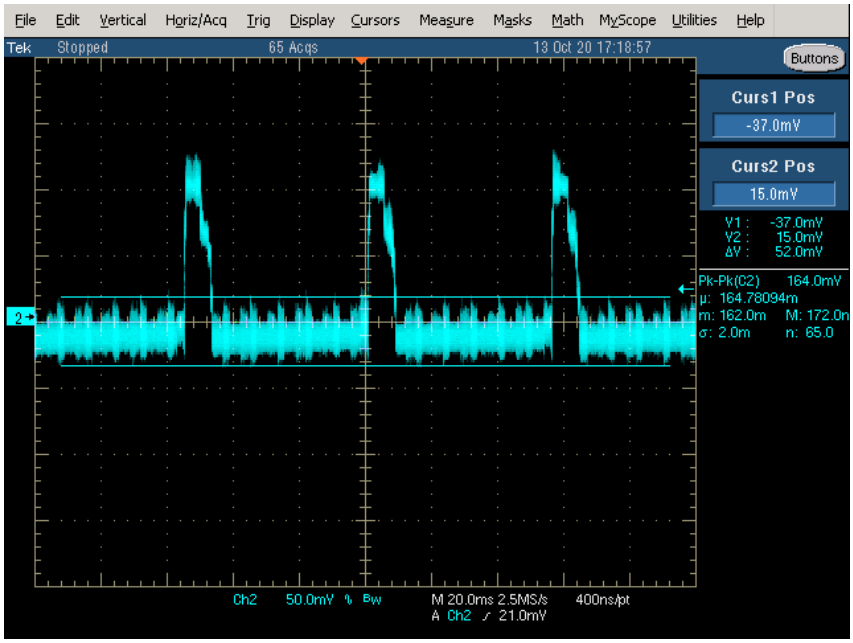

Figure 14 V_{PoC} Noise Measurement

6.3 Measuring R_{IN+} Noise

6.3.1 Requirements

- R_{IN+} noise must be less than 10mV peak-to-peak between 0 and 50MHz

6.3.2 Measurement Procedures

- Connect the serializer and deserializer using a coax cable

- Power on deserializer board
- Pull PDB pin low to turn off both serializer and deserialiser
- Set oscilloscope bandwidth to 0 – 50MHz
- Use a short probe tip for measuring ground
- Account for noise floor

6.3.3 Example

This example shows how to measure the R_{IN+} noise at the input of the deserializer. This example is very similar to the previous example for measuring V_{POC} noise in the system except that the serializer and deserializer are powered down using the PDB pin on the deserializer. The setup can be seen in Figure 11 and the noise floor measurement will be the same as in Figure 12. After the PDB pin has been pulled low an accurate measurement of the R_{IN+} noise can be taken by probing the R_{IN+} pin on the deserializer shown in Figure 15.

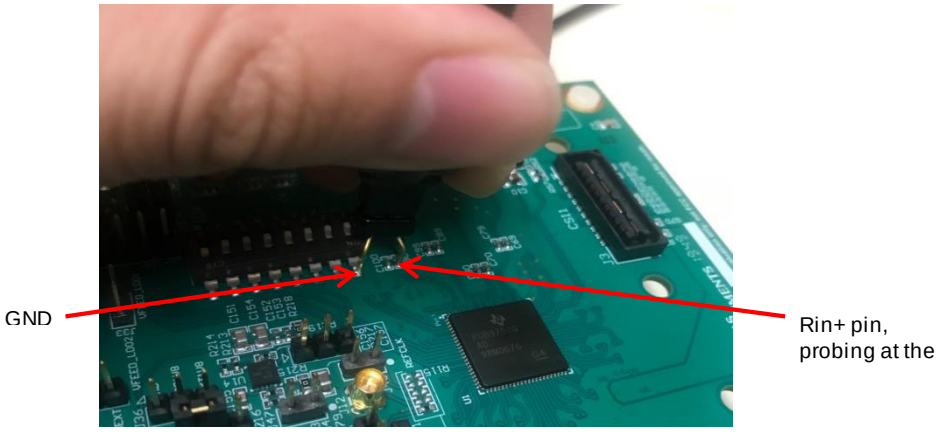

Figure 15 R_{IN+} Noise Probe Points

The noise measured can be seen in Figure 16 below and shows noise of 12.88mVpp and after the subtraction of the noise floor a total noise of 5.47 mVpp is seen at the R_{IN+} input of the deserializer.

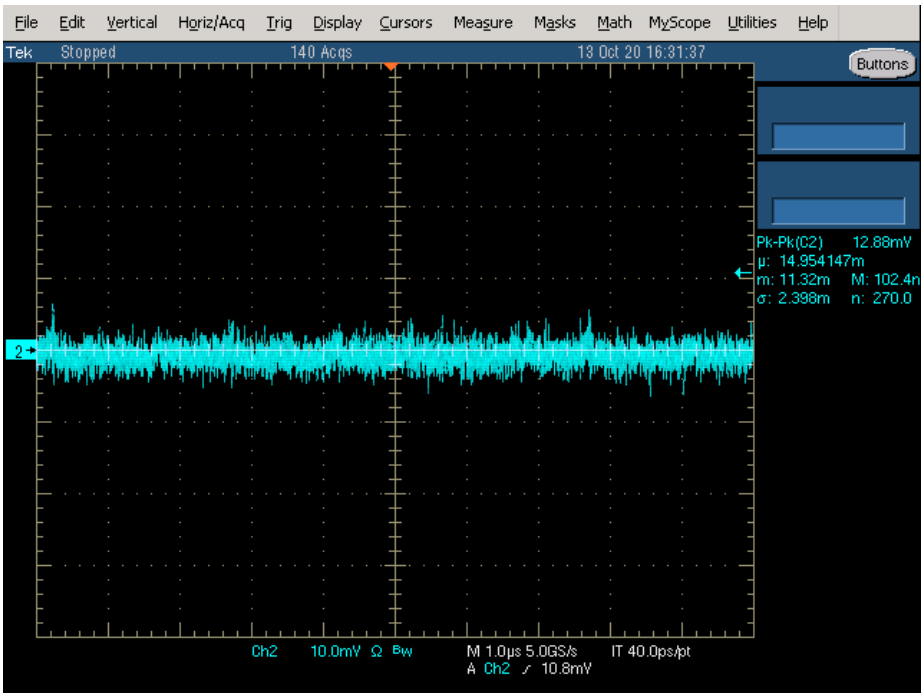

Figure 16 R_{IN+} Noise Measurement

6.4 Causes of PoC Noise

Below is a list of possible causes of PoC noise.

- Switching regulators – Switching regulators switch the output on and off at a high frequency in order to step a high voltage DC signal down to a lower voltage. This switching is back fed through the regulator to its input, V_{PoC}. The switching frequency is typically in the range of kHz and can make its way back through the PoC network and degrade the signal-to-noise ratio.
- Image sensors – Sensors can introduce noise into the system at the frame rate of the sensor due to its varying power demands. This demand peaks during the gathering of valid frame data and drops during the blanking period. This low frequency noise more easily finds its way through the PoC network which is designed to block frequencies in the MHz to GHz range.
- Poor Board Layout – Not following the guidelines in the datasheet for board layout can lead to signal degradation and extra noise in the system.
- Environmental Noise – Environmental noise is from the surroundings and may behave like white noise, and can impose noise at all frequencies across the spectrum.

6.5 Reducing Effects of PoC Noise

Switching regulators are large contributors to PoC noise. To reduce their effect, TI recommends using low-dropout regulators (LDOs) wherever possible because an LDO does not generate any noise from switching. In the case where an LDO cannot be used and a switching regulator is required, switching noise introduced into the system must be taken into account. To reduce its affect, TI recommends using a high PoC voltage. As the PoC voltage rises, current consumption by the switching regulator is reduced and with it the noise introduced from switching.

Another way to reduce the effect of noise is to use a switching regulator with a higher switching frequency. A higher switching frequency would increase the effect of the decoupling capacitors because their impedance is lowered as frequency increases. Figure 17 shows decoupling capacitors C1 and C2; with higher switching frequency these capacitors become more effective. And finally increasing the decoupling capacitance at V_{PoC} can help to better filter any high frequency noise added introduced by the regulator. Equation 2 shows the impedance of a capacitor as a function of frequency where Z is the impedance in ohms, f is the frequency in hertz and C is the capacitance in Farads. The capacitance and frequency are in the denominator, which means increasing either will decrease the impedance and therefore short high frequencies to ground. When choosing decoupling capacitors it is important to select high quality capacitors rated for the voltage and temperature range required. Some capacitors can significantly degrade when operated near their rated voltage. Sometimes the capacity can drop as low as 20 – 40% of the nominal rating. For this reason TI recommends selecting capacitors with a voltage rating 2x or 3x the voltage they will be used at to avoid any unexpected drop in capacitance.

7 TI Approved PoC Networks

This section provides all the TI approved PoC networks. TI recommends selecting one of the networks based on the desired frequency range, current rating, and temperature

Vendor	Network	Frequency Range	Current Rating	Temperature Rating
N/A	From 9702 Datasheet	25MHz – 4.2GHz	150mA	105°C
Murata	Solution 1	5MHz – 5GHz	800mA	105°C
	Solution 2	5MHz – 5GHz	825mA	105°C
	Solution 3	1MHz – 1GHz	300mA	105°C
TDK	Solution 1	5MHz – 4.2GHz	300mA	105°C
			300mA	115°C
	Solution 2	5MHz – 4.2GHz	600mA	105°C
			300mA	115°C
	Solution 3	5MHz – 4.2GHz	300mA	105°C
			200mA	115°C
	Solution 4	5MHz – 4.2GHz	1000mA	115°C
	Solution 5	5MHz – 4.2GHz	600mA	115°C
	Solution 6	5MHz – 4.2GHz	600mA	115°C
	Solution 7	1MHz – 1GHz	300mA	105°C
	Solution 8	1MHz – 1GHz	400mA	105°C
Coilcraft	Solution 1	1MHz – 5GHz	300mA	125°C
	Solution 2	1MHz – 5GHz	300mA	125°C
	Solution 3	1MHz – 5GHz	800mA	125°C
	Solution 4	1MHz – 5GHz	1200mA	125°C

Table 4 Approved Networks Operating Ratings

7.1 PoC Network from DS90UB9702-Q1 Datasheet

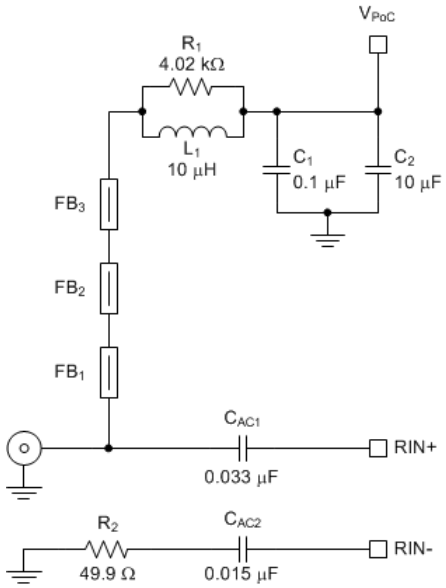

Figure 17 Recommended PoC Network from DS90UB9702-Q1 Datasheet

Designator	Description	Part Number	Vendor
L1	Inductor, 10 µH, 0.288 Ω max, 530 mA MIN(Isat, Itemp) 30 MHz SRF min, 3 mm x 3 mm, AEC-Q200	LQH3NPZ100MJR	Murata
	Inductor, 10 µH, 0.360 Ω max, 450 mA MIN(Isat, Itemp) 30 MHz SRF min, 3.2 mm x 2.5 mm, AEC-Q200	NLCV32T-100K-EFD	TDK
	Inductor, 10 µH, 0.400 Ω typ, 550 mA MIN(Isat, Itemp) 39 MHz SRF typ, 3 mm x 3 mm, AEC-Q200	TYS3010100M-10	Laird
	Inductor, 10 µH, 0.325 Ω max, 725 mA MIN(Isat, Itemp) 41 MHz SRF typ, 3 mm x 3 mm, AEC-Q200	TYS3015100M-10	Laird
FB1 – FB3	Ferrite Bead, 1.5 kΩ at 1 GHz, 0.5 Ω max @ DC 500 mA at 85°C, 0603 SMD , AEC-Q200	BLM18HE152SZ1	Murata

Table 5 Suggested PoC Network Components

7.2 Murata Networks

7.2.1 Solution 1

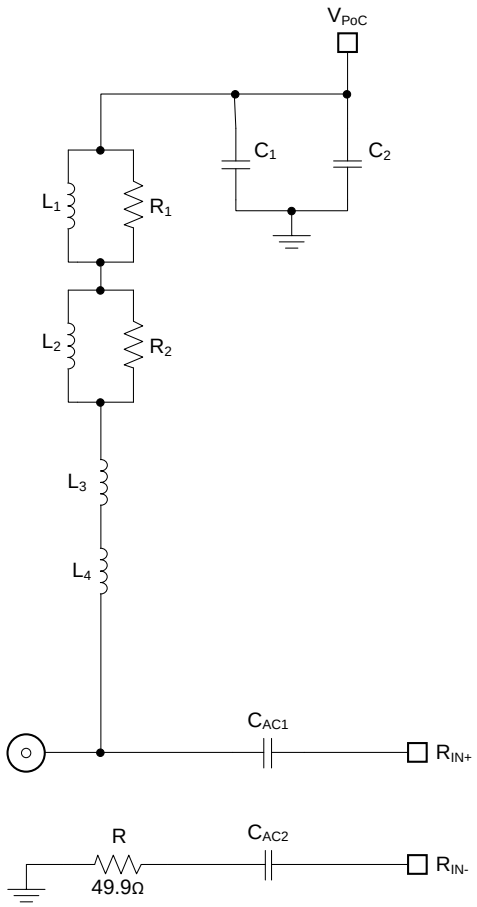

Figure 18 Murata PoC Network No. 1 Schematic

Designator	Description	Part Number	Vendor
L1	Inductor, 10uH	LQH3NPZ100MME	Murata
L2	Inductor, 3.3uH	LQW32FT3R3	
L3	Inductor, 120 nH	LQW18CNR12	
L4			
R1	1.5 kOhm		
R2	3 kOhm		

Table 6 Murata PoC Network 1 Components

7.2.2 Solution 2

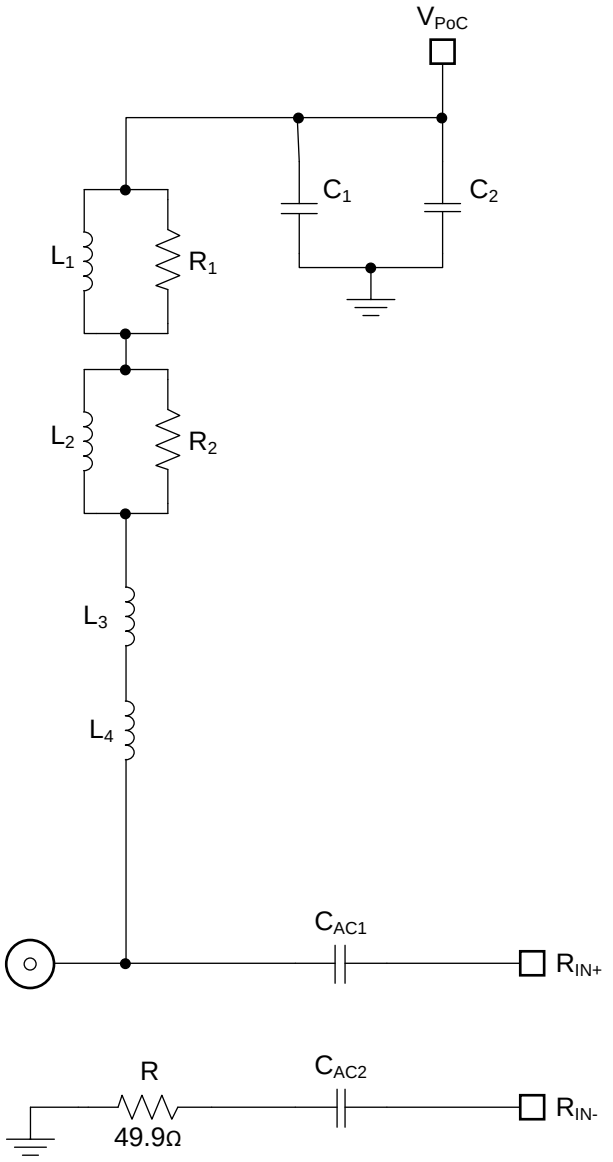

Figure 19 Murata PoC Network No. 2 Schematic

Designator	Description	Part Number	Vendor
L1	Inductor, 6.8uH	LQH3NPZ6R8MME	Murata
L2	Inductor, 3.3uH	LQW32FT3R3	
L3	Inductor, 120 nH	LQW18CNR12	
L4			
R1	1.5 kOhm		
R2	3 kOhm		

Table 7 Murata PoC Network 2 Components

7.2.3 Solution 3

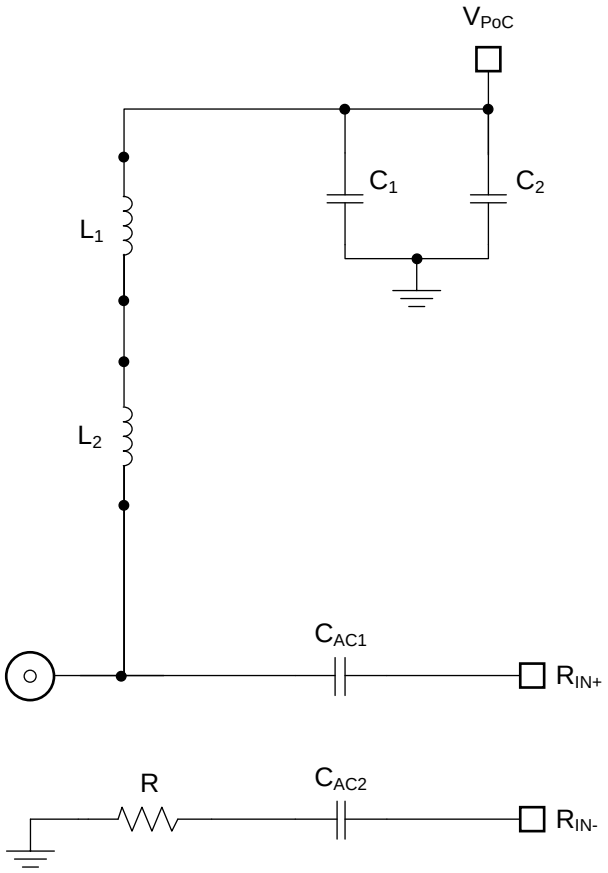

Figure 20 Murata PoC Network No. 3 Schematic

Designator	Description	Part Number	Vendor
L1	Inductor, 47uH	LQW32FT470	Murata
L2	Inductor, 2uH	LQW21FT2R0	

Table 8 Murata PoC Network 3 Components

7.3 TDK Networks

7.3.1 Solution 1

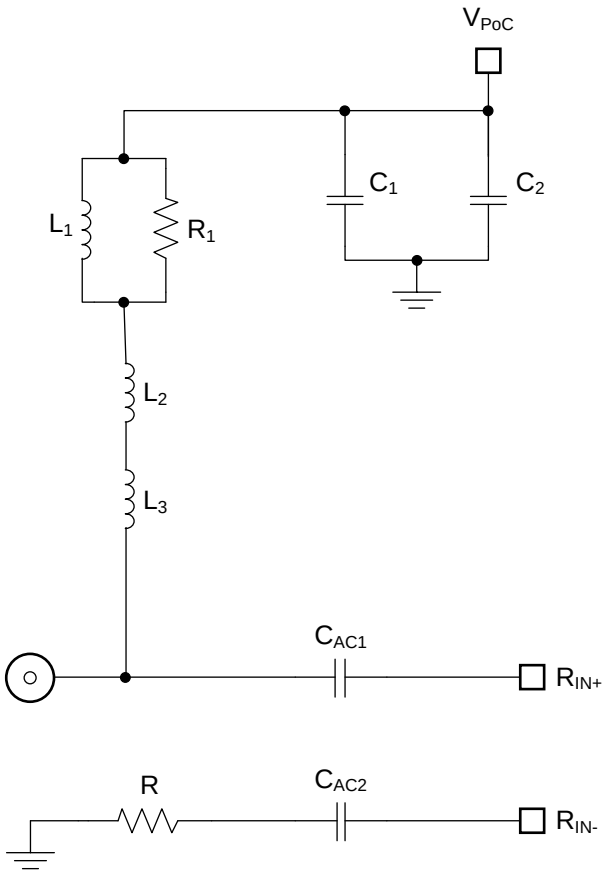

Figure 21 TDK PoC Network No. 1 Schematic

Designator	Description	Part Number	Vendor
L1	Inductor, 10uH	ADL3225VT-100M	TDK
L2	Inductor, 1.5uH	ADL2012-1R5M	
L3			
R1	1.2 kOhm	-	-

Table 9 TDK PoC Network 1 Components

7.3.2 Solution 2

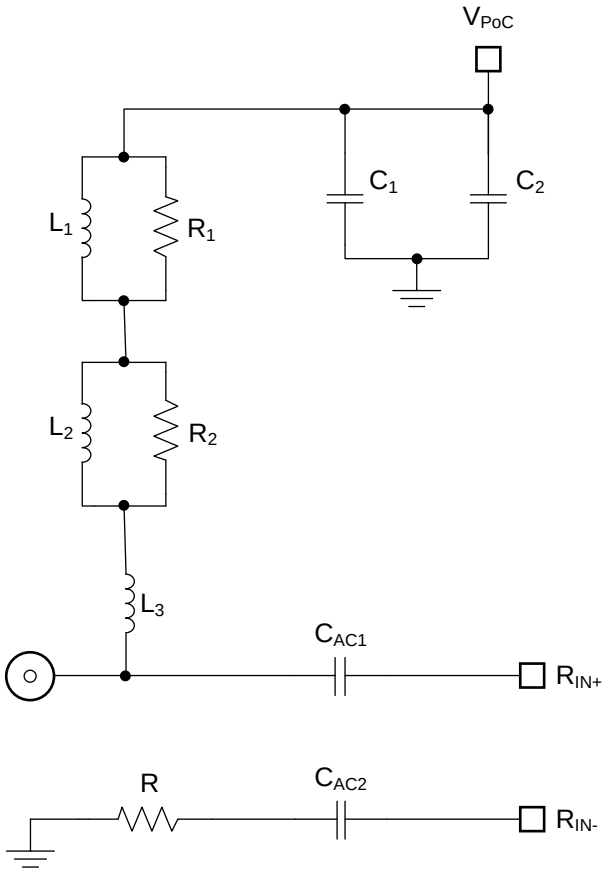

Figure 22 TDK PoC Network No. 2 Schematic

Designator	Description	Part Number	Vendor
L1	Inductor 10uH	ADM32FSC-100M	TDK
L2	Inductor, 1.5uH	ADL2012-1R5M	
L3			
R1	3 kOhm		
R2	1.5 kOhm		

Table 10 TDK PoC Network 2 Components

7.3.3 Solution 3

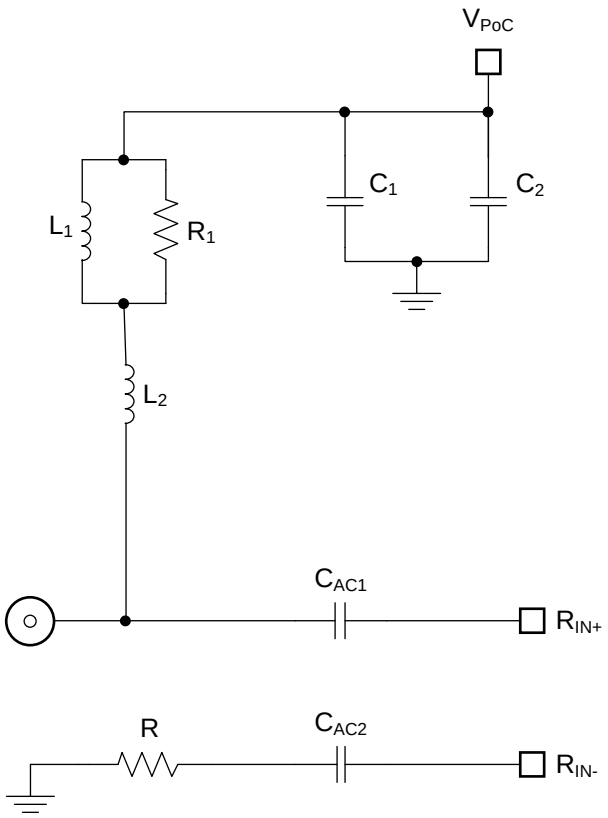

Figure 23 TDK PoC Network No. 3 Schematic

Designator	Description	Part Number	Vendor
L1	Inductor, 10uH	ADL3225VT-100M	TDK
L2	Inductor, 2.2uH	ADL2012-2R2M	
R1	1.2kOhm		

Table 11 TDK PoC Network 3 Components

7.3.4 Solution 4

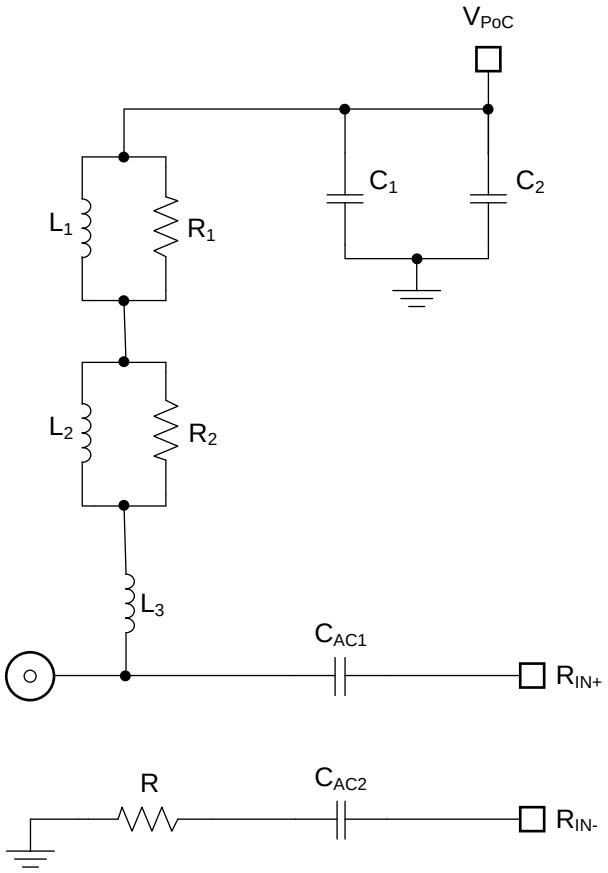

Figure 24 TDK PoC Network No. 4 Schematic

Designator	Description	Part Number	Vendor
L1	Inductor, 10uH	ADM45FDC-100M	TDK
L2	Inductor, 2.2uH	ADL3225VM-2R2M	
L3			
R1	1kOhm		
R2			

Table 12 TDK PoC Network 4 Components

7.3.5 Solution 5

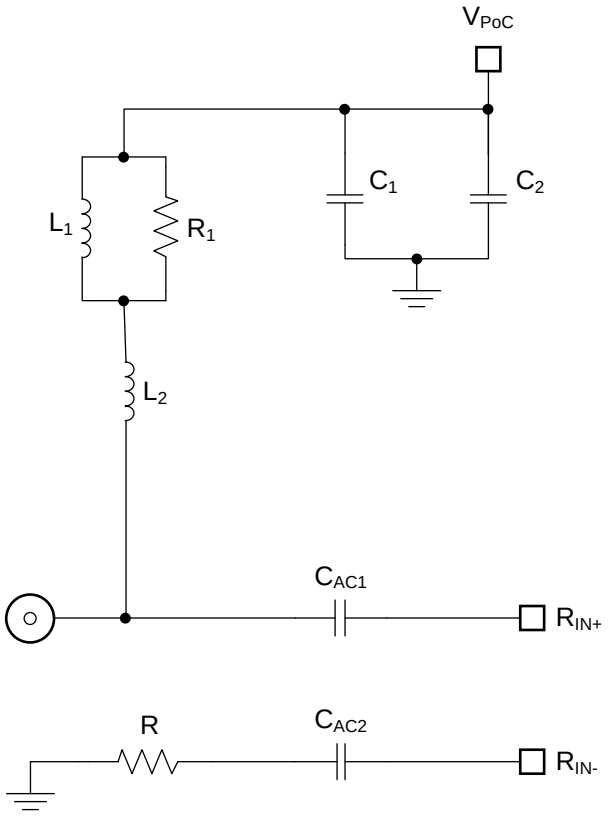

Figure 25 TDK PoC Network No. 5 Schematic

Designator	Description	Part Number	Vendor
L1	Inductor 10uH	ADM32FSC-100M	TDK
L2	Inductor, 2.2uH	ADL3225VM-2R2M	
R1	1kOhm		

Table 13 TDK PoC Network 5 Components

7.3.6 Solution 6

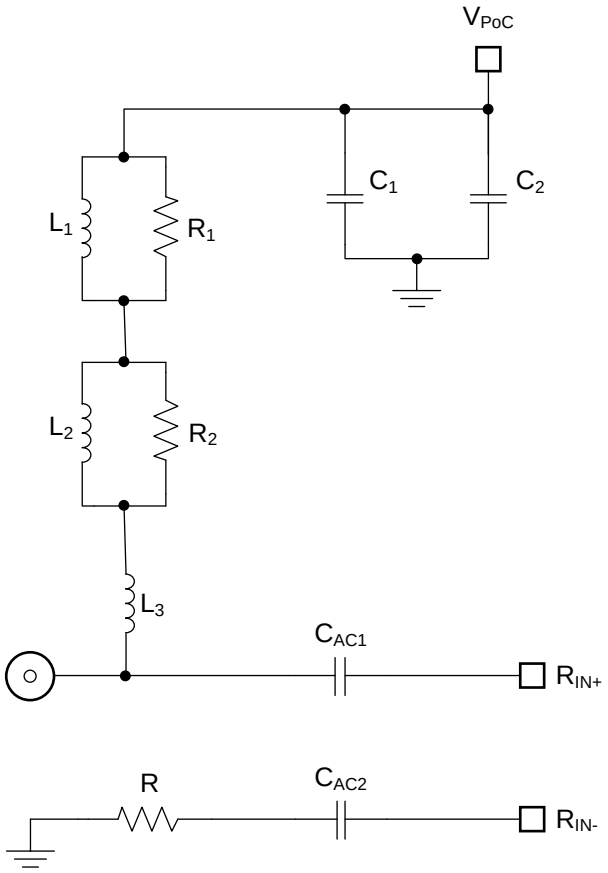

Figure 26 TDK PoC Network No. 6 Schematic

Designator	Description	Part Number	Vendor
L1	Inductor 10uH	ADM32FSC-100M	TDK
L2	Inductor, 2.2uH	ADL3225VM-2R2M	
L3			
R1	1kOhm		
R2			

Table 14 TDK PoC Network 6 Components

7.3.7 Solution 7

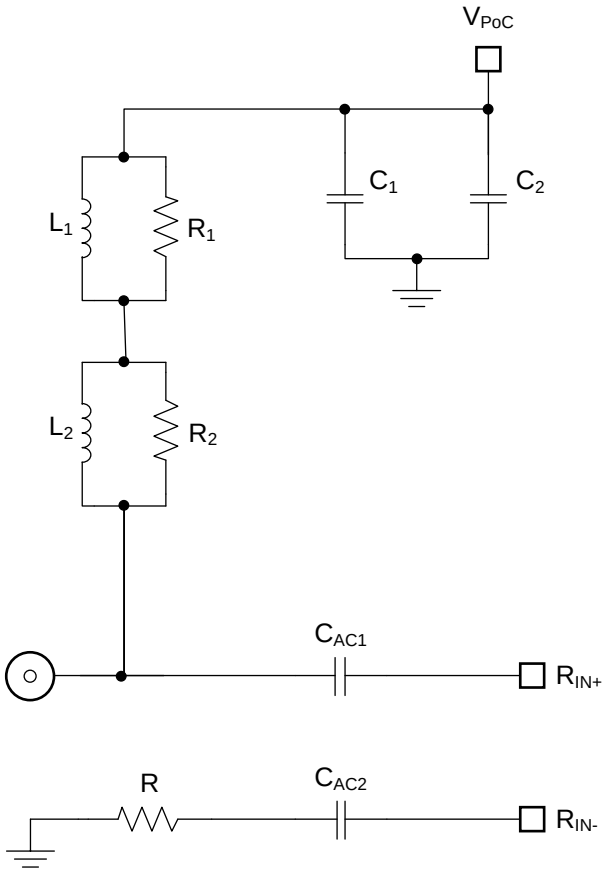

Figure 27 TDK PoC Network No. 7 Schematic

Designator	Description	Part Number	Vendor
L1	Inductor, 47uH	VLS3015CX-470M-H	TDK
L2	Inductor, 2.2uH	ADL2012-2R2M	
R1	1kOhm		
R2	2kOhm		

Table 15 TDK PoC Network 7 Components

7.3.8 Solution 8

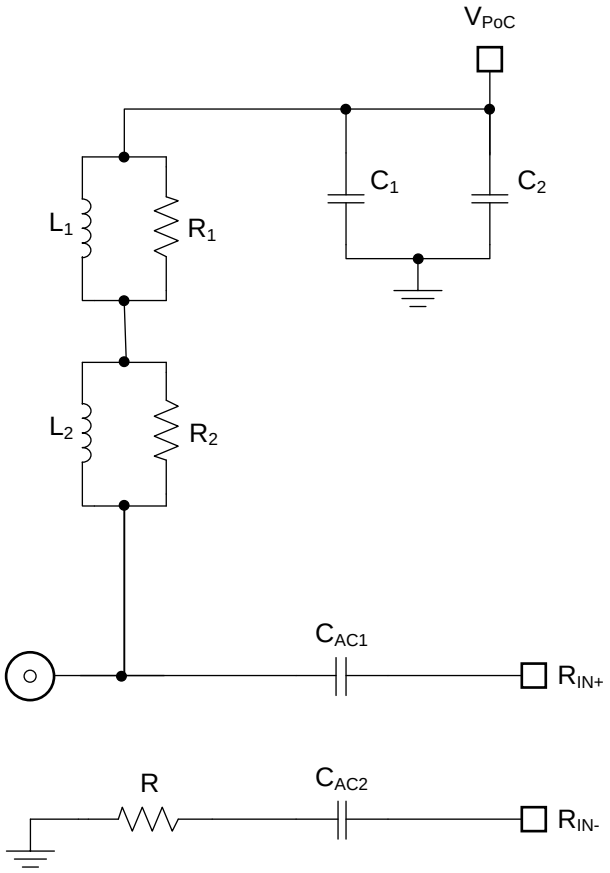

Figure 28 TDK PoC Network No. 8 Schematic

Designator	Description	Part Number	Vendor
L1	Inductor, 100uH	VLS5045EX-101M-H	TDK
L2	Inductor, 2.2uH	ADL2012-2R2M	
R1	1kOhm		
R2	2kOhm		

Table 16 TDK PoC Network 8 Components

7.4 Coilcraft Networks

7.4.1 Solution 1

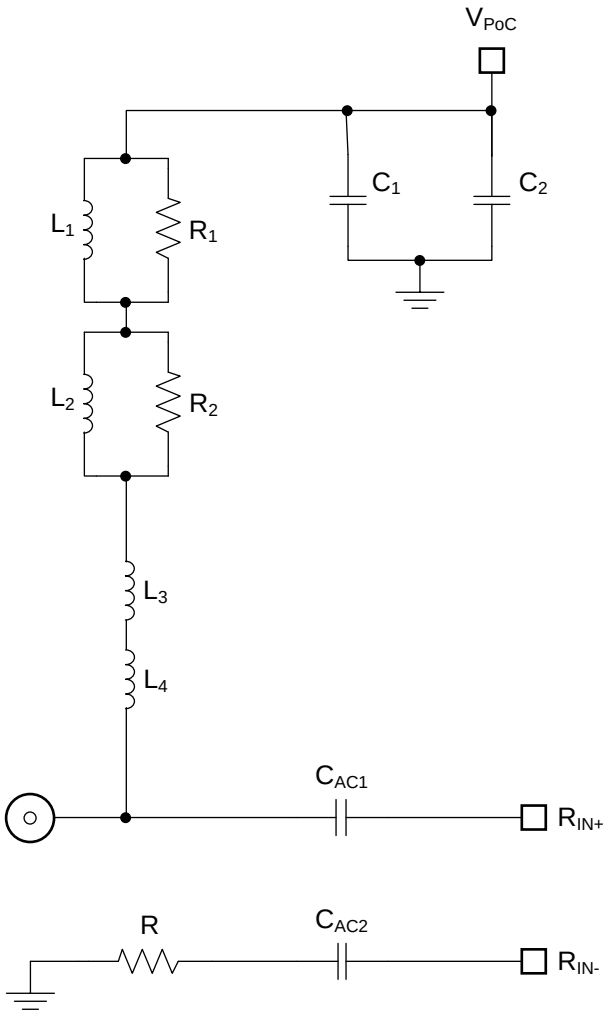

Figure 29 Coilcraft PoC Network No. 1 Schematic

Designator	Description	Part Number	Vendor
L1	Inductor, 100uH	MSS5131H-104	Coilcraft
L2	Inductor, 6.8uH	1210POC-682	
L3	Inductor, 100nH	PFL1005-101	
L4			
R1	3kΩ		
R2	3.6kΩ		

Table 17 Coilcraft PoC Network 1 Components

7.4.2 Solution 2

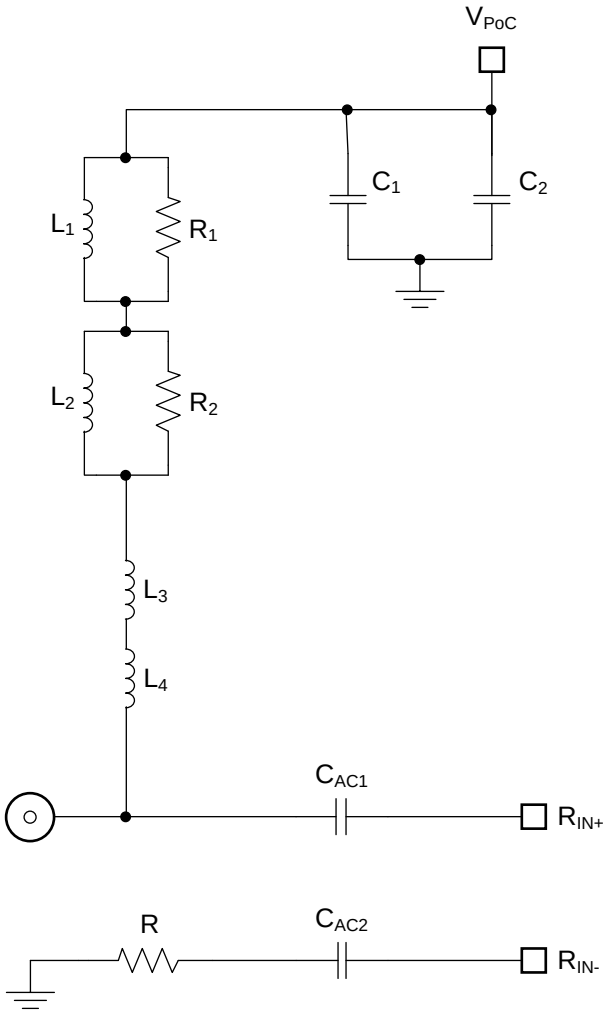

Figure 30 Coilcraft PoC Network No. 2 Schematic

Designator	Description	Part Number	Vendor
L1	Inductor, 100uH	LPS4018-104	Coilcraft
L2	Inductor, 6.8uH	1205POC-682	
L3	Inductor, 180 nH	PFL1005-181	
L4			
R1	2.61kOhm		
R2	3.6kOhm		

Table 18 Coilcraft PoC Network 2 Components

7.4.3 Solution 3

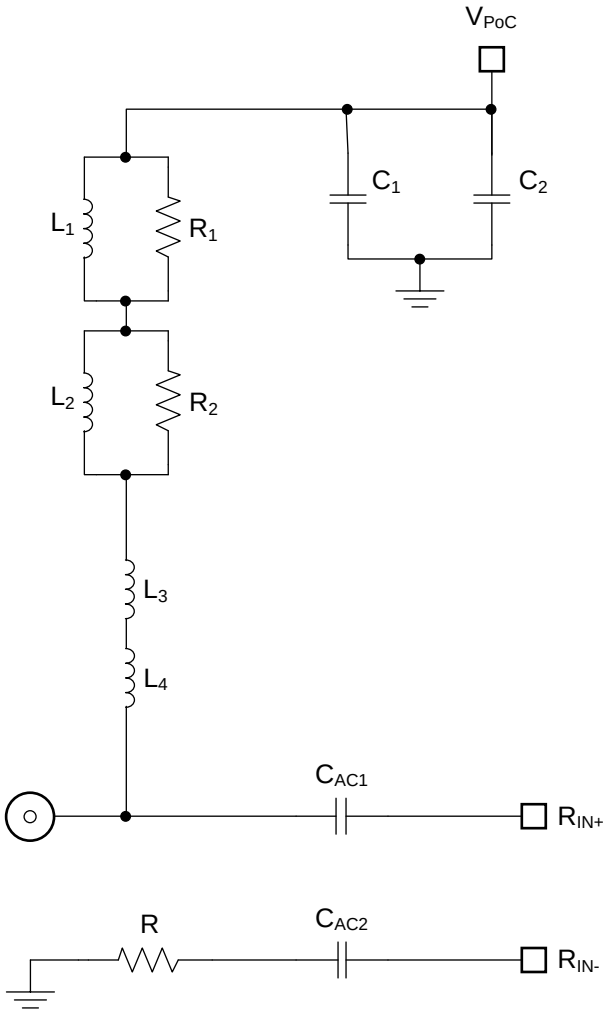

Figure 31 Coilcraft PoC Network No. 3 Schematic

Designator	Description	Part Number	Vendor
L1	Inductor, 100uH	MSS1048T-104	Coilcraft
L2	Inductor, 10uH	1812PS-103	
L3	Inductor, 470nH	PFL2010-471	
L4	Inductor, 150nH	0402DF-151	
R1	2.55kΩ		
R2	3kΩ		

Table 19 Coilcraft PoC Network 3 Components

7.4.4 Solution 4

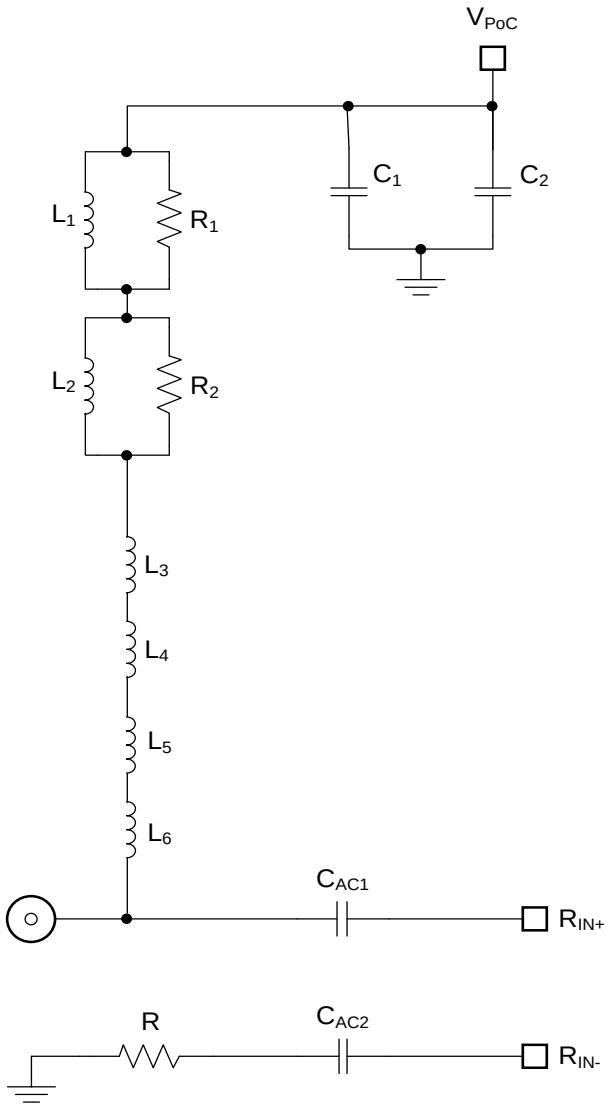

Figure 32 Coilcraft PoC Network No. 4 Schematic

Designator	Description	Part Number	Vendor
L1	Inductor, 100uH	MSS1048T-104	Coilcraft
L2	Inductor, 22uH	MSS6132T-223	
L3	Inductor, 5.6uH	1812PS-562	
L4	Inductor, 470nH	PFL2010-471	
L5	Inductor, 20nH	0402DF-200	
L6			
R1	3kΩ		
R2	2kΩ		

Table 20 Coilcraft PoC Network 4 Components

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