# PCI2050B

## Implementation Guide

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TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

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# 1. Introduction

This document is provided to assist platform developers who are using the PCI2050B PCI-to-PCI bridge controller.

Chapter 2 is a list of the features of the PCI2050B.

Chapter 3 is a listing of the device terminals with corresponding signal names for each terminal.

Chapter 4 includes the electrical guidelines. This chapter explains the pull-up resistors and voltage level capacitors required for proper implementation of the PCI2050B. The PCI specification requires all signals to be driven to a known level. This is accomplished with pull-up resistors or by the PCI device. Some small capacitors are recommended on the power connections of the PCI2050B. This is standard practice in PCB design to provide a stable supply voltage when large loads are placed on the system.

Chapter 5 describes a number of functional considerations in implementing a PCI2050B solution, including bus speed configuration, proper use of an external arbiter, an explanation of how PCI interrupts and IDSEL mapping interrelate, how to implement PCI hot-swap with the PCI2050B, implementing PCI power management, and an explanation of the GPIO interface.

## 2. PCI2050B Feature Set

The PCI2050B provides the following features.

- Supports PCI Local Bus Specification Revision 2.2 and PCI-PCI Bridge Specification Revision 1.1
- 3.3-V core logic with universal PCI interfaces compatible with 3.3-V and 5-V PCI signaling environments
- Supports two 32-bit PCI buses at the following speeds:
  - 33 MHz primary / 33 MHz secondary
  - 66 MHz primary / 33 MHz secondary
  - 66 MHz primary / 66 MHz secondary
- Provides internal arbitration for up to nine external secondary bus masters with programmable control
- Provides ten secondary PCI bus clock outputs
- Supports a range of sustained pass-through bandwidth from 132 to 264 Mbps
- Packaged in advanced technology 208 Pin LQFP
- External arbiter option
- Support for bus locking
- Support for CompactPCI™ hot-swap
- Independent read and write buffers upstream and downstream
- Provides VGA/palette decoding options

# 3. Terminal Assignments

**Table 3-1. 208-Pin LQFP Signal Names Sorted by Terminal Number**

| No. | Terminal Name | No. | Terminal Name | No. | Terminal Name | No. | Terminal Name |
|---|---|---|---|---|---|---|---|
| 1 | VCC | 53 | VCC | 105 | VCC | 157 | VCC |
| 2 | S_REQ#[1] | 54 | GND | 106 | MS1 | 158 | GND |
| 3 | S_REQ#[2] | 55 | P_AD[29] | 107 | P_AD[9] | 159 | S_AD[11] |
| 4 | S_REQ#[3] | 56 | VCC | 108 | VCC | 160 | GND |
| 5 | S_REQ#[4] | 57 | P_AD[28] | 109 | P_AD[8] | 161 | S_AD[12] |
| 6 | S_REQ#[5] | 58 | P_AD[27] | 110 | P_CBE#[0] | 162 | S_AD[13] |
| 7 | S_REQ#[6] | 59 | GND | 111 | GND | 163 | VCC |
| 8 | S_REQ#[7] | 60 | P_AD[26] | 112 | P_AD[7] | 164 | S_AD[14] |
| 9 | S_REQ#[8] | 61 | P_AD[25] | 113 | P_AD[6] | 165 | S_AD[15] |
| 10 | S_GNT#[0] | 62 | VCC | 114 | VCC | 166 | GND |
| 11 | S_GNT#[1] | 63 | P_AD[24] | 115 | P_AD[5] | 167 | S_CBE#[1] |
| 12 | GND | 64 | P_CBE#[3] | 116 | P_AD[4] | 168 | S_PAR |
| 13 | S_GNT#[2] | 65 | P_IDSEL | 117 | GND | 169 | S_SERR# |
| 14 | S_GNT#[3] | 66 | GND | 118 | P_AD[3] | 170 | VCC |
| 15 | S_GNT#[4] | 67 | P_AD[23] | 119 | P_AD[2] | 171 | S_PERR# |
| 16 | S_GNT#[5] | 68 | P_AD[22] | 120 | VCC | 172 | S_LOCK# |
| 17 | S_GNT#[6] | 69 | VCC | 121 | P_AD[1] | 173 | S_STOP# |
| 18 | S_GNT#[7] | 70 | P_AD[21] | 122 | P_AD[0] | 174 | GND |
| 19 | S_GNT#[8] | 71 | P_AD[20] | 123 | GND | 175 | S_DEVSEL# |
| 20 | GND | 72 | GND | 124 | P_VIO | 176 | S_TRDY# |
| 21 | S_CLK | 73 | P_AD[19] | 125 | CONFIG66 | 177 | S_IRDY# |
| 22 | S_RST# | 74 | P_AD[18] | 126 | MSK_IN | 178 | VCC |
| 23 | S_CFN# | 75 | VCC | 127 | HSENUM# | 179 | S_FRAME# |
| 24 | HSSWITCH/GPIO[3] | 76 | P_AD[17] | 128 | HSLED | 180 | S_CBE#[2] |
| 25 | GPIO[2] | 77 | P_AD[16] | 129 | TDI | 181 | GND |
| 26 | VCC | 78 | GND | 130 | TDO | 182 | S_AD[16] |
| 27 | GPIO[1] | 79 | P_CBE#[2] | 131 | VCC | 183 | S_AD[17] |
| 28 | GPIO[0] | 80 | P_FRAME# | 132 | TMS | 184 | VCC |
| 29 | S_CLKOUT[0] | 81 | VCC | 133 | TCK | 185 | S_AD[18] |
| 30 | S_CLKOUT[1] | 82 | P_IRDY# | 134 | TRST# | 186 | S_AD[19] |
| 31 | GND | 83 | P_TRDY3 | 135 | S_VIO | 187 | GND |
| 32 | S_CLKOUT[2] | 84 | P_DEVSEL# | 136 | GND | 188 | S_AD[20] |
| 33 | S_CLKOUT[3] | 85 | P_STOP# | 137 | S_AD[0] | 189 | S_AD[21] |
| 34 | VCC | 86 | GND | 138 | S_AD[1] | 190 | VCC |
| 35 | S_CLKOUT[4] | 87 | P_LOCK# | 139 | VCC | 191 | S_AD[22] |
| 36 | S_CLKOUT[5] | 88 | P_PERR# | 140 | S_AD[2] | 192 | S_AD[23] |
| 37 | GND | 89 | P_SERR# | 141 | S_AD[3] | 193 | GND |
| 38 | S_CLKOUT[6] | 90 | P_PAR | 142 | GND | 194 | S_CBE#[3] |
| 39 | S_CLKOUT[7] | 91 | VCC | 143 | S_AD[4] | 195 | S_AD[24] |
| 40 | VCC | 92 | P_CBE#[1] | 144 | S_AD[5] | 196 | VCC |
| 41 | S_CLKOUT[8] | 93 | P_AD[15] | 145 | VCC | 197 | S_AD[25] |
| 42 | S_CLKOUT[9] | 94 | GND | 146 | S_AD[6] | 198 | S_AD[26] |
| 43 | P_RST# | 95 | P_AD[14] | 147 | S_AD[7] | 199 | GND |
| 44 | BPCCE | 96 | P_AD[13] | 148 | GND | 200 | S_AD[27] |
| 45 | P_CLK | 97 | VCC | 149 | S_CBE#[0] | 201 | S_AD[28] |
| 46 | P_GNT# | 98 | P_AD[12] | 150 | S_AD[8] | 202 | VCC |
| 47 | P_REQ# | 99 | P_AD[11] | 151 | VCC | 203 | S_AD[29] |
| 48 | GND | 100 | GND | 152 | S_AD[9] | 204 | S_AD[30] |
| 49 | P_AD[31] | 101 | P_AD[10] | 153 | S_M66ENA | 205 | GND |
| 50 | P_AD[30] | 102 | P_M66ENA | 154 | S_AD[10] | 206 | S_AD[31] |
| 51 | VCC | 103 | VCC | 155 | MS0 | 207 | S_REQ#[0] |
| 52 | GND | 104 | GND | 156 | GND | 208 | VCC |

# 4. Electrical Guidelines

## 4.1 Pull-up Resistors

This discussion on PCI pull-up requirements is taken from the PCI Specification Rev 2.2, and is provided for reference in designing in the PCI2050B.

PCI control signals always require pull-up resistors on the motherboard (NOT the expansion board) to ensure that they contain stable values when no agent is actively driving the bus. This includes, FRAME#, TRDY#, IRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, INTA#, INTB#, INTC#, INTD#, and when used, REQ64#, and ACK64#. The point-to-point and shared 32-bit signals do not require pull-ups; bus parking ensures their stability.

**Table 4-1. Minimum and Typical PCI Pull-Up Resistor Values**

| Signaling Rail | $R_{MIN}$ | $R_{TYPICAL}$ | $R_{MAX}$ |
|---|---|---|---|
| 5V | 963 W | 2.7 kΩ @ 10% | Dependent on # loads. Equation below. |
| 3.3V | 2.42 kW | 8.2 kΩ @ 10% | Dependent on # loads. Equation below. |

Equation to calculate $R_{max}$:

$\mathbf{R_{MAX}} = [V_{CC(MIN)} - V_X] / [num\_loads \times I_{IH}]$ ; where $V_X = 2.7V$ for 5V signaling, and $V_X = 2.3V$ for 3.3V signaling.

Because the PCI2050B is not a 64 bit device, it does not have S_ACK64# or S_REQ64# pins. These signals are needed on the secondary PCI bus if there is a device which requires them or if expansion slots are provided on the secondary bus. In these cases, the S_ACK64# and S_REQ64# signals should have pull-up resistors to ensure that all devices know the bus is 32 bits wide. The table below contains both PCI control signals and other PCI2050B specific signals that should have pull-up (keeper) resistors. Texas Instruments also recommends that the signals be pulled up to 3.3 V to reduce leakage current.

**Table 4-2. PCI2050B Pull-ups**

| Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name |
|---|---|---|---|---|---|
| 175 | S_DEVSEL# | 207 | S_REQ0# | 7 | S_REQ6# |
| 176 | S_TRDY# | 2 | S_REQ1# | 8 | S_REQ7# |
| 179 | S_FRAME# | 3 | S_REQ2# | 9 | S_REQ8# |
| 177 | S_IRDY# | 4 | S_REQ3# | 22 | S_RST# |
| 172 | S_LOCK# | 5 | S_REQ4# | 169 | S_SERR# |
| 171 | S_PERR# | 6 | S_REQ5# | 173 | S_STOP# |

The signals in Table 4-3 may need pull-ups. The designer should refer to the section related to the signal to determine if a pull-up resistor is necessary.

**Table 4-3. Optional Pull-ups**

| Pin No. | Pin Name | Refer to Section On | Pin No. | Pin Name | Refer to Section On |
|---|---|---|---|---|---|
| 23 | S_CFN# | External Arbiter | 28 | GPIO0 | GPIO Interface |
| 127 | HS_ENUM# | cPCI Hot Swap | 126 | MSK_IN | GPIO Interface |
| 24 | GPIO3/ HS_SWITCH# | GPIO Interface/ cPCI Hot Swap | 125 | CONFIG66 | Bus Speed Configuration |
| 25 | GPIO2 | GPIO Interface | 153 | S_M66ENA# | Bus Speed Configuration |
| 27 | GPIO1 | GPIO Interface | | | |

The signals listed in Table 4-4 can be hardwired to GND or 3.3 V if they are not going to be used in the design. Texas Instruments strongly recommends that all active low signals listed in Table 4-4 be hardwired to 3.3 V if they are not used. All other signals can be hardwired to GND or 3.3 V.

**Table 4-4. Signals Which Could be Hardwired to GND or 3.3 V**

| Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name |
|---|---|---|---|---|---|
| 207 | S_REQ0# | 6 | S_REQ5# | 24 | HS_SWITCH/GPIO3 |
| 2 | S_REQ1# | 7 | S_REQ6# | 25 | GPIO2 |
| 3 | S_REQ2# | 8 | S_REQ7# | 27 | GPIO1 |
| 4 | S_REQ3# | 9 | S_REQ8# | 28 | GPIO0 |
| 5 | S_REQ4# | | | | |

## 4.2 Power and Signal Levels

The PCI2050B supports both 3.3-V and 5-V signaling environments. This is accomplished using the P_VCCP and S_VCCP clamping rails. These two rails are not power rails. They only clamp the signals at the rail voltage (3.3 V or 5 V). All I/O buffers are powered by the VCC rail. Because VCC powers both the core and the I/O buffers, it must always be at 3.3 V. The table below depicts the signaling combinations supported by the PCI2050B and the P_VCCP and S_VCCP voltages needed to operate in these signaling environments.

**Table 4-5. VCC Combinations Based on Signaling Environment**

| Primary Bus Signaling Environment [V] | Secondary Bus Signaling Environment [V] | P_VCCP [V] | S_VCC [V] | VCC [V] |
|---|---|---|---|---|
| 5 | 5 | 5 | 5 | 3.3 |
| 5 | 3.3 | 5 | 3.3 | 3.3 |
| 3.3 | 5 | 3.3 | 5 | 3.3 |
| 3.3 | 3.3 | 3.3 | 3.3 | 3.3 |

Table 4-6 shows the power measurements for the PCI2050B. Measurements were taken at VCC = 3.3V, P_VCCP = 5.0V, and S_VCCP = 3.3V. Typical measurements were taken with a 66 MHz capable SCSI adapter and hard drive on the secondary bus. Maximum measurements were taken using bus exercisers toggling the address/data lines between 0 and 1. A measurement of 0 means the current drawn is negligible.

**Table 4-6. PCI2050B Power Measurements**

| Conditions | Power State | $I_{VCC}$ (typ) | $I_{VCC}$ (max) | $I_{P\ VCCP}$ (typ) | $I_{S\ VCCP}$ (typ) |
|---|---|---|---|---|---|
| Primary Bus Frequency = 33 MHz<br>Secondary Bus Frequency = 33 MHz | D0 | 37.0 mA | 169 mA | 10 µA | 0 |
| | D1 | 37.0 mA | | 10 µA | 0 |
| | D2 | 12.4 mA | | 10 µA | 0 |
| | $D3_{Hot}$ | 12.4 mA | | 10 µA | 0 |
| Primary Bus Frequency = 66 MHz<br>Secondary Bus Frequency = 33 MHz | D0 | 43.5 mA | 189 mA | 27 µA | 0 |
| | D1 | 43.5 mA | | 27 µA | 0 |
| | D2 | 20.7 mA | | 27 µA | 0 |
| | $D3_{Hot}$ | 20.7 mA | | 27 µA | 0 |
| Primary Bus Frequency = 66 MHz<br>Secondary Bus Frequency = 66 MHz | D0 | 61.0 mA | 234 mA | 27 µA | 17 µA |
| | D1 | 61.0 mA | | 27 µA | 17 µA |
| | D2 | 20.5 mA | | 27 µA | 0 |
| | $D3_{Hot}$ | 20.5 mA | | 27 µA | 0 |

## 4.3 Bypass Capacitors

Standard design rules for the supply bypass should be followed. Low inductance ceramic chip capacitors are best for bypass capacitors. A value of 0.1 uF is recommended for each of the power supply pins VCC, P_VCCP, and S_VCCP. The designer should also include a 0.01 uF capacitor located within 0.25 inches of the P_M66EN pin on the add-in connector.

## 4.4 Secondary Clocks

The PCI2050B has ten secondary clocks. Each secondary clock can be enabled or disabled through the Secondary Clock Control Register located at PCI offset 68h. We suggest the configuration software or BIOS disable any clocks which are not in use to conserve power. When a secondary clock is disabled, the PCI2050B will drive the clock signal low until the clock is re-enabled. Texas Instruments also recommends the use of a 50Ω series terminator resistor to be connected to each secondary clock to reduce reflections.

The S_CLKOUT9 (pin 42) output must be used as the input clock on the S_CLK (pin 21) input terminal. This loop is used to allow the system designer to synchronize the PCI2050B with the other devices on the secondary PCI bus. To ensure that the skew between the S_CLK input and the clock inputs to the secondary devices is minimized, the trace length between S_CLKOUT9 and S_CLK should match the trace length of the other S_CLKOUT traces. If one or more of the S_CLKOUT pins is being routed to a PCI socket (as opposed to an onboard device), then the clock trace lengths to the onboard devices should be 2.5 inches longer than the clock traces to the sockets to compensate for the extra load created by the socket.

# 5. Functional Considerations

## 5.1 Bus Speed Configuration

To enable 66 MHz operation, the CONFIG66 signal must be tied high on the board. This sets the 66 MHz capable bit in the primary and secondary status registers. To be compliant with Intel's 21150 device, P_M66ENA and S_M66ENA should never be pulled high unless CONFIG66 is also high. If CONFIG66 is pulled low, disabling 66 MHz operation, P_M66ENA should also be connected to GND. S_M66ENA can be an open drain output and therefore should have a pull-up resistor.

The signals P_M66ENA and S_M66ENA indicate whether the primary or secondary interfaces are running at 66 MHz. This information is needed to control the frequency of the secondary bus. Note that PCI Local Bus Specification 2.2 restricts clock frequency changes above 33 MHz to during reset only. The following frequency combinations are supported on the primary and secondary buses in PCI2050B:

**Table 5-1. Bus Speed Truth Table**

| P_M66ENA | S_M66ENA | CONFIG66 | Primary Bus Frequency | Secondary Bus Frequency |
|---|---|---|---|---|
| Low | Low | Low | 33 MHz | 33 MHz |
| Low | Low | High | 33 MHz | 33 MHz |
| High | Low | High | 66 MHz | 33 MHz |
| High | Low | High | 66 MHz | 66 MHz |

The PCI2050B does not support 33 MHz primary/66 MHz secondary bus operation. If CONFIG66 is high and P_M66ENA is low, the PCI2050B pulls down S_M66ENA to indicate that the secondary bus is running at 33 MHz.

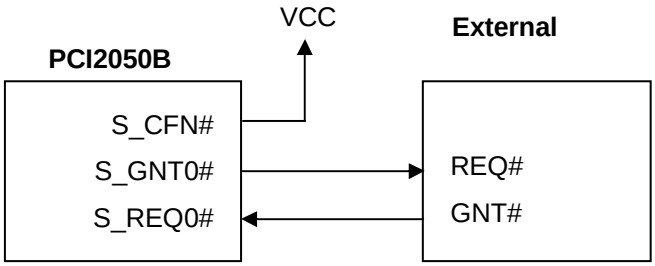
Also note that 66 MHz operation may require tighter tolerances than 33 MHz operation for board layout. For example, not as many loads are allowed and shorter trace lengths are required in a 66 MHz environment. Please refer to PCI Local Bus Specification 2.2 for more information.

## 5.2 External Arbiter

The PCI2050B allows an external arbiter to be used in place of the default internal arbiter. This function is controlled by S_CFN# (pin 23). In order to use an external arbiter with the PCI2050B, S_CFN# must be pulled up with a 10kΩ resistor or hardwired to 3.3 V. If an external arbiter is not going to be used (the PCI2050B internal arbiter will be used instead), then S_CFN# must be hardwired to GND.

When an external secondary bus arbiter is used, the PCI2050B internally reconfigures the S_REQ0# and S_GNT0# signals so that S_REQ0# becomes the secondary bus master grant for the bridge and S_GNT0# becomes the secondary bus master request for the PCI2050B. This is done because S_REQ0# is an input and can thus be used to provide the grant input to the bridge and S_GNT0# is an output and can thus provide the request output from the bridge.

**Figure 5-1. External Arbiter**




When an external arbiter is used, all unused secondary bus grant outputs (S_GNT[8:1]#) are in a high impedance state. Any unused secondary bus request lines (S_REQ[8:1]#) should be pulled high or hardwired to 3.3 V to prevent the inputs from oscillating.

## 5.3 PCI Interrupts and IDSEL Mapping

The PCI2050B can support up to four devices on the secondary side. Each device's IDSEL should be connected to a secondary address line (S_AD[31:16]). In order to reduce capacitive load on the secondary address line, the connection can be made through a 1kΩ series resistor.

Because the PCI2050B is a bridge device, all parallel PCI Interrupts on the secondary interface must be routed as sideband signals to the PCI Interrupts on the primary interface. When using multiple devices behind the PCI2050B, a device's ID and how the PCI Interrupts are routed should be a very important consideration in a design. Some operating systems like Windows 95™ expect a device's PCI interrupt to be routed to a specific interrupt on the motherboard based on its ID number. For example if a device's ID is 4 and its PCI INTA# is routed to PCI INTB# on the motherboard, Windows 95 will not configure the device properly. In order to reduce any chance of incompatibilities, we suggest the designer implement the interrupt routing scheme outlined in section 2.2.6 of the *PCI Local Bus Specification Revision 2.2*. The table below summarizes section 2.2.6:

**Table 5-2. Interrupt Routing**

| Device Number on Secondary Bus | Interrupt Pin on Device | Interrupt Pin on Connector |
|---|---|---|
| 0, 4, 8, 16, 20, 24, 28 | INTA#<br>INTB#<br>INTC#<br>INTD# | INTA#<br>INTB#<br>INTC#<br>INTD# |
| 1, 5, 9, 13, 17, 21, 25, 29 | INTA#<br>INTB#<br>INTC#<br>INTD# | INTB#<br>INTC#<br>INTD#<br>INTA# |
| 2, 6, 10, 14, 18, 22, 26, 30 | INTA#<br>INTB#<br>INTC#<br>INTD# | INTC#<br>INTD#<br>INTA#<br>INTB# |
| 3, 7, 11, 15, 19, 23, 27, 31 | INTA#<br>INTB#<br>INTC#<br>INTD# | INTD#<br>INTA#<br>INTB#<br>INTC# |

## 5.4 Mode Selection

The PCI2050B can be programmed to operate in three separate modes TI Compact PCI mode, TI Power Management mode, and Intel 21150 compatible mode.

**Table 5-3. Mode Select Pins Definition**

| MS0 | MS1 | MODE |
|---|---|---|
| 0 | 0 | TI hot-swap |
| 0 | 1 | TI power management |
| 1 | X | Intel™ 21150 compatible |

### 5.4.1 CompactPCI Hot-Swap Mode

When in CompactPCI hot-swap mode GPIO3 / HS_SWITCH# and HS_ENUM# must be pulled up to ensure the proper functionality of the hot swap logic.

## 5.5 PCI Power Management

When using the PCI2050B in a power managed environment, it is important to remember that PME# and 3.3Vaux are sideband signals as far as the bridge is concerned. If any devices on the secondary bus need PME# or 3.3Vaux, these signals must be routed around the bridge.

## 5.6 GPIO Interface

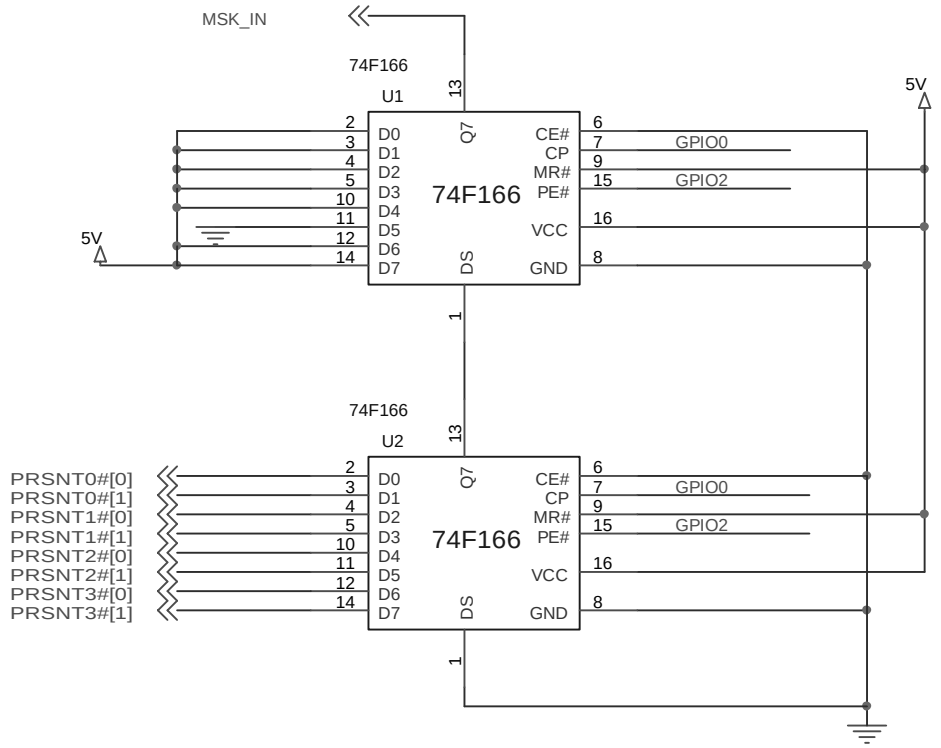
The PCI2050B GPIO pins default to inputs after reset and should be pulled up to prevent oscillation if this interface is not going to be used.

### 5.6.1 Secondary Clock Mask

GPIO0 and GPIO2 can be used to provide the control signals to two external 74F166 shift register to shift data into the secondary clock control register located at PCI offset 68h. If the external shift registers are not used, MSK_IN can be tied low to enable all secondary clocks or tied high to disable all secondary clocks.

The following sample circuit could be used to control the secondary clock outputs for a secondary bus with three PCI slots. D5 through D0 on the first shift register correspond to bits 13 through 8 in the secondary clock control register. In this case, since D5 is grounded, only CLKOUT9 will be turned on. This clock should always be enabled because it goes to the S_CLK input on the 2050B. D7 through D0 on the second shift register correspond to bits 7 through 0 in the clock control register. In this case, these pins are tied to the card present pins on the PCI slots so the clocks will only be turned on if a card is inserted in the slot.

**Figure 5-2. Sample Clock Mask Circuit**




## 5.7 Sample Schematics

For sample schematics see the *PCI2050B Evaluation Module Users Guide.*