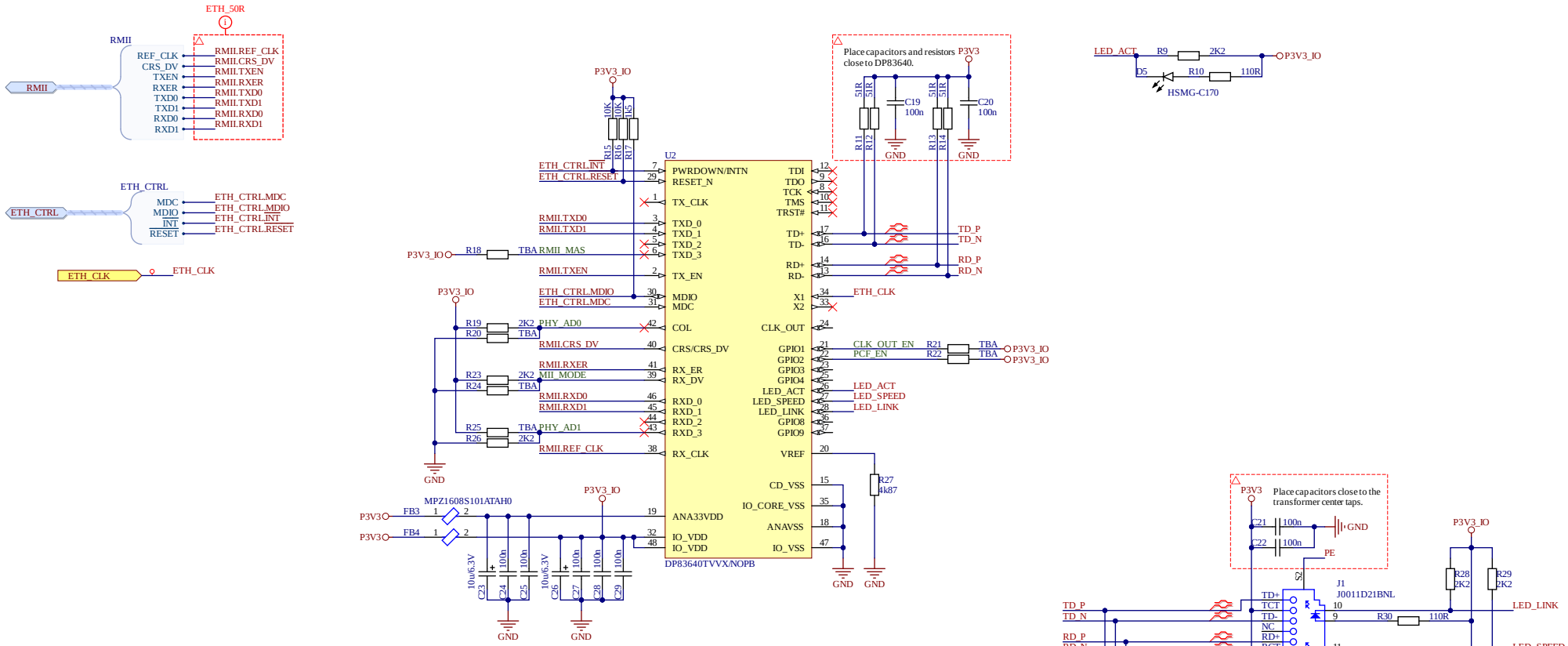
Tento výkres je důsevním vlastnictvím fy ERA a.s. a může být použit jen s jejím souhlasem. Zneužití je trestné.



PHY ADDRESS		
PHY_AD1	PHY_AD0	ADDRESS
0	0	0
0	1	1

AUTO-NEGOTIATION ENABLE
LED_LINK
When high, this enables Auto Negotiation with the capability set by AN0 and AN1 pins

CLK_OUT OUTPUT ENABLE
CLK_OUT_EN
When high, enables clock output on the CLK_OUT pin at power-up.

FX ENABLE
RX_ER
This strapping option enables 100Base-FX (Fiber) mode. This mode is disabled by default

LED CONFIGURATION
CRS/CRS_DV
This strapping option determines the mode of operation of the LED pins. Default is Mode 1

MII MODE SELECT	
MII_MODE	MAC Interface Mode
0	MII Mode
1	RMII Mode

PHY CONTROL FRAME ENABLE
PCF_EN
When high, allows the DP83640 to respond to PHY Control Frames.

RMII MASTER ENABLE
RMII_MAS
When MII_MODE is strapped high, this strapping option enables RMII Master mode

VYVOJOVA VERZE 01

KRESLIL: ccc	SCHVALIL: aaa
PREZKOUSEL: bbb	DNE: 19.08.2024
TYP: MIL/CIV	STARY VYKRES:
NAZEV: Name	NAME: eth.SchDoc
	EMxxxxxxxxxx_xx
	TYP LISTU: 030 LISTU/LIST: 12/8