SN1804044ZBHR USB Type-C and USB-PD Controller, Power Switch, and High-Speed Multiplexer

1 Features

- USB Power Delivery (PD) Controller
  - Mode Configuration for Source (Host), Sink (Device), or Source-Sink
  - Biphase Marked Encoding/Decoding (BMC)
  - Physical Layer (PHY) Protocol
  - Policy Engine
  - Configurable at Boot and Host-Controlled
  - Supports PD2.0 and PD3.0 specifications.
- USB Type-C Specification Compliant
  - Detect USB Cable Plug Attach
  - Cable Orientation and Role Detection
  - Assigns CC and VCONN Pins
  - Advertises Default, 1.5 A or 3 A for Type-C Power
- Port-Power Switch
  - 5-V, 3-A Integrated Switch to VBUS for Type-C Power
  - 5-V, 600-mA Switches for VCONN
  - Overcurrent Limiter, Overvoltage Protector
  - Slew-Rate Control
  - Hard Reset Support
- Port-Data Multiplexer
  - USB 2.0 HS Data, UART Data, and USB Low-Speed Endpoint
  - Sideband Use Data for Alternate Modes (DisplayPort and Thunderbolt™)
- Power Management
  - Gate Control and Current Sense for External 5-V to 20-V, 5-A Bidirectional Switch (Back-to-Back NFETs)
  - Power Supply from 3.3-V or VBUS Source
  - 3.3-V LDO Output for Dead Battery Support
- and Package Options
  - 0.5-mm Pitch
  - Through-Hole Via Compatible for All Pins

2 Applications

- Notebook Computers
- Tablets and Ultrabooks
- Docking Systems
- Charger Adapters
- USB PD Hosts, Devices, and Dual-Role Ports
- USB PD–Enabled Bus-Powered Devices
- DisplayPort, Thunderbolt, and HDMI

3 Description

The SN1804044ZBHR device is a stand-alone USB Type-C and power-delivery (PD) controller providing cable-plug and orientation detection at the USB Type-C connector. Upon cable detection, the SN1804044ZBHR device communicates on the CC wire using the USB PD protocol. When cable detection and USB PD negotiation are complete, the SN1804044ZBHR device enables the appropriate power path and configures alternate mode settings for internal and (optional) external multiplexers.

The mixed-signal front-end on the CC pins advertises default (500 mA), 1.5 A or 3 A for Type-C power sources, detects a plug event and determines the USB Type-C cable orientation, and autonomously negotiates USB PD contracts by adhering to the specified biphase marked coding (BMC) and physical layer (PHY) protocol.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN1804044ZBHR	NFBGA (96)	6.00 mm × 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Diagram

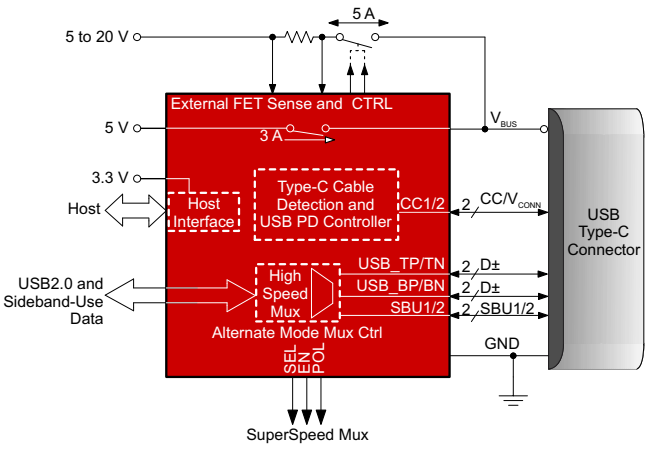


Table of Contents

4 Description (continued)

The port power switch provides up to 3-A downstream at 5 V for legacy and Type-C USB power. An additional external bidirectional switch path can be used to provide USB PD power up to 5 A at a maximum of 20 V as either a source (host), sink (device), or source-sink.

The SN1804044ZBHR device is also an upstream-facing port (UFP), downstream-facing port (DFP), or dual-role port for data. The port-data multiplexer passes data to or from the top or bottom D+/D– signal pair at the port for USB 2.0 HS and also integrates a USB 2.0 low-speed endpoint. Additionally, the sideband-use (SBU) signal pair is used for auxiliary or alternate modes of communication (DisplayPort or Thunderbolt, for example).

The power management circuitry uses a 3.3-V supply inside the system and can also use VBUS to start up and negotiate power for a dead-battery or no-battery condition.

5 Pin Configuration and Functions

Figure 1. Legend for Pinout Drawing

Pin Functions

PIN		TYPE	POR STATE	DESCRIPTION
NAME	NO.			
HIGH CURRENT POWER PINS				
PP_5V0	A11, B11, C11, D11	Power	—	5-V supply for VBUS. Bypass with capacitance CPP_5V0 to GND. Tie pin to GND when unused.
PP_CABLE	H10	Power	—	5-V supply for C_CC pins. Bypass with capacitance CPP_CABLE to GND when not tied to PP_5V0. Tie pin to PP_5V0 when unused.
VBUS	H11, J10, J11, K11	Power	—	5-V output from PP_5V0. Input or output from PP_EXT up to 20 V. Bypass with capacitance CVBUS to GND.
LOW CURRENT POWER PINS				
VIN_3V3	H1	Power	—	Supply for core circuitry and I/O. Bypass with capacitance CVIN_3V3 to GND.
VDDIO	B1	Power	—	VDD for I/O. Some I/Os are reconfigurable to be powered from VDDIO instead of LDO_3V3. When VDDIO is not used, tie pin to LDO_3V3. When not tied to LDO_3V3 and used as a supply input, bypass with capacitance CVDDIO to GND.
VOUT_3V3	H2	Power	—	Output of supply switched from VIN_3V3. Bypass with capacitance COUT_3V3 to GND. Float pin when unused.
LDO_3V3	G1	Power	—	Output of the VBUS to 3.3 V LDO or connected to VIN_3V3 by a switch. Main internal supply rail. Used to power optional external flash memory. Bypass with capacitance CLDO_3V3 to GND.
LDO_1V8A	K1	Power	—	Output of the 3.3-V or 1.8-V LDO for core analog circuits. Bypass with capacitance CLDO_1V8A to GND.
LDO_1V8D	A2	Power	—	Output of the 3.3-V or 1.8-V LDO for core digital circuits. Bypass with capacitance CLDO_1V8D to GND.
LDO_BMC	E1	Power	—	Output of the USB-PD BMC transceiver output level LDO. Bypass with capacitance CLDO_BMC to GND.
TYPE-C PORT PINS				
C_CC1	L9	Analog I/O	Hi-Z	Output to Type-C CC or VCONN pin. Filter noise with capacitance CC_CC1 to GND.
C_CC2	L10	Analog I/O	Hi-Z	Output to Type-C CC or VCONN pin. Filter noise with capacitance CC_CC2 to GND.
RPD_G1	K9	Analog I/O	Hi-Z	Tie pin to C_CC1 when configured to receive power in dead-battery or no-power condition. Tie pin to GND otherwise.
RPD_G2	K10	Analog I/O	Hi-Z	Tie pin to C_CC2 when configured to receive power in dead-battery or no-power condition. Tie pin to GND otherwise.
C_USB_TP	K6	Analog I/O	Hi-Z	Port-side top USB D+ connection to port multiplexer.
C_USB_TN	L6	Analog I/O	Hi-Z	Port-side top USB D– connection to port multiplexer.
C_USB_BP	K7	Analog I/O	Hi-Z	Port-side bottom USB D+ connection to port multiplexer.
C_USB_BN	L7	Analog I/O	Hi-Z	Port-side bottom USB D– connection to port multiplexer.
C_SBU1	K8	Analog I/O	Hi-Z	Port-side sideband. Use connection of port multiplexer.
C_SBU2	L8	Analog I/O	Hi-Z	Port-side sideband .Use connection of port multiplexer.
PORT MULTIPLEXER PINS				
SWD_DATA	F4	Digital I/O	Resistive pull high	SWD serial data. Float pin when unused.
SWD_CLK	G4	Digital input	Resistive pull high	SWD serial clock. Float pin when unused.
UART_RX	F2	Digital input	Digital input	UART serial receive data. Connect pin to another SN1804044ZBHR UART_TX to share firmware. Connect UART_RX to UART_TX when not connected to another SN1804044ZBHR and ground pin through a 100-kΩ resistance.
UART_TX	E2	Digital output	UART_RX	UART serial transmit data. Connect pin to another SN1804044ZBHR UART_TX to share firmware. Connect UART_RX to UART_TX when not connected to another SN1804044ZBHR.
USB_RP_P	L5	Analog I/O	Hi-Z	System-side USB2.0 high-speed connection to port multiplexer. Ground pin with between 1-kΩ and 5-MΩ resistance when unused.
USB_RP_N	K5	Analog I/O	Hi-Z	System-side USB2.0 high-speed connection to port multiplexer. Ground pin with between 1-kΩ and 5-MΩ resistance when unused.
LSX_R2P	L4	Digital input	Digital input	System-side low-speed TX from system to port. This pin is configurable to be an input to the digital core or the crossbar multiplexer to the port. Ground pin with between 1-kΩ and 5-MΩ resistance when unused.
LSX_P2R	K4	Digital output	Hi-Z	System side low speed RX to system from port. This pin is configurable to be an output from the digital core or the crossbar multiplexer from the port. Float pin when unused.
AUX_P	J1	Analog I/O	Hi-Z	System-side DisplayPort connection to port multiplexer. Ground pin with between 1-kΩ and 5-MΩ resistance when unused.

Pin Functions (continued)

PIN		TYPE	POR STATE	DESCRIPTION
NAME	NO.			
AUX_N	J2	Analog I/O	Hi-Z	System-side DisplayPort connection to port multiplexer. Ground pin with between 1-kΩ and 5-MΩ resistance when unused.
EXTERNAL HV FET CONTROL/SENSE PINS AND SOFT START				
SENSEP	B10	Analog input	Analog input	Positive sense for external high voltage power path current sense resistance. Short pin to VBUS when unused.
SENSEN	A10	Analog input	Analog input	Positive sense for external high voltage power path current sense resistance. Short pin to VBUS when unused.
HV_GATE1	B9	Analog output	Short to SENSEP	External NFET gate control for high voltage power path. Float pin when unused.
HV_GATE2	A9	Analog output	Short to VBUS	External NFET gate control for high voltage power path. Float pin when unused.
SS	H7	Analog output	Driven low	Soft Start. Tie pin to capacitance CSS to ground.
DIGITAL CORE I/O AND CONTROL PINS				
R_OSC	G2	Analog I/O	Hi-Z	External resistance setting for oscillator accuracy. Connect R_OSC to GND through resistance RR_OSC.
GPIO0 (HD3 AMSEL)	B2	Digital I/O	Hi-Z	General purpose digital I/O 0. Device configurable as alternate mode select signal to external super-speed multiplexer (tri-state capable with pullup and pulldown resistors). Ground pin with a 1-MΩ resistor when unused in the application.
PP_HVEXT_EN (GPIO1)	C2	Digital I/O	Hi-Z	Active high output indicating PP_HVEXT external switch enabled. During boot, this terminal will be driven based on the BUSPOWERZ connection. After boot, the terminal can be reconfigured as GPIO. General purpose digital I/O 1. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-MΩ resistor when unused in the application.
PP_HV_EN (GPIO2)	D10	Digital I/O	Hi-Z	Active high output indicating PP_HV external switch enabled. During boot, this terminal will be driven based on the BUSPOWERZ connection. After boot, the terminal can be reconfigured as GPIO. General purpose digital I/O 2. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-MΩ resistor when unused in the application.
GPIO3 (HD3 EN)	G11	Digital I/O	Hi-Z	General purpose digital I/O 3. Enable signal to external super-speed multiplexer. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-MΩ resistor when unused in the application.
GPIO4 (HPD TXRX)	C10	Digital I/O	Hi-Z	General purpose digital I/O 4. Configured as hot-plug detect (HPD) TX, HPD RX, or both when DisplayPort Mode supported. Ground pin with a 1-MΩ resistor when unused in the application.
GPIO5 (HPD RX)	E10	Digital I/O	Hi-Z	General purpose digital I/O 5. Can be configured as hot-plug detect(HPD) RX when DisplayPort Mode supported. Must be tied high or low through a 1-kΩ pullup or pulldown resistor when used as a configuration input. Ground pin with a 1-MΩ resistor when unused in the application.
GPIO6	G10	Digital I/O	Hi-Z	General purpose digital I/O 6. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-MΩ resistor when unused in the application.
GPIO7	D7	Digital I/O	Hi-Z	General purpose digital I/O 7. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-MΩ resistor when unused in the application.
CONFIG (GPIO8)	H6	Analog input	Hi-Z	General purpose digital I/O 8. At device boot, the voltage on this pin is sensed and is used to load one of eight factory preset configurations. After device boot, this pin can be reused as GPIO. Refer to the *Boot Flow* section for more details.
RESETZ (GPIO9)	F11	Digital I/O	Push-pull output (low)	General purpose digital I/O 9. Active low reset output when VOUT_3V3 is low (driven low on start-up). Float pin when unused.
BUSPOWERZ (GPIO10)	F10	Analog input	Input (Hi-Z)	General purpose digital I/O 10. Sampled by ADC at boot. Tie pin to LDO_3V3 through a 100-kΩ resistor to disable PP_EXT power path during dead-battery or no-battery boot conditions. Refer to the *BUSPOWERZ* table for more details.
MRESET (GPIO11)	E11	Digital I/O	Hi-Z	General purpose digital I/O 11. Forces RESETZ to assert. By default, this pin asserts RESETZ when pulled high. The pin can be programmed to assert RESETZ when pulled low. Ground pin with a 1-MΩ resistor when unused in the application.
DEBUG4 (GPIO12)	K3	Digital I/O	Hi-Z	General purpose digital I/O 12. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-MΩ resistor when unused in the application.
DEBUG3 (GPIO13)	L3	Digital I/O	Hi-Z	General purpose digital I/O 13. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-MΩ resistor when unused in the application.
DEBUG2 (GPIO14, HD3 POL)	K2	Digital I/O	Hi-Z	General purpose digital I/O 14. Polarity signal to external super-speed multiplexer. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-MΩ resistor when unused in the application.

Pin Functions (continued)

PIN		TYPE	POR STATE	DESCRIPTION
NAME	NO.			
DEBUG1 (GPIO15)	L2	Digital I/O	Hi-Z	General purpose digital I/O 15. Ground pin with a 1-MΩ resistor when unused in the application.
DEBUG_CTL1 (GPIO16, I^2C ADDR B4)	E4	Digital I/O	Hi-Z	General purpose digital I/O 16. At power-up, pin state is sensed to determine bit 4 of the I^2C address.
DEBUG_CTL2 (GPIO17, I^2C ADDR B5)	D5	Digital I/O	Hi-Z	General Purpose Digital I/O 17. At power-up, pin state is sensed to determine bit 5 of the I^2C address.
HRESET	D6	Digital Input	Hi-Z	Active high hardware reset input. Assertion causes a reboot sequence. Ground pin when HRESET functionality will not be used.
I2C_SDA1	D1	Digital I/O	Digital input	I^2C port 1 serial data. Open-drain output. Tie pin to LDO_3V3 or VDDIO (depending on configuration) through a 10-kΩ resistance when used or unused.
I2C_SCL1	D2	Digital I/O	Digital input	I^2C port 1 serial clock. Open-drain output. Tie pin to LDO_3V3 or VDDIO (depending on configuration) through a 10-kΩ resistance when used or unused.
I2C_IRQ1Z	C1	Digital output	Hi-Z	I^2C port 1 interrupt. Active low. Implement externally as an open drain with a pullup resistance. Float pin when unused.
I2C_SDA2	A5	Digital I/O	Digital input	I^2C port 2 serial data. Open-drain output. Tie pin to LDO_3V3 or VDDIO (depending on configuration) through a 10-kΩ resistance when used or unused.
I2C_SCL2	B5	Digital I/O	Digital input	I^2C port 2 serial clock. Open-drain output. Tie pin to LDO_3V3 or VDDIO (depending on configuration) through a 10-kΩ resistance when used or unused.
I2C_IRQ2Z	B6	Digital output	Hi-Z	I^2C port 2 interrupt. Active low. Implement externally as an open drain with a pullup resistance. Float pin when unused.
I2C_ADDR	F1	Analog I/O	Analog input	Sets the I^2C address for both I^2C ports as well as determine the primary and secondary slave devices for memory code sharing.
SPI_CLK	A3	Digital output	Digital input	SPI serial clock. Ground pin when unused
SPI_MOSI	B4	Digital output	Digital input	SPI serial master output to slave. Ground pin when unused.
SPI_MISO	A4	Digital input	Digital input	SPI serial master input from slave. This pin is used during boot sequence to determine if the optional flash memory is valid. Refer to the *Device Functional Modes* section for more details. Ground pin when unused.
SPI_SSZ	B3	Digital output	Digital input	SPI slave select. Ground pin when unused.
GROUND AND NO CONNECT PINS				
GND	A1, B8, D8, E5, E6, E7, E8, F5, F6, F7, F8, G5, G6, G7, G8, H4, H5, H8, L1	Ground	NA	Ground. Connect all balls to ground plane.
NC	L11	Blank	NA	Populated Ball that must remain unconnected.
No Ball	C3, C4, C5, C6, C7, C8, C9, D3, D4, D9, E3, E9, F3, F9, G3, G9, H3, H9, J3, J4, J5, J6, J7, J8, J9	Blank	NA	Unpopulated Ball for A1 marker and unpopulated inner ring.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_I Input voltage(2)	PP_CABLE, PP_5V0	–0.3	6	V
	VIN_3V3	–0.3	3.6	
	SENSEP, SENSEN(3)	–0.3	24	
	VDDIO, UART_RX	–0.3	LDO_3V3 + 0.3	
V_{IO} Output voltage(2)	LDO_1V8A, LDO_1V8D, LDO_BMC, SS	–0.3	2	V
	LDO_3V3	–0.3	3.45	
		–0.3	LDO_3V3 + 0.3	
	HV_GATE1, HV_GATE2	–0.3	30	
	HV_GATE1 (relative to SENSEP), HV_GATE2 (relative to VBUS)	–0.3	6	
V_{IO} I/O voltage(2)	VBUS	–0.3	24	V
	I2C_SDA1, I2C_SCL1, SWD_DATA, SPI_MISO, I2C_SDA2, I2C_SCL2, LSX_R2P, USB_RP_P, USB_RP_N, AUX_N, AUX_P, DEBUG1, DEBUG2, DEBUG3, DEBUG4, DEBUG_CTL1, DEBUG_CTL2, GPIOn, MRESET, BUSPOWERZ, GPIO0-8	–0.3	LDO_3V3 + 0.3	
		–0.3	2	
	HRESET	-0.3	LDO_1V8D + 0.3	
	C_USB_TP, C_USB_TN, C_USB_BP, C_USB_BN, C_SBU2, C_SBU1 (Switches Open)	–2	6	
	C_USB_TP, C_USB_TN, C_USB_BP, C_USB_BN, C_SBU2, C_SBU1 (Switches Closed)	–0.3	6	
	C_CC1, C_CC2, RPD_G1, RPD_G2	–0.3	6	
T_J Operating junction temperature		–10	125	°C
T_{stg} Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network GND. All GND pins must be connected directly to the GND plane of the board.
(3) The 24-V maximum is based on keeping HV_GATE1/2 at or below 30 V. Fast voltage transitions (<100 ns) can occur up to 30 V.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_I	Input voltage(1)	VIN_3V3	2.85	3.45	V
		PP_5V0	4.75	5.5	
		PP_CABLE	2.95	5.5	
		VDDIO	1.7	3.45	
V_{IO}	I/O voltage(1)	VBUS	4	22	V
		C_USB_PT, C_USB_NT, C_USB_PB, C_USB_NB, C_SBU1, C_SBU2	–2	5.5	
		C_CC1, C_CC2	0	5.5	
T_A	Ambient operating temperature		–10	85	°C
T_B	Operating board temperature		–10	100	°C
T_J	Operating junction temperature		–10	125	°C

(1) All voltage values are with respect to network GND. All GND pins must be connected directly to the GND plane of the board.

6.4 Power Supply Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXTERNAL						
VIN_3V3	Input 3.3-V supply		2.85	3.3	3.45	V
PP_CABLE	Input voltage to power C_CC pins		2.95	5	5.5	V
VBUS	Bi-direction DC bus voltage. Output from the SN1804044ZBHR or input to the SN1804044ZBHR		4	5	22	V
PP_5V0	5-V supply input to power VBUS. This supply does not power the SN1804044ZBHR		4.75	5	5.5	V
VDDIO(1)	Optional supply for I/O cells		1.7		3.45	V
INTERNAL						
VLDO_3V3	DC 3.3 V generated internally by either a switch from VIN_3V3, an LDO from PP_CABLE, or an LDO from VBUS		2.7	3.3	3.45	V
VDO_LDO3V3	Drop Out Voltage of LDO_3V3 from PP_CABLE	I_{LOAD} = 50 mA			250	mV
	Drop Out Voltage of LDO_3V3 from VBUS		250	500	750	mV
VLDO_1V8D	DC 1.8 V generated for internal digital circuitry		1.7	1.8	1.9	V
VLDO_1V8A	DC 1.8 V generated for internal analog circuitry		1.7	1.8	1.9	V
VLDO_BMC	DC voltage generated on LDO_BMC. Setting for USB-PD.		1.05	1.125	1.2	V
ILDO_3V3	DC current supplied by the 3.3-V LDOs. This includes internal core power and external load on LDO_3V3				50	mA
ILDO_3V3EX	External DC current supplied by LDO_3V3				10	mA
IOUT_3V3	External DC current supplied by VOUT_3V3				100	mA
ILDO_1V8D	DC current supplied by LDO_1V8D. This is intended for internal loads only but small external loads may be added				50	mA
ILDO_1V8DEX	External DC current supplied by LDO_1V8D				5	mA
ILDO_1V8A	DC current supplied by LDO_1V8A. This is intended for internal loads only but small external loads may be added				20	mA
ILDO_1V8AEX	External DC current supplied by LDO_1V8A				5	mA
ILDO_BMC	DC current supplied by LDO_BMC. This is intended for internal loads only				5	mA
ILDO_BMCEX	External DC current supplied by LDO_BMC				0	mA
VFWD_DROP	Forward voltage drop across VIN_3V3 to LDO_3V3 switch	I_{LOAD} = 50 mA	25	60	90	mV
RIN_3V3	Input switch resistance from VIN_3V3 to LDO_3V3	$V_{VIN\_3V3} - V_{LDO\_3V3}$ > 50 mV	0.5	1.1	1.75	Ω
ROUT_3V3	Output switch resistance from VIN_3V3 to VOUT_3V3			0.35	0.7	Ω
TR_OUT3V3	10-90% rise time on VOUT_3V3 from switch enable	C_{VOUT_3V3} = 1 µF	35		120	µs

(1) I/O buffers are not fail-safe to LDO_3V3. Therefore, VDDIO may power-up before LDO_3V3. When VDDIO powers up before LDO_3V3, the I/Os shall not be driven high. When VDDIO is low and LDO_3V3 is high, the I/Os may be driven high.

6.5 Power Supervisor Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UV_LDO3V3	Undervoltage threshold for LDO_3V3. Locks out 1.8-V LDOs	LDO_3V3 rising	2.2	2.325	2.45	V
UVH_LDO3V3	Undervoltage hysteresis for LDO_3V3	LDO_3V3 falling	20	80	150	mV
UV_VBUS_LDO	Undervoltage threshold for VBUS to enable LDO	VBUS rising	3.35	3.75	3.95	V
UVH_VBUS_LDO	Undervoltage hysteresis for VBUS to enable LDO	VBUS falling	20	80	150	mV
UV_PCBL	Undervoltage threshold for PP_CABLE	PP_CABLE rising	2.5	2.625	2.75	V
UVH_PCBL	Undervoltage hysteresis for PP_PCABLE	PP_CABLE falling	20	50	80	mV
UV_5V0	Undervoltage threshold for PP_5V0	PP_5V0 rising	3.5	3.725	3.95	V
UVH_5V0	Undervoltage hysteresis for PP_P5V0	PP_5V0 falling	20	80	150	mV
OV_VBUS	Overvoltage threshold for VBUS. This value is a 6-bit programmable threshold	VBUS rising	5		24	V
OVLSB_VBUS	Overvoltage threshold step for VBUS. This value is the LSB of the programmable threshold	VBUS rising		328		mV
OVH_VBUS	Overvoltage hysteresis for VBUS	VBUS falling, % of OV_VBUS	0.9%	1.3%	1.7%	
UV_VBUS	Undervoltage threshold for VBUS. This value is a 6-bit programmable threshold	VBUS falling	2.5		18.21	V
UVLSB_VBUS	Undervoltage threshold step for VBUS. This value is the LSB of the programmable threshold	VBUS falling		249		mV
UVH_VBUS	Undervoltage hysteresis for VBUS	VBUS rising, % of UV_VBUS	0.9%	1.3%	1.7%	
UVR_OUT3V3	Configurable undervoltage threshold for VOUT_3V3 rising. Deasserts RESETZ	Setting 0	2.019	2.125	2.231	V
		Setting 1	2.138	2.25	2.363	
		Setting 2	2.256	2.375	2.494	
		Setting 3	2.375	2.5	2.625	
		Setting 4	2.494	2.625	2.756	
		Setting 5	2.613	2.75	2.888	
		Setting 6	2.731	2.875	3.019	
		Setting 7	2.85	3	3.15	
UVRH_OUT3V3	Undervoltage hysteresis for VOUT_3V3 falling.	OUT_3V3 falling		30	50	mV
TUVRASSERT	Delay from falling VOUT_3V3 or MRESET assertion to RESETZ asserting low				75	µs
TUVRDELAY	Configurable delay from VOUT_3V3 to RESETZ deassertion.		0		161.3	ms

6.6 Power Consumption Characteristics

Recommended operating conditions; T_A = 25°C (Room temperature) unless otherwise noted(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
IVIN_3V3 in sleep(2)	VIN_3V3 = VDDIO = 3.45 V, VBUS = 0, PPCABLE = 0; 100-kHz oscillator running		71		µA
IVIN_3V3 idle(3)	VIN_3V3 = VDDIO = 3.45 V, VBUS=0, PPCABLE = 0; 100-kHz oscillator running, 48-MHz oscillator running		2.2		mA
IVIN_3V3 active(4)	VIN_3V3 = VDDIO = 3.45 V, VBUS = 0, PPCABLE = 0; 100-kHz Oscillator running, 48-MHz oscillator running		5.3		mA

(1) Application code can result in other power consumption measurements by adjusting enabled circuitry and clock rates. Application code also provisions the wake-up mechanisms (for example, I^2C activity and GPIO activity).
(2) Sleep is defined as Type-C cable detect activated as DFP or UFP, internal power management and supervisory functions active.
(3) Idle is defined as Type-C cable detect activated as DFP or UFP, internal power management and supervisory functions active, and the digital core is clocked at 4 MHz.
(4) Active is defined as Type-C cable detect activated as DFP or UFP, internal power management and supervisory functions active, all core functionality active, and the digital core is clocked at 12 MHz.

6.7 Cable Detection Characteristics

Recommended operating conditions; T_A = –10°C to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IH_CC_USB	Source current through each C_CC pin when in a disconnected state and configured as a DFP advertising Default USB current to a peripheral device		73.6	80	86.4	µA
IH_CC_1P5	Source current through each C_CC pin when in a disconnected state when configured as a DFP advertising 1.5 A to a UFP		169	180	191	µA
IH_CC_3P0	Source current through each C_CC pin when in a disconnected state and configured as a DFP advertising 3 A to a UFP	VIN_3V3 ≥ 3.135 V	303	330	356	µA
VD_CCH_USB	Voltage threshold for detecting a DFP attach when configured as a UFP and the DFP is advertising default USB current source capability		0.15	0.2	0.25	V
VD_CCH_1P5	Voltage threshold for detecting a DFP advertising 1.5-A source capability when configured as a UFP		0.61	0.66	0.7	V
VD_CCH_3P0	Voltage threshold for detecting a DFP advertising 3-A source capability when configured as a UFP		1.169	1.23	1.29	V
VH_CCD_USB	Voltage threshold for detecting a UFP attach when configured as a DFP and advertising default USB current source capability	IH_CC = IH_CC_USB	1.473	1.55	1.627	V
VH_CCD_1P5	Voltage threshold for detecting a UFP attach when configured as a DFP and advertising 1.5-A source capability	IH_CC = IH_CC_1P5	1.473	1.55	1.627	V
VH_CCD_3P0	Voltage threshold for detecting a UFP attach when configured as a DFP and advertising 3-A source capability	IH_CC = IH_CC_3P0 VIN_3V3 ≥ 3.135 V	2.423	2.55	2.67	V
VH_CCA_USB	Voltage threshold for detecting an active cable attach when configured as a DFP and advertising default USB current capability		0.15	0.2	0.25	V
VH_CCA_1P5	Voltage threshold for detecting active cables attach when configured as a DFP and advertising 1.5-A capability		0.35	0.4	0.45	V
VH_CCA_3P0	Voltage threshold for detecting active cables attach when configured as a DFP and advertising 3-A capability		0.76	0.8	0.84	V
RD_CC	Pulldown resistance through each C_CC pin when in a disconnect state and configured as a UFP. LDO_3V3 powered	V = 1 V, 1.5 V	4.85	5.1	5.35	kΩ
RD_CC_OPEN	Pulldown resistance through each C_CC pin when in a disconnect state and configured as a UFP. LDO_3V3 powered	V = 0 V to LDO_3V3	500			kΩ
RD_DB	Pulldown resistance through each C_CC pin when in a disconnect state and configured as a UFP when configured for dead battery (RPD_Gn tied to C_CCn). LDO_3V3 unpowered	V = 1.5 V, 2 V RPD_Gn tied to C_CCn	4.08	5.1	6.12	kΩ
RD_DB_OPEN	Pulldown resistance through each C_CC pin when in a disconnect state and configured as a UFP when not configured for dead battery (RPD_Gn tied to GND). LDO_3V3 unpowered	V = 1.5 V, 2 V RPD_Gn tied to GND	500			kΩ
VTH_DB	Threshold voltage of the pulldown FET in series with RD during dead battery	I_CC = 80 µA	0.5	0.9	1.2	V
R_RPD	Resistance between RPD_Gn and the gate of the pulldown FET		25	50	85	MΩ

6.8 USB-PD Baseband Signal Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMMON						
PD_BITRATE	PD data bit rate		270	300	330	Kbps
UI(1)	Unit interval (1/PD_BITRATE)		3.03	3.33	3.7	µs
CCBLPLUG(2)	Capacitance for a cable plug (each plug on a cable may have up to this value)				25	pF
ZCABLE	Cable characteristic impedance		32		65	Ω
CRECEIVER(3)	Receiver capacitance. Capacitance looking into C_CCn pin when in receiver mode		70		120	pF
TRANSMITTER						
ZDRIVER	TX output impedance. Source output impedance at the Nyquist frequency of USB2.0 low speed (750 kHz) while the source is driving the C_CCn line		33		75	Ω
TRISE	Rise time. Maximum set by TX mask	10% to 90% amplitude points, minimum is under an unloaded condition	300			ns
TFALL	Fall time. Maximum set by TX mask	90% to 10% amplitude points, minimum is under an unloaded condition	300			ns
RECEIVER						
VRXTR	Rx receive rising-input threshold		605	630	655	mV
VRXTF	Rx receive falling-input threshold		450	470	490	mV
NCOUNT(4)	Number of transitions for signal detection (number to count to detect non-idle bus)		3			
TTRANWIN(4)	Time window for detecting non-idle bus		12		20	µs
ZBMCRX	Receiver input impedance	Does not include pullup or pulldown resistance from cable detect. Transmitter is Hi-Z.	10			MΩ
TRXFILTER(5)	Rx bandwidth limiting filter. Time constant of a single pole filter to limit broadband noise ingression		100			ns

(1) UI denotes the time to transmit an unencoded data bit not the shortest high or low times on the wire after encoding with BMC. A single data bit cell has duration of 1 UI, but a data bit cell with value 1 will contain a centrally place 01 or 10 transition in addition to the transition at the start of the cell.
(2) The capacitance of the bulk cable is not included in the CCBLPLUG definition. It is modeled as a transmission line.
(3) CRECEIVER includes only the internal capacitance on a C_CCn pin when the pin is configured to be receiving BMC data. External capacitance is needed to meet the required minimum capacitance per the USB-PD Specifications. TI recommends adding capacitance to bring the total pin capacitance to 300 pF for improved TX behavior.
(4) BMC packet collision is avoided by the detection of signal transitions at the receiver. Detection is active when a minimum of NCOUNT transitions occur at the receiver within a time window of TTRANWIN. After waiting TTRANWIN without detecting NCOUNT transitions, the bus is declared idle.
(5) Broadband noise ingression is because of coupling in the cable interconnect.

6.9 USB-PD TX Driver Voltage Adjustment Parameter

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted(1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
VTXP0	TX transmit peak voltage, 0		1.615	1.7	1.785	V
VTXP1	TX transmit peak voltage, 1		1.52	1.6	1.68	V
VTXP2	TX transmit peak voltage, 2		1.425	1.5	1.575	V
VTXP3	TX transmit peak voltage, 3		1.33	1.4	1.47	V
VTXP4	TX transmit peak voltage, 4		1.235	1.3	1.365	V
VTXP5	TX transmit peak voltage, 5		1.188	1.25	1.312	V
VTXP6	TX transmit peak voltage, 6		1.14	1.2	1.26	V
VTXP7	TX transmit peak voltage, 7		1.116	1.175	1.233	V
VTXP8	TX transmit peak voltage, 8		1.092	1.15	1.208	V

(1) VTXP voltage settings are determined by application code and the setting used must meet the requirements of the application and adhere to the USB-PD Specifications.

USB-PD TX Driver Voltage Adjustment Parameter (continued)

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted[1]

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
VTXP9	TX transmit peak voltage, 9		1.068	1.125	1.181	V
VTXP10	TX transmit peak voltage, 10		1.045	1.1	1.155	V
VTXP11	TX transmit peak voltage, 11		1.021	1.075	1.128	V
VTXP12	TX transmit peak voltage, 12		0.998	1.05	1.102	V
VTXP13	TX transmit peak voltage, 13		0.974	1.025	1.076	V
VTXP14	TX transmit peak voltage, 14		0.95	1	1.05	V
VTXP15	TX transmit peak voltage, 15		0.903	0.95	0.997	V

6.10 Port-Power Switch Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS[1]	MIN	TYP	MAX	UNIT
RPPCC	PP_CABLE to C_CCn power switch resistance				312	mΩ
RPP5V	PP_5V0 to VBUS power switch resistance			50	60	mΩ
IHVEXTACT	Active quiescent current from SENSEP pin, switch closed	Configured as source			1	mA
	Active quiescent current from VBUS pin, switch closed	Configured as sink			3.5	
IHVEXTSD	Shutdown quiescent current from SENSEP pin, switch opened				40	µA
IPP5VACT	Active quiescent current from PP_5V0				1	mA
IPP5VSD	Shutdown quiescent current from PP_5V0				100	µA
ILIMHVEXT[2][3]	PP_EXT current limit, setting 0		0.986	1.12	1.254	A
	PP_EXT current limit, setting 1		1.231	1.399	1.567	
	PP_EXT current limit, setting 2		1.477	1.678	1.879	
	PP_EXT current limit, setting 3		1.761	1.957	2.153	
	PP_EXT current limit, setting 4		2.012	2.236	2.46	
	PP_EXT current limit, setting 5		2.263	2.515	2.767	
	PP_EXT current limit, setting 6		2.514	2.794	3.074	
	PP_EXT current limit, setting 7		2.765	3.073	3.381	
	PP_EXT current limit, setting 8		3.016	3.352	3.688	
	PP_EXT current limit, setting 9		3.267	3.631	3.995	
	PP_EXT current limit, setting 10		3.519	3.91	4.301	
	PP_EXT current limit, setting 11		3.77	4.189	4.608	
	PP_EXT current limit, setting 12		4.021	4.468	4.915	
	PP_EXT current limit, setting 13		4.272	4.747	5.222	
	PP_EXT current limit, setting 14		4.523	5.026	5.529	
	PP_EXT current limit, setting 15		5.025	5.584	6.143	

(1) Maximum capacitance on VBUS when configured as a source must not exceed 12 µF.
(2) Specified for a 10-mΩ RSENSE resistor and 10-mΩ RSENSE application code setting. Values scale with a different RSENSE resistance and application code setting.
(3) Settings selected automatically by application code for the current limit required in the application.

Port-Power Switch Characteristics (continued)

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS[1]	MIN	TYP	MAX	UNIT
ILIMPP5V[3]	PP_5V0 current limit, setting 0		1.006	1.118	1.330	A
	PP_5V0 current limit, setting 1		1.132	1.258	1.484	
	PP_5V0 current limit, setting 2		1.258	1.398	1.638	
	PP_5V0 current limit, setting 3		1.384	1.538	1.691	
	PP_5V0 current limit, setting 4		1.51	1.677	1.845	
	PP_5V0 current limit, setting 5		1.636	1.817	1.999	
	PP_5V0 current limit, setting 6		1.761	1.957	2.153	
	PP_5V0 current limit, setting 7		1.887	2.097	2.307	
	PP_5V0 current limit, setting 8		2.013	2.237	2.46	
	PP_5V0 current limit, setting 9		2.139	2.376	2.614	
	PP_5V0 current limit, setting 10		2.265	2.516	2.768	
	PP_5V0 current limit, setting 11		2.39	2.656	2.922	
	PP_5V0 current limit, setting 12		2.516	2.796	3.075	
	PP_5V0 current limit, setting 13		2.642	2.936	3.229	
	PP_5V0 current limit, setting 14		2.768	3.075	3.383	
	PP_5V0 current limit, setting 15		3.019	3.355	3.69	
ILIMPPCC	PP_CABLE current limit (highest setting)		0.6	0.75	0.9	A
	PP_CABLE current limit (lowest setting)		0.35	0.45	0.55	
IHVEXT_ACC	PP_EXT current sense accuracy (excluding RSENSE accuracy)	I = 100 mA , RSENSE = 10 mΩ, reverse current blocking disabled	3.5	5	6.5	A/V
		I = 200 mA, RSENSE = 10 mΩ	4	5	6	A/V
		I = 500 mA, RSENSE = 10 mΩ	4.4	5	5.6	A/V
		I ≥ 1 A, RSENSE = 10 mΩ	4.5	5	5.5	A/V
IPP5V_ACC[4]	PP_5V0 current sense accuracy	I = 100 mA, reverse current blocking disabled	1.95	3	4.05	A/V
		I = 200 mA	2.4	3	3.6	A/V
		I = 500 mA	2.64	3	3.36	A/V
		I ≥ 1 A	2.7	3	3.3	A/V
IPPCBL_ACC	PP_CABLE current sense accuracy	I = 100 mA	-	1	-	A/V
		I = 200 mA	-	1	-	A/V
		I = 500 mA	-	1	-	A/V
IGATEEXT[5]	External gate-drive current on HV_GATE1 and HV_GATE2		4	5	6	µA
VGSEXT	VGS voltage driving external FETs		4.5		7.5	V
TON_5V	PP_5V0 path turn on time from enable to VBUS = 95% of PP_5V0 voltage	Configured as a source or as a sink with soft start disabled. PP_5V0 = 5 V, CVBUS = 10 µF, ILOAD = 100 mA			2.5	ms
TON_CC	PP_CABLE path turn on time from enable to C_CCn = 95% of the PP_CABLE voltage	PP_CABLE = 5 V, C_CCn = 500 nF, ILOAD = 100 mA			2	ms
ISS	Soft-start charging current		5.5	7	8.5	µA
RSS_DIS	Soft-start discharge resistance		0.6	1	1.4	kΩ
VTHSS	Soft-start complete threshold		1.35	1.5	1.65	V
TSSDONE	Soft-start complete time	CSS = 220 nF	31.9	46.2	60.5	ms
VREVPEXT	Reverse-current blocking voltage threshold for PP_EXT external switches		2	6	10	mV
VREV5V0	Reverse-current blocking voltage threshold for PP_5V0 switches		2	6	10	mV

(4) The current sense in the ADC does not accurately read below the current VREV5V0/RPP5V or VREVHV/RPPHV because of the reverse blocking behavior. When reverse blocking is disabled, the values given for accuracy are valid.
(5) Limit the resistance from the HV_GATE1/2 pins to the external FET gate pins to < 1 Ω to provide adequate response time to short-circuit events.

Port-Power Switch Characteristics (continued)

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS[1]	MIN	TYP	MAX	UNIT
VHVDISPD	Voltage threshold above VIN at which the pulldown RHVDISPD on VBUS is disabled during a transition from PHV to 5V0		45	200	250	mV
VSAFE0V	Voltage that is a safe 0 V per USB-PD Specifications		0		0.8	V
TSAFE0V	Voltage transition time to VSAFE0V				650	ms
VSO_HVEXT	Voltage on PP_EXT above which the PP_EXT to PP_5V0 transition on VBUS will meet transition requirements		9.9			V
SRPOS	Maximum slew rate for positive voltage transitions				0.03	V/µs
SRNEG	Maximum slew rate for negative voltage transitions		–0.03			V/µs
TSTABLE	EN to stable time for both positive and negative voltage transitions				275	ms
VSRCVALID	Supply-output tolerance beyond VSRCNEW during time TSTABLE		–0.5		0.5	V
VSRCNEW	Supply-output tolerance		–5		5	%
RFRSTX	Fast Role Swap request pulldown resistance				5	Ω
TFRSTX	Fast Role Swap request transmit duration		60		120	µs
VFRSDETECT	Fast Role Swap request voltage detection threshold		490	520	550	mV
TFRSRX	Fast Role Swap request detection time		30		50	µs

6.11 Port-Data Multiplexer Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWD MULTIPLEXER PATH[1]						
SWD_RON_U	On resistance of SWD_DATA/CLK to C_USB_TP/TN/BP/BN	V_i = 3.3 V, I_O = 20 mA		35	55	Ω
		V_i = 1 V, I_O = 20 mA		30	46	
SWD_ROND_U	On-resistance difference between P and N paths of SWD_DATA/CLK to C_USB_ TP/TN/BP/BN	V_i = 1 V to 3.3 V, I_O = 20 mA	–2.5		2.5	Ω
SWD_RON_S	On resistance of SWD_DATA/CLK to C_SBU1/2	V_i = 3.3 V, I_O = 20 mA		26	42	Ω
		V_i = = 1 V, I_O = 20 mA		24	37	
SWD_ROND_S	On-resistance difference between P and N paths of SWD_DATA/CLK to C_SBU1/2	V_i = 1 V to 3.3 V, I_O = 20 mA	–1.5		1.5	Ω
SWD_TON	Switch-on time from enable of SWD path	Time from enable bit with charge pump off			150	µs
		Time from enable bit at charge-pump steady state			10	
SWD_TOFF	Switch-off time from disable of SWD path	Time from disable bit at charge-pump steady state			500	ns
SWD_BW	3-dB bandwidth of SWD path	C_L = 10 pF	200			MHz
DEBUG1/2 MULTIPLEXER PATH[1]						
DB1_RON_U	On resistance DEBUG1/2 to C_USB_TP/TN/BP/BN	V_i = 3.3 V, I_O = 20 mA		14	26	Ω
		V_i = 1 V, I_O = 20 mA		10	17	
DB1_ROND_U	On-resistance difference between P and N paths of DEBUG1/2 to C_USB_TP/TN/BP/BN	V_i = 1 V to 3.3 V, I_O = 20 mA	–2.5		2.5	Ω
DB1_RON_S	On resistance of DEBUG1/2 to C_SBU1/2	V_i = 3.3 V, I_O = 20 mA		9.5	17	Ω
		V_i = 1 V, I_O = 20 mA		6.5	12	
DB1_ROND_S	On-resistance difference between P and N paths of Debug path DEBUG1/2 to C_SBU1/2	V_i = 1 V to 3.3 V, I_O = 20 mA	–0.5		0.5	Ω

(1) All RON specified maximums are the maximum of either of the switches in a pair. All ROND specified maximums are the maximum difference between the two switches in a pair. ROND does not add to RON.

Port-Data Multiplexer Characteristics (continued)

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DB1_TON	Switch-on time from enable of DEBUG path	Time from enable bit with charge pump off			150	µs
		Time from enable bit at charge-pump steady state			10	
DB1_TOFF	Switch-off time from disable of DEBUG path	Time from disable bit at charge-pump steady state			500	ns
DB1_BW	3-dB bandwidth of DEBUG path	C_L = 10 pF	200			MHz
DEBUG3/4 MULTIPLEXER PATH(1)						
DB3_RON_U	On resistance of DEBUG3/4 to C_USB_TP/TN/BP/BN	V_i = 3.3 V, I_O = 20 mA		14	24	Ω
		V_i = 1 V, I_O = 20 mA		9	17	
DB3_ROND_U	On-resistance difference between P and N paths of DEBUG3/4 to C_USB_ TP/TN/BP/BN	V_i = 1 V to 3.3 V, I_O = 20 mA	–1.5		1.5	Ω
DB3_RON_S	On resistance of DEBUG3/4 to C_SBU1/2	V_i = 3.3 V, I_O = 20 mA		9.5	18	Ω
		V_i = 1 V, I_O = 20 mA		6.5	12	
DB3_ROND_S	On-resistance difference between P and N paths of DEBUG3/4 to C_SBU1/2	V_i = 1 V to 3.3 V, I_O = 20 mA	–0.15		0.15	Ω
DB3_TON	Switch-on time from enable of DEBUG3/4 path	Time from enable bit with charge pump off			150	µs
		Time from enable bit at charge-pump steady state			10	
DB3_TOFF	Switch-off time from disable of DEBUG3/4 path	Time from disable bit at charge-pump steady state			500	ns
DB3_BW	3-dB bandwidth of DEBUG3/4 path	C_L = 10 pF	200			MHz
LSX_R2P/P2R MULTIPLEXER PATH(1)						
LSX_RON	On resistance of LSX_P2R/R2P to C_SBU1/2	V_i = 3.3 V, I_O = 20 mA		8.5	17	Ω
		V_i = 1 V, I_O = 20 mA		5.5	11	
LSX_ROND	On-resistance difference between P and N paths of LSX path	V_i = 1 V to 3.3 V, I_O = 20 mA	–0.3		0.3	Ω
LSX_TON	Switch-on time from enable of LSX path	Time from enable bit with charge pump off			150	µs
		Time from enable bit at charge-pump steady state			10	
LSX_TOFF	Switch-off time from disable of LSX path	Time from disable bit at charge-pump steady state			500	ns
LSX_BW	3-dB bandwidth of LSX path	C_L = 10 pF	200			MHz
AUX MULTIPLEXER PATH(1)						
AUX_RON	On resistance of AUX_P/N to C_SBU1/2	V_i = 3.3 V, I_O = 20 mA		3.5	7	Ω
		V_i = 1 V, I_O = 20 mA		2.5	5	
AUX_ROND	On-resistance difference between P and N paths of AUX_P/N to C_SBU1/2	V_i = 1 V to 3.3 V, I_O = 20 mA	–0.25		0.25	Ω
AUX_TON	Switch-on time from enable of AUX_P/N to C_SBU1/2	Time from enable bit with charge pump off			150	µs
		Time from enable bit at charge-pump steady state			15	
AUX_TOFF	Switch-off time from disable of AUX_P/N to C_SBU1/2	Time from disable bit at charge-pump steady state			500	ns
AUX_BW	3-dB bandwidth of AUX_P/N to C_SBU1/2 path	C_L = 10 pF	200			MHz
UART MULTIPLEXER PATH (2nd Stage Only)(1)(2)						
UART_RON	On resistance of UART buffers to C_USB_TP/TN/BP/BN or C_SBU1/2	V_i = 3.3 V, I_O = 20 mA		3.1	12	Ω
UART_TON	Switch-on time from enable of UART buffer C_USB_TP/TN/BP/BN or C_SBU1/2 path	Time from enable bit with charge pump off			150	µs
		Time from enable bit at charge-pump steady state			10	

(2) The UART switch path connects from the UART buffers to the port pins. See the *Input/Output (I/O) Characteristics* table for buffer specifications.

Port-Data Multiplexer Characteristics (continued)

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UART_TOFF	Switch-off time from disable of UART buffer path	Time from disable bit at charge-pump steady state			500	ns
UART_BW	3-dB bandwidth of UART buffer path	C_L = 10 pF	200			MHz
USB_RP MULTIPLEXER PATH (1)(3)						
USB_RON	On resistance of USB_RP to C_USB_TP/TN/BP/BN	V_I = 3 V, I_O = 20 mA		4.5	10	Ω
		V_I = 400 mV, I_O = 20 mA		3	7	
USB_ROND	On-resistance difference between P and N paths of USB_RP to C_USB_TP/TN/BP/BN	V_I = 0.4 V to 3 V, I_O = 20 mA	–0.15		0.15	Ω
USB_TON	Switch-on time from enable of USB USB_RP path	Time from enable bit with charge pump off			150	µs
		Time from enable bit at charge-pump steady state			15	
USB_TOFF	Switch-off time from disable of USB_RP path	Time from disable bit at charge-pump steady state			500	ns
USB_BW	3-dB bandwidth of USB_RP path	C_L = 10 pF	850			MHz
USB_ISO	Off isolation of USB_RP path	R_L = 50 Ω, V_I = 800 mV, f = 240 MHz			–19	dB
USB_XTLK	Channel-to-channel crosstalk of USB_RP path	R_L = 50 Ω, f = 240 MHz			–26	dB
C_SBU1/2 OUTPUT						
R_SBU_OPEN	Resistance of the open C_SBU1/2 paths	V_I = 0 V to LDO_3V3	1			MΩ
R_USB_OPEN	Resistance of the open C_USB_T/B/P/N paths	V_I = 0 V to LDO_3V3	1			MΩ

(3) See the *Port-Data Multiplexer USB Endpoint Characteristics* table for the USB_EP specifications.

6.12 Port-Data Multiplexer Clamp Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCLMP_IND	Clamp voltage triggering indicator to the digital core		3.8	3.95	4.1	V
ICLMP_IND	Clamp current at VCLMP_IND		10		250	µA
TCLMP_PRT(1)	Time from clamp-current crossing ICLMP_IND to interrupt signal assertion	I ≥ ICLMP_IND rising	0		4	µs
ICLMP	USB_EP and USB_RP port-clamp current	V = LDO_3V3			250	nA
		V = VCLMP_IND + 500 mV	3.5		15	mA

(1) The TCLMP_PRT time includes the time through the digital synchronizers. When the clock speed is reduced, the signal assertion time can be longer.

6.13 Port-Data Multiplexer SBU Detection Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIH_PORT	Port switch detect input high voltage	LDO_3V3 = 3.3 V	2			V
VIL_PORT	Port switch detect input low voltage	LDO_3V3 = 3.3 V			0.8	V

6.14 Port-Data Multiplexer Signal Monitoring Pullup and Pulldown Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RPU05	500-Ω pullup and pulldown resistance	LDO_3V3 = 3.3 V	350	500	650	Ω
RTPU5	5-kΩ pullup and pulldown resistance	LDO_3V3 = 3.3 V	3.5	5	6.5	kΩ
RPU100	100-kΩ pullup and pulldown resistance	LDO_3V3 = 3.3 V	70	100	130	kΩ

6.15 Port-Data Multiplexer USB Endpoint Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TRANSMITTER(1)						
T_RISE_EP	Rising transition time	Low-speed (1.5 Mbps) data rate only	75		300	ns
T_FALL_EP	Falling transition time	Low-speed (1.5 Mbps) data rate only	75		300	ns
T_RRM_EP	Rise and fall time matching	Low-speed (1.5 Mbps) data rate only	–20%		25%	
V_XOVER_EP	Output crossover voltage		1.3		2	V
RS_EP	Source resistance of driver including 2nd-stage port-data multiplexer			34		Ω
DIFFERENTIAL RECEIVER(1)						
VOS_DIFF_EP	Input offset		–100		100	mV
VIN_CM_EP	Common-mode range		0.8		2.5	V
RPU_EP	D– bias resistance	Receiving	1.425		1.575	kΩ
SINGLE ENDED RECEIVER(1)						
VTH_SE_EP	Single ended threshold	Signal rising or falling	0.8		2	V
VHYS_SE_EP	Single ended threshold hysteresis	Signal falling		200		mV

(1) The USB endpoint PHY is functional across the entire VIN_3V3 operating range, but parameter values are only verified by design for VIN_3V3 ≥ 3.135 V

6.16 Port-Data Multiplexer BC1.2 Detection Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DATA CONTACT DETECT						
IDP_SRC	DCD source current	LDO_3V3 = 3.3 V	7	10	13	µA
RDM_DWN	DCD pulldown resistance		14.25	20	24.8	kΩ
VLGC_HI	Threshold for no connection	VC_USB_TP/BP ≥ VLGC_HILDO_3V3 = 3.3 V LDO_3V3 = 3.3 V	2			V
VLGC_LO	Threshold for connection	VC_USB_TP/BP ≤ VLGC_LO LDO_3V3 = 3.3 V			0.8	V
PRIMARY AND SECONDARY DETECT						
VDX_SRC	Source voltage		0.55	0.6	0.65	V
VDX_RSRC	Total series resistance because of the port-data multiplexer	VDX_SRC = 0.65 V			65	Ω
VDX_ILIM	VDX_SRC current limit		250		400	µA
IDX_SNK	Sink current	VC_USB_TN/BN ≥ 250 mV	25	75	125	µA

6.17 Analog-to-Digital Converter (ADC) Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RES_ADC	ADC Resolution			10		bits
F_ADC	ADC clock frequency		1.477	1.5	1.523	MHz
T_ENA	ADC enable time		42.14	43	43.86	µs
T_SAMPLEA	ADC input sample time		10.5	10.67	10.9	µs
T_CONVERTA	ADC conversion time		7.88	8	8.12	µs
T_INTA	ADC interrupt time		1.31	1.33	1.35	µs
LSB	Least significant bit		1.152	1.17	1.188	mV
DNL	Differential non-linearity		–0.65		0.65	LSB
INL	Integral non-linearity		–1.2		1.2	LSB
GAIN_ERR	Gain error (divider)		–1.5%		1.5%	
	Gain error (no divider)		–1		1	

Analog-to-Digital Converter (ADC) Characteristics (continued)

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOS_ERR	Buffer offset error		–10		10	mV
THERM_ACC	Thermal sense accuracy		–8		8	°C
THERM_GAIN	Thermal slope			3.095		mV/°C
THERM_V0	Zero degree voltage			0.823		V

6.18 Input/Output (I/O) Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPI						
SPI_VIH	High-level input voltage	LDO_3V3 = 3.3 V	2			V
SPI_VIL	Low-level input voltage	LDO_3V3 = 3.3 V			0.8	V
SPI_HYS	Input hysteresis voltage	LDO_3V3 = 3.3 V	0.2			V
SPI_ILKG	Leakage current	Output is Hi-Z, V_{IN} = 0 to LDO_3V3	–1		1	µA
SPI_VOH	SPI output high voltage	I_O = –8 mA, LDO_3V3=3.3 V	2.9			V
		I_O = –15 mA, LDO_3V3=3.3 V	2.5			
SPI_VOL	SPI output low voltage	I_O = 10 mA			0.4	V
		I_O = 20 mA			0.8	

Input/Output (I/O) Characteristics (continued)

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWDIO						
SWDIO_VIH	High-level input voltage	LDO_3V3 = 3.3 V	2			V
SWDIO_VIL	Low-level input voltage	LDO_3V3 = 3.3 V			0.8	V
SWDIO_HYS	Input hysteresis voltage	LDO_3V3 = 3.3 V	0.2			V
SWDIO_ILKG	Leakage current	Output is Hi-Z, V_{IN} = 0 to LDO_3V3	–1		1	µA
SWDIO_VOH	Output high voltage	I_O = –8 mA, LDO_3V3 = 3.3 V	2.9			V
		I_O = –15 mA, LDO_3V3 = 3.3 V	2.5			
SWDIO_VOL	Output low voltage	I_O = 10 mA			0.4	V
		I_O = 20 mA			0.8	
SWDIO_RPU	Pullup resistance		2.8	4	5.2	kΩ
SWDIO_TOS	SWDIO output skew to falling edge SWDCLK		–5		5	ns
SWDIO_TIS	Input setup time required between SWDIO and rising edge of SWCLK		6			ns
SWDIO_TIH	Input hold time required between SWDIO and rising edge of SWCLK		1			ns
SWDCLK						
SWDCL_VIH	High-level input voltage	LDO_3V3 = 3.3 V	2			V
SWDCL_VIL	Low-level input voltage	LDO_3V3 = 3.3 V			0.8	V
SWDCL_THI	SWDIOCLK HIGH period		0.05		500	µs
SWDCL_TLO	SWDIOCLK LOW period		0.05		500	µs
SWDCL_HYS	Input hysteresis voltage	LDO_3V3 = 3.3 V	0.2			V
SWDCL_RPU	Pullup resistance		2.8	4	5.2	kΩ
GPIO, MRESET, RESETZ, BUSPOWERZ						
GPIO_VIH	High-level input voltage	LDO_3V3 = 3.3 V	2			V
		VDDDIO = 1.8 V	1.25			
GPIO_VIL	Low-level input voltage	LDO_3V3 = 3.3 V			0.8	V
		VDDIO = 1.8 V			0.63	
GPIO_HYS	Input hysteresis voltage	LDO_3V3 = 3.3 V	0.2			V
		VDDIO = 1.8 V	0.09			
GPIO_ILKG	I/O leakage current	INPUT = 0 V to VDD	–1		1	µA
GPIO_RPU	Pullup resistance	Pullup enabled	50	100	150	kΩ
GPIO_RPU_DEBUG_CTL	Pullup resistance DEBUG_CTL1, DEBUG_CTL2	Pullup enabled	2.5	5	7.5	kΩ
GPIO_RPD	Pulldown resistance	Pulldown enabled	50	100	150	kΩ
GPIO_DG	Digital input path deglitch			20		ns
GPIO_VOH	GPIO output high voltage	IO = –2 mA, LDO_3V3 = 3.3 V	2.9			V
		IO = –2 mA, VDDIO = 1.8 V	1.35			
GPIO_VOL	GPIO output low voltage	IO = 2 mA, LDO_3V3 = 3.3 V			0.4	V
		IO = 2 mA, VDDIO = 1.8 V			0.45	
HRESET						
HRESET_VIH	High-level input voltage		1.25			V
HRESET_VIL	Low-level input voltage				0.63	V
HRESET_HYS	Input hysteresis Voltage		0.09			V
HRESET_ILKG	I/O leakage current	INPUT = 0 V to LDO_1V8D	–1		1	µA
HRESET_THIGH	HRESET minimum high time to assert a reset condition.		0.6			ms
HRESET_TLOW	HRESET minimum low time to deassert a reset condition.		0.6			
UART_RX/TX, LSX_P2R/R2P						
UARTRX_VIH	High-level input voltage	LDO_3V3 = 3.3 V	2			V
		VDDDIO = 1.8 V	1.25			
UARTRX_VIL	Low-level input voltage	LDO_3V3 = 3.3 V			0.8	V
		VDDIO = 1.8 V			0.63	

Input/Output (I/O) Characteristics (continued)

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UARTRX_HYS	Input hysteresis voltage	LDO_3V3 = 3.3 V	0.2			V
		VDDIO = 1.8 V	0.09			
UARTTX_VOH	GPIO output high voltage	I_O = –2 mA, LDO_3V3 = 3.3 V	2.9			V
		I_O = –2 mA, VDDIO = 1.8 V	1.35			
UARTTX_VOL	GPIO output low voltage	I_O = 2 mA, LDO_3V3 = 3.3 V			0.4	V
		I_O = 2 mA, VDDIO = 1.8 V			0.45	
UARTTX_RO	Output impedance, TX channel	LDO_3V3 = 3.3 V	35	70	115	Ω
UARTTX_TRTF	Rise and fall time, TX channel	10%–90%, C_L = 20 pF	1		40	ns
UART_FMAX	Maximum UART baud rate				1.1	Mbps
I2C_IRQ1Z, I2C_IRQ2Z						
OD_VOL	Low-level output voltage	IOL = 2 mA			0.4	V
OD_LKG	Leakage current	Output is Hi-Z, V_{IN} = 0 to LDO_3V3	–1		1	µA
SBU						
SBU_VIH	High-level input voltage	LDO_3V3 = 3.3 V	2			V
SBU_VIL	Low-level input voltage	LDO_3V3 = 3.3 V			0.8	V
SBU_HYS	Input hysteresis voltage	LDO_3V3 = 3.3 V	0.2			V

6.19 I²C Slave Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SDA and SCL COMMON CHARACTERISTICS						
ILEAK	Input leakage current	Voltage on pin = LDO_3V3	-3		3	µA
VOL	SDA output low voltage	IOL = 3 mA, LDO_3V3 = 3.3 V			0.4	V
		IOL = 3 mA, VDDIO = 1.8 V			0.36	
IOL	SDA maximum output-low current	VOL = 0.4 V	3			mA
		VOL = 0.6 V	6			
VIL	Input low signal	LDO_3V3 = 3.3 V			0.99	V
		VDDIO = 1.8 V			0.54	
VIH	Input high signal	LDO_3V3 = 3.3 V	2.31			V
		VDDIO = 1.8 V	1.26			
VHYS	Input hysteresis	LDO_3V3 = 3.3 V	0.17			V
		VDDIO = 1.8 V	0.09			
TSP	I²C pulse width suppressed				50	ns
CI	Pin Capacitance				10	pF
SDA and SCL STANDARD MODE CHARACTERISTICS						
FSCL	I²C clock frequency		0		100	kHz
THIGH	I²C clock high time		4			µs
TLOW	I²C clock low time		4.7			µs
TSUDAT	I²C serial data-setup time		250			ns
THDDAT	I²C serial data-hold time		0			ns
TVDDAT	I²C valid data time	SCL low to SDA output valid			3.4	µs
TVDACK	I²C valid data time of ACK condition	ACK signal from SCL low to SDA (out) low			3.4	µs
TOCF	I²C output fall time	10 pF to 400 pF bus			250	ns
TBUF	I²C bus free time between stop and start		4.7			µs
TSTS	I²C start or repeated start condition setup time		4.7			µs
TSTH	I²C start or repeated start condition hold time		4			µs
TSPS	I²C stop-condition setup time		4			µs
SDA and SCL FAST MODE CHARACTERISTICS						

I²C Slave Characteristics (continued)

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FSCL	I²C clock frequency		0		400	kHz
THIGH	I²C clock high time		0.6			µs
TLOW	I²C clock low time		1.3			µs
TSUDAT	I²C serial data-setup time		100			ns
THDDAT	I²C serial data-hold time		0			ns
TVDDAT	I²C valid data time	SCL low to SDA output valid			0.9	µs
TVDACK	I²C valid data time of ACK condition	ACK signal from SCL low to SDA (out) low			0.9	µs
TOCF	I²C output fall time	10 pF to 400 pF bus, VDD = 3.3 V	12		250	ns
		10 pF to 400 pF bus, VDD = 1.8 V	6.5		250	
TBUF	I²C bus free time between stop and start		1.3			µs
TSTS	I²C start or repeated start condition setup time		0.6			µs
TSTH	I²C start or repeated start condition hold time		0.6			µs
TSPS	I²C stop-condition setup time		0.6			µs

6.20 BUSPOWERZ Configuration Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VBPZ_EXT	BUSPOWERZ voltage for receiving VBUS power through the PP_EXT path				0.8	V
VBPZ_HV_EN	BUSPOWERZ voltage for PP_HV_EN GPIO event indicating a system request to receive VBUS power through an additional optional external power path		0.8		2.4	V
VBPZ_DIS	BUSPOWERZ voltage for disabling system power from VBUS		2.4			V

6.21 Thermal Shutdown Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TSD_MAIN	Thermal shutdown temperature of the main thermal shutdown	Temperature rising	145	160	175	°C
TSDH_MAIN	Thermal shutdown hysteresis of the main thermal shutdown	Temperature falling		20		°C
TSD_PWR	Thermal shutdown temperature of the power-path block	Temperature rising	135	150	165	°C
TSDH_PWR	Thermal shutdown hysteresis of the power-path block	Temperature falling		37		°C
TSD_DG	Programmable thermal shutdown detection deglitch time				0.1	ms

6.22 Oscillator Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FOSC_48M	48-MHz oscillator		47.28	48	48.72	MHz
FOSC_100K	100-kHz oscillator		95	100	105	kHz
RR_OSC	External oscillator set resistance (0.2%)		14.985	15	15.015	kΩ

6.23 Single-Wire Debugger (SWD) Timing Requirements

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FSWD	Frequency of SWD_CLK				10	MHz
TPER	Period of SWD_CLK (1/FSWD)		100			ns

Single-Wire Debugger (SWD) Timing Requirements (continued)

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TWHI	SWD_CLK high width		35			ns
TWLO	SWD_CLK low width		35			ns
TDOUT	SWD_CLK rising to SWD_DATA valid delay time		2		25	ns
TSUIN	SWD_DATA valid to SWD_CLK rising setup time		9			ns
THDIN	SWD_DATA hold time from SWD_CLK rising		3			ns
TRSWD	SWD output rise time	10% to 90%, C_L = 5 pF to 50 pF, LDO_3V3 = 3.3 V	0.1		8	ns
TFSWD	SWD output fall time	90% to 10%, C_L = 5 pF to 50 pF, LDO_3V3 = 3.3 V	0.1		8	ns

6.24 HPD Timing Requirements

Recommended operating conditions; T_A = –10°C to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DP SOURCE SIDE (HPD TX)						
T_IRQ_MIN	HPD IRQ minimum assert time		675	750	825	µs
T_3MS_MIN	HPD assert 3-ms minimum time		3	3.33	3.67	ms
DP SINK SIDE (HPD RX)						
T_HPD_HDB	HPD high debounce time	HPD_HDB_SEL = 0	300	375	450	µs
		HPD_HDB_SEL = 1	100	111	122	ms
T_HPD_LDB	HPD low debounce time		300	375	450	µs
T_HPD_IRQ	HPD IRQ limit time		1.35	1.5	1.65	ms

6.25 SPI Master Switching Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FSPI	Frequency of SPI_CLK		11.82	12	12.18	MHz
TPER	Period of SPI_CLK (1/F_SPI)		82.1	83.33	84.6	ns
TWHI	SPI_CLK high width		30			ns
TWLO	SPI_CLK low width		30			ns
TDACT	SPI_SZZ falling to SPI_CLK rising delay time		30		50	ns
TDINACT	SPI_CLK falling to SPI_SSZ rising delay time		160		180	ns
TDMOSI	SPI_CLK falling to SPI_MOSI Valid delay time		–5		5	ns
TSUMISO	SPI_MISO valid to SPI_CLK falling setup time		21			ns
THDMSIO	SPI_CLK falling to SPI_MISO invalid hold time		0			ns
TRSPI	SPI_SSZ/CLK/MOSI rise time	10% to 90%, C_L = 5 pF to 50 pF, LDO_3V3 = 3.3 V	0.1		8	ns
TFSPI	SPI_SSZ/CLK/MOSI fall time	90% to 10%, C_L = 5 pF to 50 pF, LDO_3V3 = 3.3 V	0.1		8	ns

6.26 Typical Characteristics

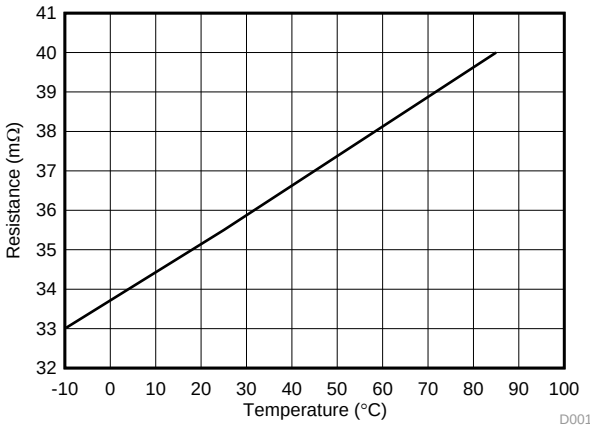


Figure 2. PP_5V0 Switch On-Resistance vs Temperature

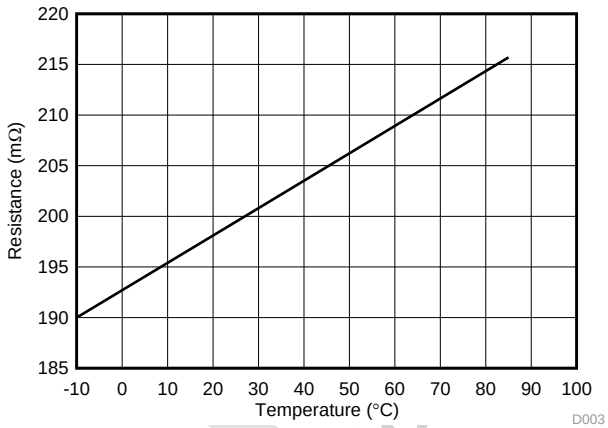


Figure 3. PP_CABLE Switch On-Resistance vs Temperature

7 Parameter Measurement Information

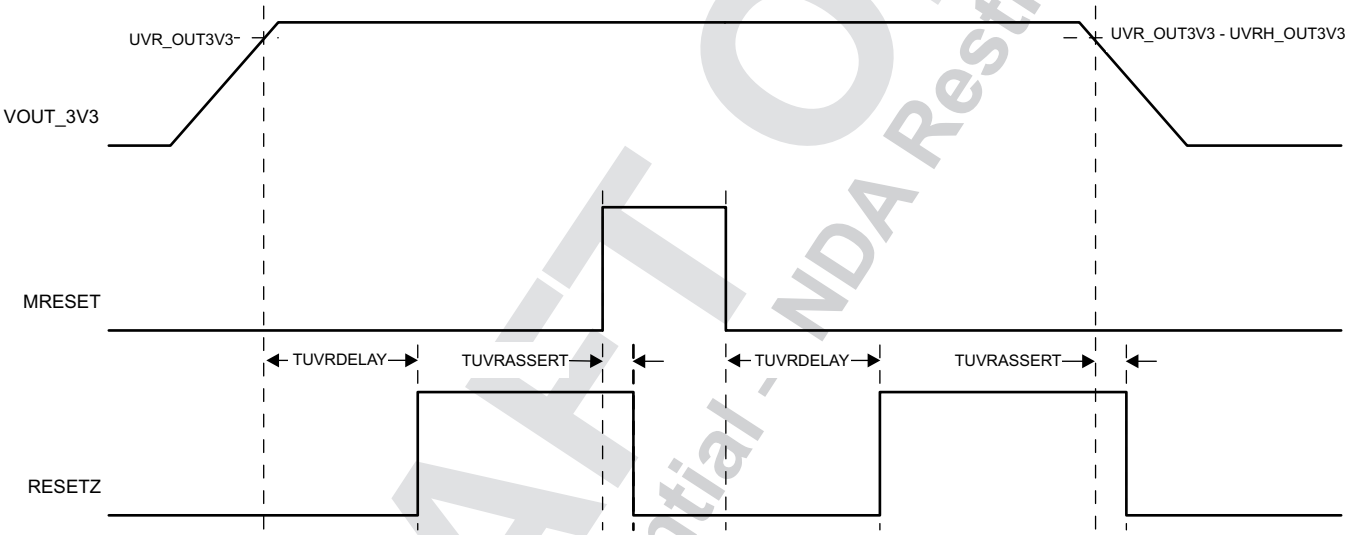


Figure 4. RESETZ Assertion Timing

Parameter Measurement Information (continued)

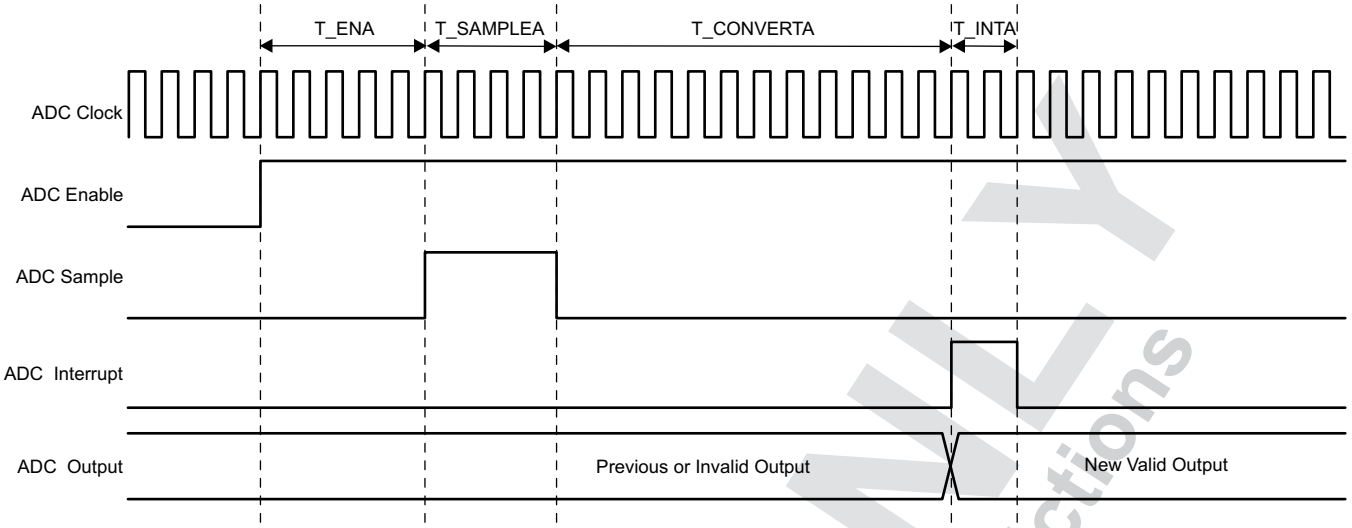


Figure 5. ADC Enable and Conversion Timing

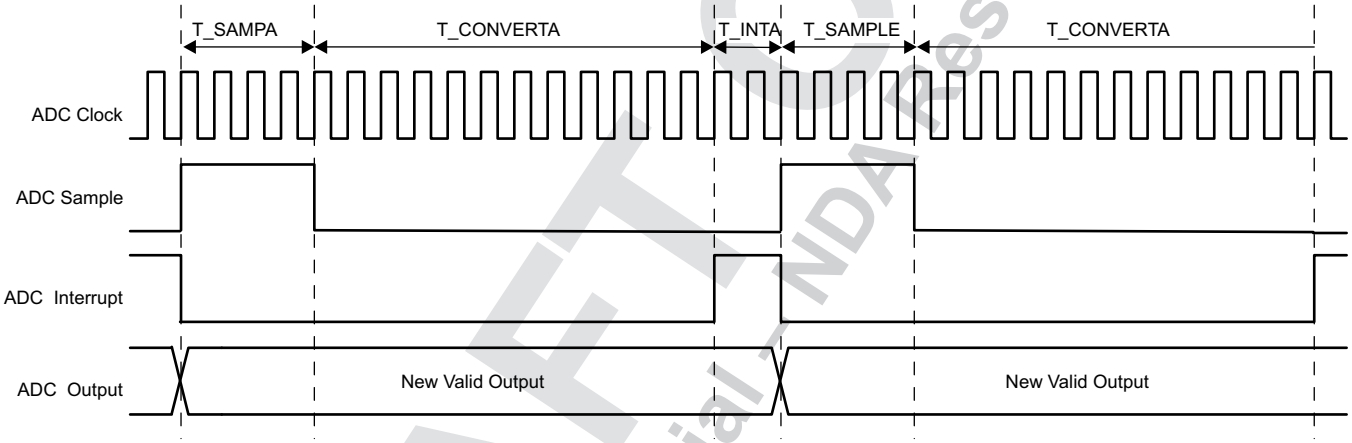


Figure 6. ADC Repeated Conversion Timing

Parameter Measurement Information (continued)

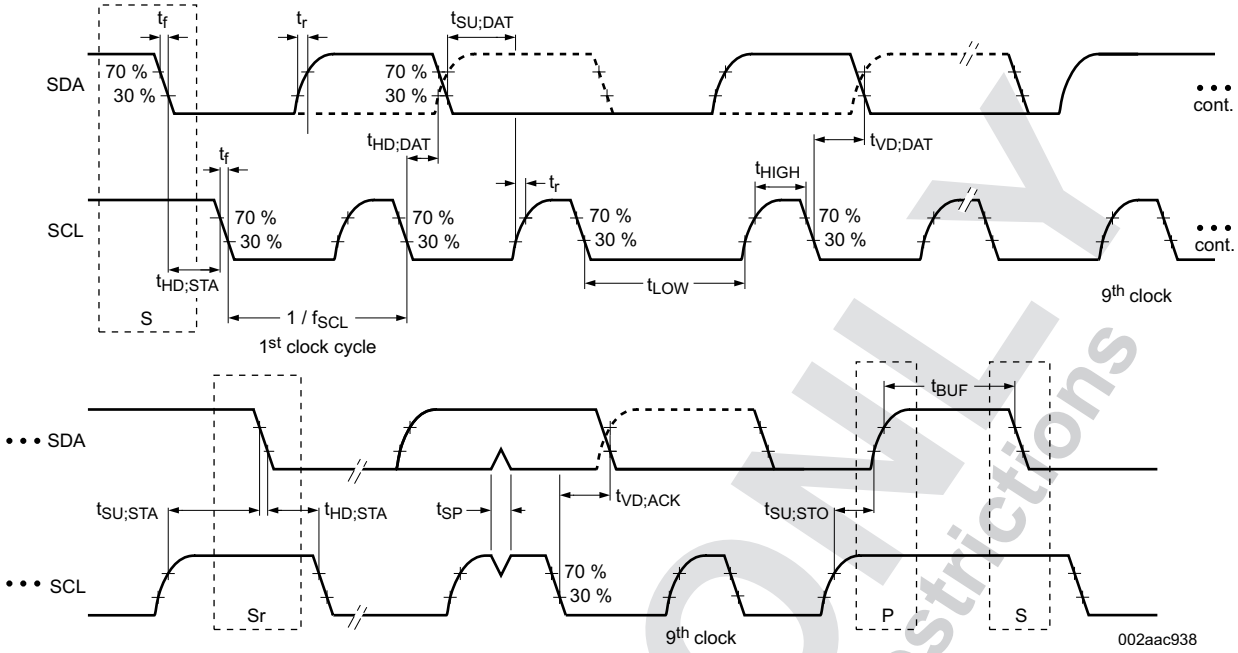


Figure 7. I²C Slave Interface Timing

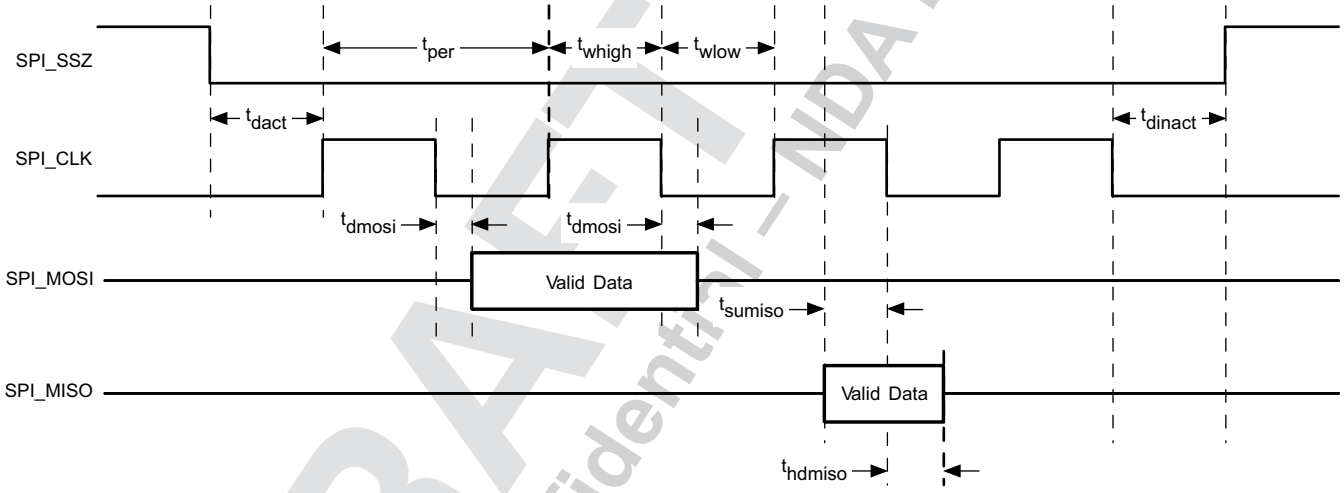


Figure 8. SPI Master Timing

Parameter Measurement Information (continued)

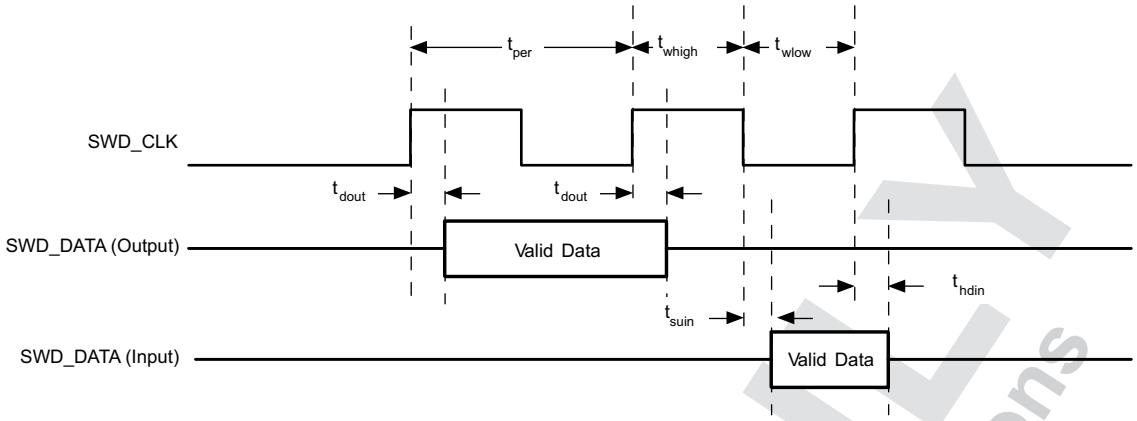


Figure 9. SWD Timing

8 Detailed Description

8.1 Overview

The SN1804044ZBHR device is a fully-integrated USB power-delivery (USB-PD) management device providing cable-plug and orientation detection for a USB Type-C and PD plug or receptacle. The SN1804044ZBHR device communicates with the cable and another USB Type-C and PD device at the opposite end of the cable, enables integrated port-power switches, controls an external high-current port-power switch, and multiplexes high-speed data to the port for USB2.0 and supported Alternate Mode sideband information. The SN1804044ZBHR device also controls an attached super-speed multiplexer to simultaneously support USB3.0/3.1 data rates and DisplayPort video.

The SN1804044ZBHR device is divided into six main sections: the USB-PD controller, the cable-plug and orientation detection circuitry, the port-power switches, the port-data multiplexer, the power-management circuitry, and the digital core.

The USB-PD controller provides the physical layer (PHY) functionality of the USB-PD protocol. The USB-PD data is output through either the C_CC1 pin or the C_CC2 pin, depending on the orientation of the reversible USB Type-C cable. See the *USB-PD Physical Layer* section for a high-level block diagram of the USB-PD physical layer, a description of the features, and more detailed circuitry.

The cable-plug and orientation detection analog circuitry automatically detects a USB Type-C cable plug insertion and also automatically detects the cable orientation. See the *Cable-Plug and Orientation Detection* section for a high-level block diagram of cable-plug and orientation detection, a description of the features, and more detailed circuitry.

The port+power switches provide power to the system port through the VBUS pin and also through the C_CC1 or C_CC2 pins based on the detected plug orientation. See the *Port-Power Switches* section for a high-level block diagram of the port power switches, a description of the features, and more detailed circuitry.

The port-data multiplexer connects various input pairs to the system port through the C_USB_TP, C_USB_TN, C_USB_BP, C_USB_BN, C_SBU1 and C_SBU2 pins. For a high-level block diagram of the port-data multiplexer, a description of the features, and more detailed circuitry, refer to the *USB Type-C Port-Data Multiplexer* section.

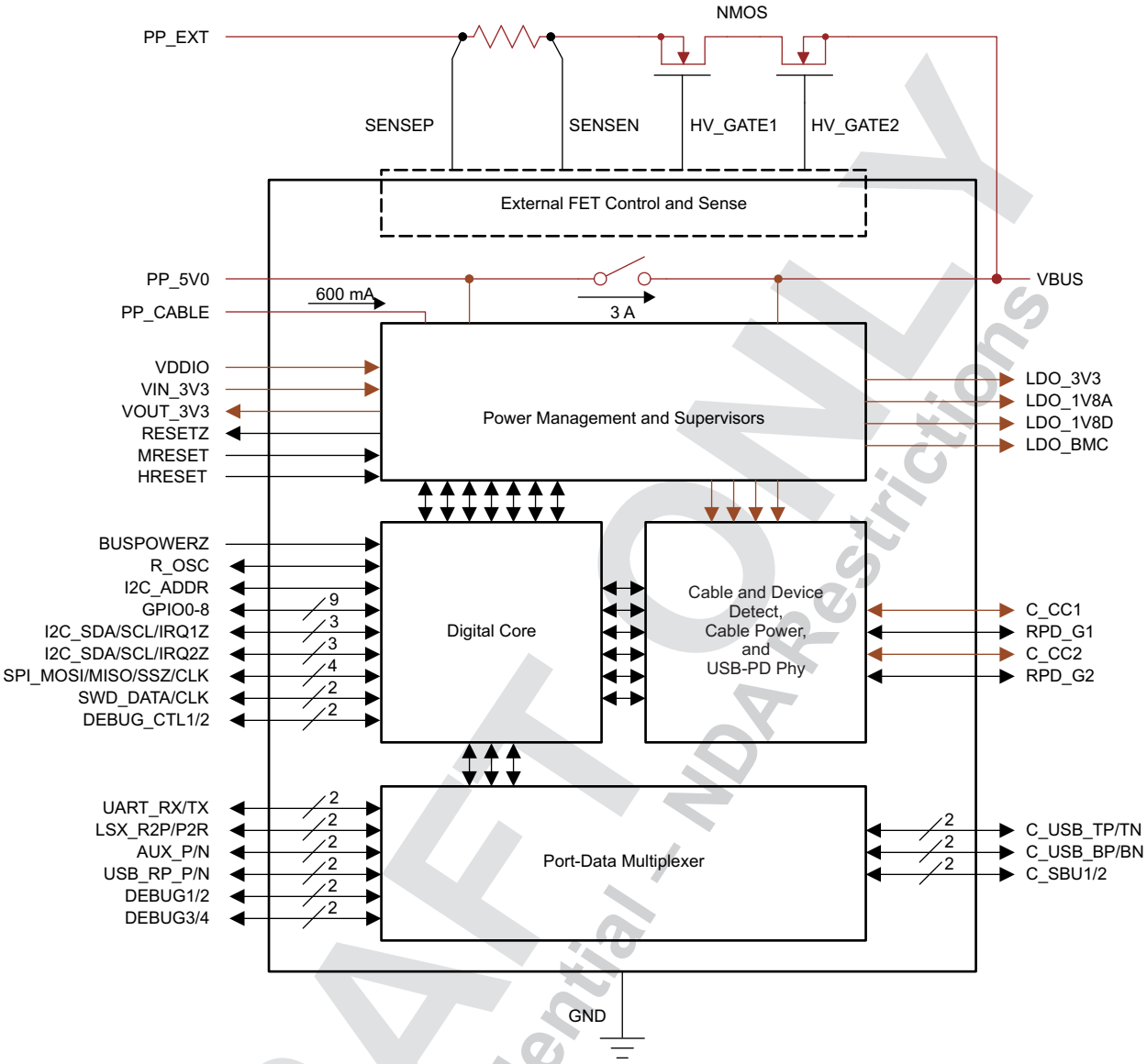
The power-management circuitry receives and provides power to the SN1804044ZBHR internal circuitry and to the VOUT_3V3 and LDO_3V3 outputs. See the *Power Management* section for a high-level block diagram of the power management circuitry, a description of the features, and more detailed circuitry.

The digital core provides the engine for receiving, processing, and sending all USB-PD packets as well as handling control of all other SN1804044ZBHR functionality. A portion of the digital core contains ROM memory which contains all the firmware required to execute Type-C and PD applications. In addition, a section of the ROM, called *boot code*, is capable of initializing the SN1804044ZBHR device, loading of device configuration information for up to two devices, and loading any code patches into volatile memory in the digital core. See the *Digital Core* section for a high-level block diagram of the digital core, a description of the features, and more detailed circuitry.

The digital core of the SN1804044ZBHR device also interprets and uses information provided by the analog-to-digital converter (ADC) (see the *ADC* section), is configurable to read the status of general purpose inputs and trigger events accordingly, and controls general outputs which are configurable as push-pull or open-drain types with integrated pullup or pulldown resistors and can operate tied to a 1.8-V or 3.3-V rail. The SN1804044ZBHR is an I^2C slave to be controlled by a host processor (see the *I^2C Slave Interface* section), an SPI master to write to and read from an optional external flash memory (see the *SPI Master Interface* section), and is programmed by a single-wire debugger (SWD) connection (see the *Single-Wire Debugger Interface* section).

The SN1804044ZBHR device also integrates a thermal shutdown mechanism (see the *Thermal Shutdown* section) and runs off of accurate clocks provided by the integrated oscillators (see the *Oscillators* section).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 USB-PD Physical Layer

Figure 10 shows the block for the USB-PD physical layer surrounded by a simplified version of the analog plug and orientation detection block.

Feature Description (continued)

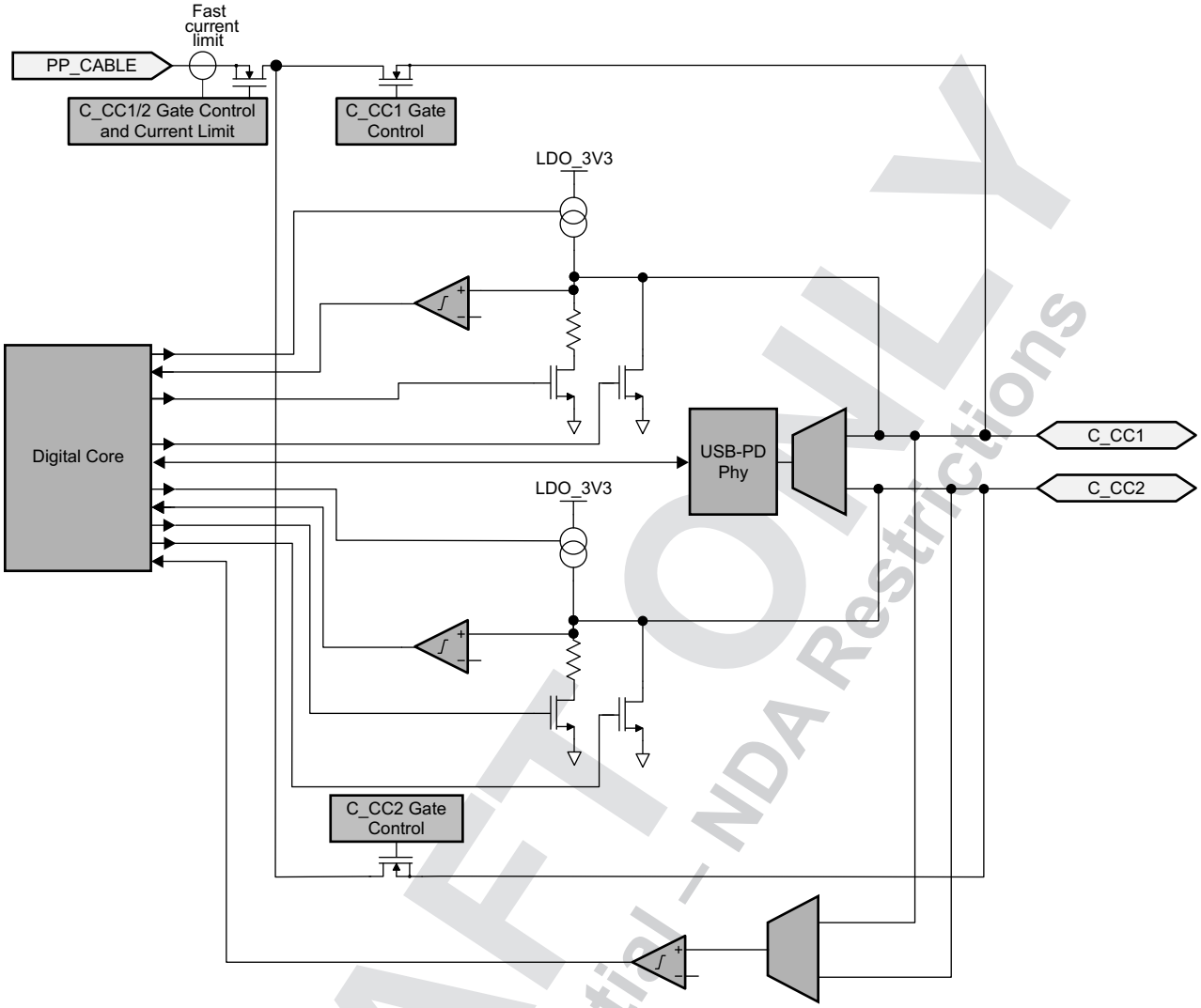


Figure 10. USB-PD Physical Layer and Simplified Plug and Orientation Detection Circuitry

USB-PD messages are transmitted in a USB Type-C system using a BMC signaling. The BMC signal is output on the same pin (C_CC1 or C_CC2) that is DC biased because of the DFP (or UFP) cable-attach mechanism described in the *Cable-Plug and Orientation Detection* section.

8.3.1.1 USB-PD Encoding and Signaling

Figure 11 shows the high-level block diagram of the baseband USB-PD transmitter. Figure 12 shows the high-level block diagram of the baseband USB-PD receiver.

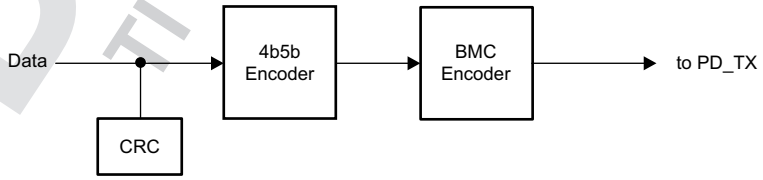


Figure 11. USB-PD Baseband Transmitter Block Diagram

Feature Description (continued)

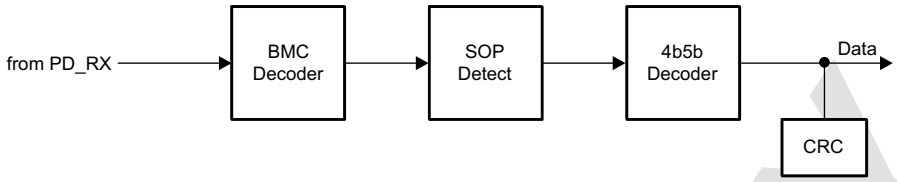


Figure 12. USB-PD Baseband Receiver Block Diagram

The USB-PD baseband signal is driven on the C_CCn pins with a tri-state driver. The tri-state driver is slew-rate limited to reduce the high frequency components imparted on the cable and to avoid interference with frequencies used for communication.

8.3.1.2 USB-PD Biphase-Marked Coding

The USBP-PD physical layer implemented in the SN1804044ZBHR device is compliant with the USB-PD Specifications. The encoding scheme used for the baseband PD signal is a version of Manchester coding called Biphase Mark Coding (BMC). In this code, a transition occurs at the start of every bit time and a second transition occurs in the middle of the bit cell when a 1 is transmitted. This coding scheme is nearly DC balanced with limited disparity (limited to ½ bit over an arbitrary packet, so a very low DC level). Figure 13 shows Biphase Mark Coding.

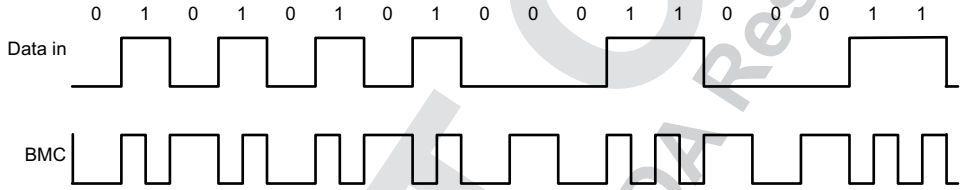


Figure 13. Biphase Mark Coding Example

The USB PD baseband signal is driven onto the C_CC1 or C_CC2 pins with a tri-state driver. The tri-state driver is slew rate to limit coupling to D+/D– and to other signal lines in the Type-C fully featured cables. When sending the USB-PD preamble, the transmitter starts by transmitting a low level. The receiver at the other end tolerates the loss of the first edge. The transmitter terminates the final bit by an edge to ensure the receiver clocks the final bit of EOP.

8.3.1.3 USB-PD Transmit (TX) and Receive (Rx) Masks

The USB-PD driver meets the defined USB-PD BMC TX masks. Because a BMC of 1 contains a signal edge at the beginning and middle of the UI, and the BMC of 0 contains only an edge at the beginning, the masks are different for each. The USB-PD receiver meets the defined USB-PD BMC Rx masks. The boundaries of the Rx outer mask are specified to accommodate a change in signal amplitude because of the ground offset through the cable. The Rx masks are therefore larger than the boundaries of the TX outer mask. Similarly, the boundaries of the Rx inner mask are smaller than the boundaries of the TX inner mask. Triangular time masks are superimposed on the TX outer masks and defined at the signal transitions to require a minimum edge rate that has minimal impact on adjacent higher speed lanes. The TX inner mask enforces the maximum limits on the rise and fall times. Refer to the USB-PD Specifications for more details.

8.3.1.4 USB-PD BMC Transmitter

The SN1804044ZBHR device transmits and receives USB-PD data over one of the C_CCn pins. The C_CCn pin is also used to determine the cable orientation (see the *Cable-Plug and Orientation Detection* section) and maintain cable and device attach detection. Therefore, a DC bias exists on the C_CCn. The transmitter driver overdrives the C_CCn DC bias while transmitting, but returns to a Hi-Z state allowing the DC voltage to return to the C_CCn pin when not transmitting. Figure 14 shows the USB-PD BMC TX and Rx driver block diagram.

Feature Description (continued)

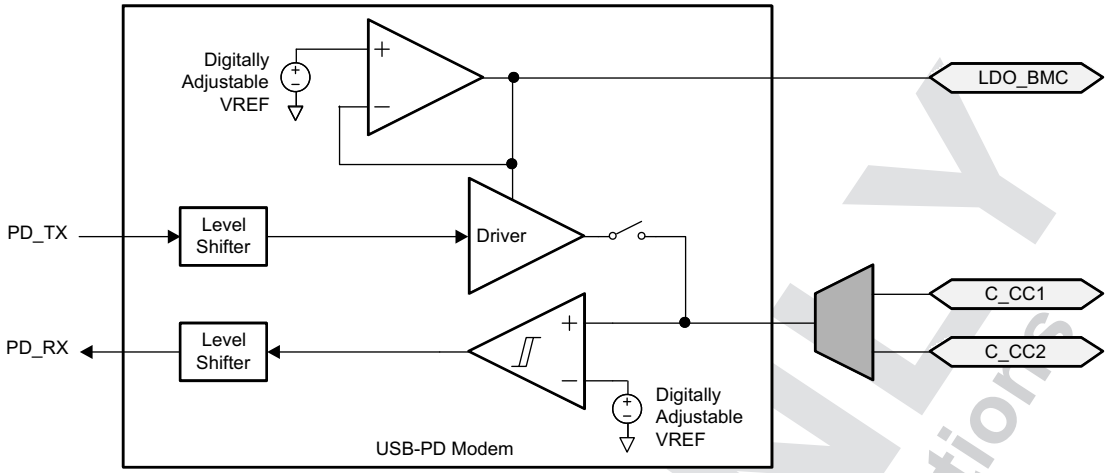


Figure 14. USB-PD BMC TX/Rx Block Diagram

Figure 15 shows the transmission of the BMC data on top of the DC bias.

NOTE

The DC bias can be anywhere between the minimum threshold for detecting a UFP attach (VD_CCH_USB) and the maximum threshold for detecting a UFP attach to a DFP (VD_CCH_3P0) defined in the *Cable-Plug and Orientation Detection* section. Therefore, the DC bias can be less than the VOH of the transmitter driver or greater than VOH.

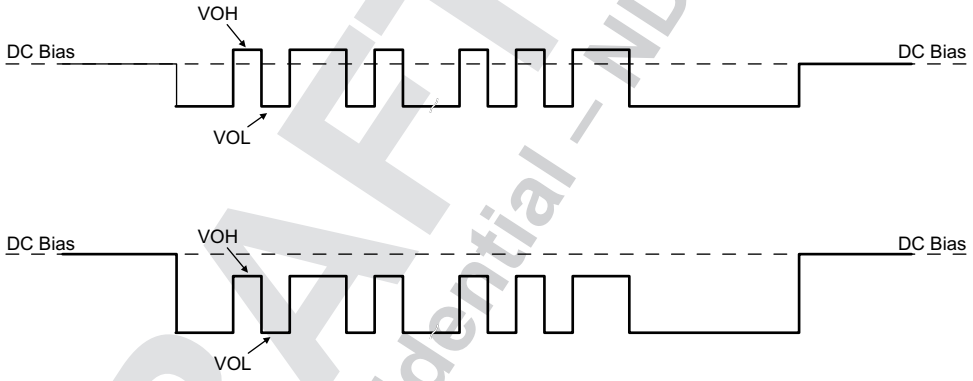


Figure 15. TX Driver Transmission with DC Bias

The transmitter drives a digital signal onto the C_CCn lines. The signal peak VTXP is adjustable by application code and sets the VOH and VOL for the BMC data that is transmitted, and is defined in *USB-PD TX Driver Voltage Adjustment Parameter* section. The settings in a final system must meet the TX masks defined in the USB-PD Specifications.

When driving the line, the transmitter driver has an output impedance of ZDRIVER. ZDRIVER is determined by the driver resistance and the shunt capacitance of the source and is frequency dependent. ZDRIVER impacts the noise ingression in the cable.

Figure 16 shows the simplified circuit determining ZDRIVER and is specified such that noise at the receiver is bounded.

Use Equation 1 to calculate the value of ZDRVER.

Feature Description (continued)

$$ZDRIVER = \frac{R_{DRIVER}}{1 + s \times R_{DRIVER} \times C_{DRIVER}} \quad (1)$$

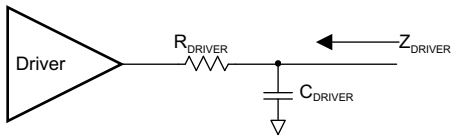


Figure 16. ZDRIVER Circuit

8.3.1.5 USB-PD BMC Receiver

The receiver block of the SN1804044ZBHR device receives a signal that falls within the allowed Rx masks defined in the USB PD specification. The receive thresholds and hysteresis come from this mask. The values for VRXTR and VRXTF are listed in *USB-PD Baseband Signal Characteristics*.

Figure 17 shows an example of a multi-drop USB-PD connection. This connection has the typical UFP (device) to DFP (host) connection, but also includes cable USB-PD TX/Rx blocks. Only one system can be transmitting at a time. All other systems are Hi-Z (ZBMCRX). The USB-PD Specification also specifies the capacitance that can exist on the wire as well as a typical DC bias-setting circuit for attach detection.

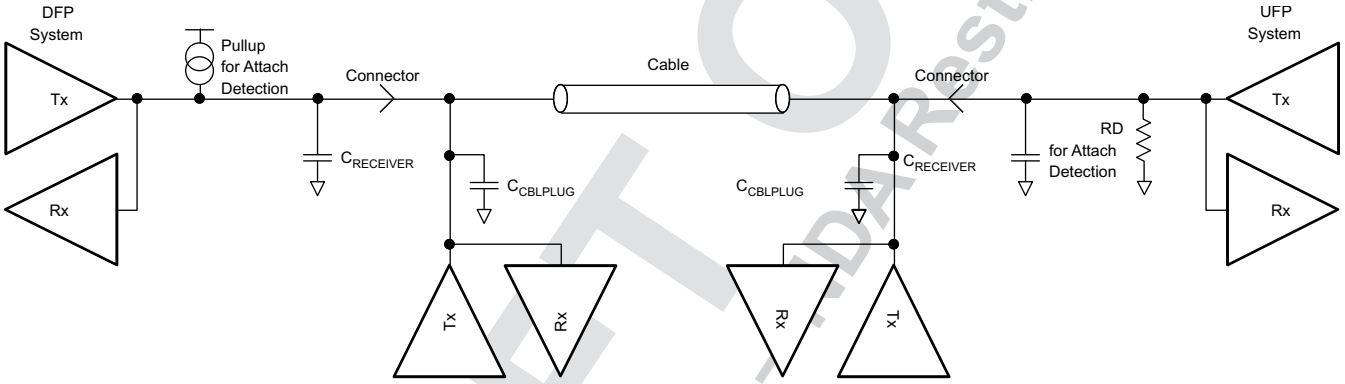


Figure 17. Example USB-PD Multi-Drop Configuration

8.3.2 Cable-Plug and Orientation Detection

Figure 18 shows the plug and orientation detection block at each C_CC pin (C_CC1 and C_CC2). Each pin has identical detection circuitry.

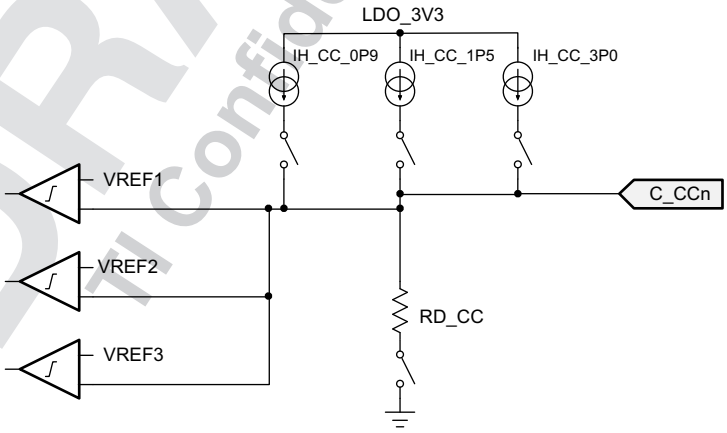


Figure 18. Plug and Orientation Detection Block

Feature Description (continued)

8.3.2.1 Configured as a DFP

When configured as a DFP, the SN1804044ZBHR device detects when a cable or a UFP is attached using the C_CC1 and C_CC2 pins. When in a disconnected state, the SN1804044ZBHR device monitors the voltages on these pins to determine what, if anything, is connected. Refer to the USB Type-C Specification for more information.

Table 1 lists the high-level detection results. Refer to the USB Type-C Specification for more information.

Table 1. Cable Detect States for a DFP

C_CC1	C_CC2	CONNECTION STATE	RESULTING ACTION
Open	Open	Nothing attached	Continue monitoring both C_CC pins for attach. Power is not applied to VBUS or VCONN until a UFP connect is detected.
Rd	Open	UFP attached	Monitor C_CC1 for detach. Power is applied to VBUS but not to VCONN (C_CC2).
Open	Rd	UFP attached	Monitor C_CC2 for detach. Power is applied to VBUS but not to VCONN (C_CC1).
Ra	Open	Powered cable and no UFP attached	Monitor C_CC2 for a UFP attach and C_CC1 for cable detach. Power is not applied to VBUS or VCONN (C_CC1) until a UFP attach is detected.
Open	Ra	Powered cable and no UFP attached	Monitor C_CC1 for a UFP attach and C_CC2 for cable detach. Power is not applied to VBUS or VCONN (C_CC1) until a UFP attach is detected.
Ra	Rd	Powered cable and no UFP attached	Provide power on VBUS and VCONN (C_CC1) then monitor C_CC2 for a UFP detach. C_CC1 is not monitored for a detach.
Rd	Ra	Powered cable and no UFP attached	Provide power on VBUS and VCONN (C_CC2) then monitor C_CC1 for a UFP detach. C_CC2 is not monitored for a detach.
Rd	Rd	Debug accessory mode attached	Sense either C_CC pin for detach.
Ra	Ra	Audio adapter accessory Mode attached	Sense either C_CC pin for detach.

When the SN1804044ZBHR device is configured as a DFP, a current IH_CC is driven out each C_CCn pin and each pin is monitored for different states. When a UFP is attached to the pin, a pulldown resistance of Rd to GND exists. The current IH_CC is then forced across the resistance Rd generating a voltage at the C_CCn pin.

When configured as a DFP advertising default, USB-current sourcing capability, the SN1804044ZBHR device applies IH_CC_USB to each C_CCn pin. When a UFP with a pulldown resistance of Rd is attached, the voltage on the C_CCn pin pulls below VH_CCD_USB. The SN1804044ZBHR device can also be configured as a DFP to advertise default (500 mA), 1.5 A and 3-A sourcing capabilities.

When the C_CCn pin is connected to an active cable VCONN (power to the active cable), the pulldown resistance is different (Ra). In this case, the voltage on the C_CCn pin pulls below VH_CCA_USB/1P5/3P0 and the system recognizes the active cable.

The VH_CCD_USB/1P5/3P0 thresholds are monitored to detect a disconnection from each of these cases respectively. When a connection is recognized and the voltage on the C_CCn pin rises above the VH_CCD_USB/1P5/3P0 threshold, the system registers a disconnection.

8.3.2.2 Configured as a UFP

When the SN1804044ZBHR device is configured as a UFP, the SN1804044ZBHR device presents a pulldown resistance of RD_CC on each C_CCn pin and waits for a DFP to attach and pull up the voltage on the pin. The DFP pulls up the C_CC pin by applying either a resistance or a current. The UFP detects an attachment by the presence of VBUS. The UFP determines the advertised current from the DFP by the pullup applied to the C_CCn pin.

8.3.2.3 Dead-Battery or No-Battery Support

Type-C USB ports require a sink to present Rd on the CC pin before a USB Type-C source provides a voltage on VBUS. The SN1804044ZBHR device is hardware-configurable to present this Rd during a dead-battery or no-battery condition. Additional circuitry provides a mechanism to turn off this Rd when the port is acting as a source. Figure 19 shows the RPD_Gn pin used to configure the behavior of the C_CCn pins, and elaborates on the basic cable-plug and orientation detection block shown in Figure 18. RPD_G1 and RPD_G2 configure

C_CC1 and C_CC2 respectively. A resistance of R_RPD is connected to the gate of the pulldown FET on each C_CCn pin. This resistance must be pin-strapped externally to configure the C_CCn pin to behave in one of two ways: present an Rd pulldown resistance or present a Hi-Z when the SN1804044ZBHR device is unpowered. During normal operation, Rd is RD_CC; however, while dead-battery or no-battery conditions exist, the resistance is untrimmed and is RD_DB. When RD_DB is presented during dead-battery or no-battery, the application code switches to RD_CC.

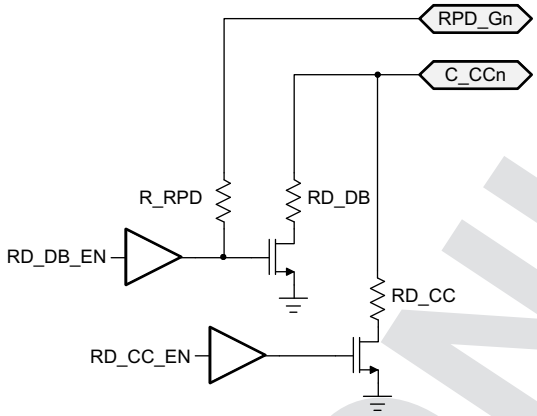


Figure 19. C_CCn and RPD_Gn pins

When C_CC1 is shorted to RPD_G1 and C_CC2 is shorted to RPD_G2 in an application using the SN1804044ZBHR device, booting from a dead-battery or no-battery conditions is supported. In this case, the gate driver for the pulldown FET is Hi-Z at the output. When an external connection pulls up on C_CCn (the case when connected to a DFP advertising with a pullup resistance Rp or pullup current), the connection through R_RPD pulls up on the FET gate turning on the pulldown through RD_DB. In this condition, the C_CCn pin acts as a clamp VTH_DB in series with the resistance RD_DB.

When RPD_G1 and RPD_G2 are shorted to GND in an application and not electrically connected to C_C1 and C_CC2, booting from a dead-battery or no-battery condition is impossible. In this case, the SN1804044ZBHR device presents a Hi-Z on the C_CC1 and C_CC2 pins and a USB Type-C source never provides a voltage on VBUS.

8.3.3 Port-Power Switches

Figure 20 shows the SN1804044ZBHR port-power path including all internal and external paths. The port-power path provides to VBUS from PP_5V0, provides power to or from an external port power node (shown and referred to as PP_EXT) from or to VBUS, and provides power from PP_CABLE to C_CC1 or C_CC2. The PP_CABLE to C_CCn switches shown in Figure 20 are the same as in Figure 10, but are now shown without the analog USB Type-C cable-plug and orientation detection circuitry.

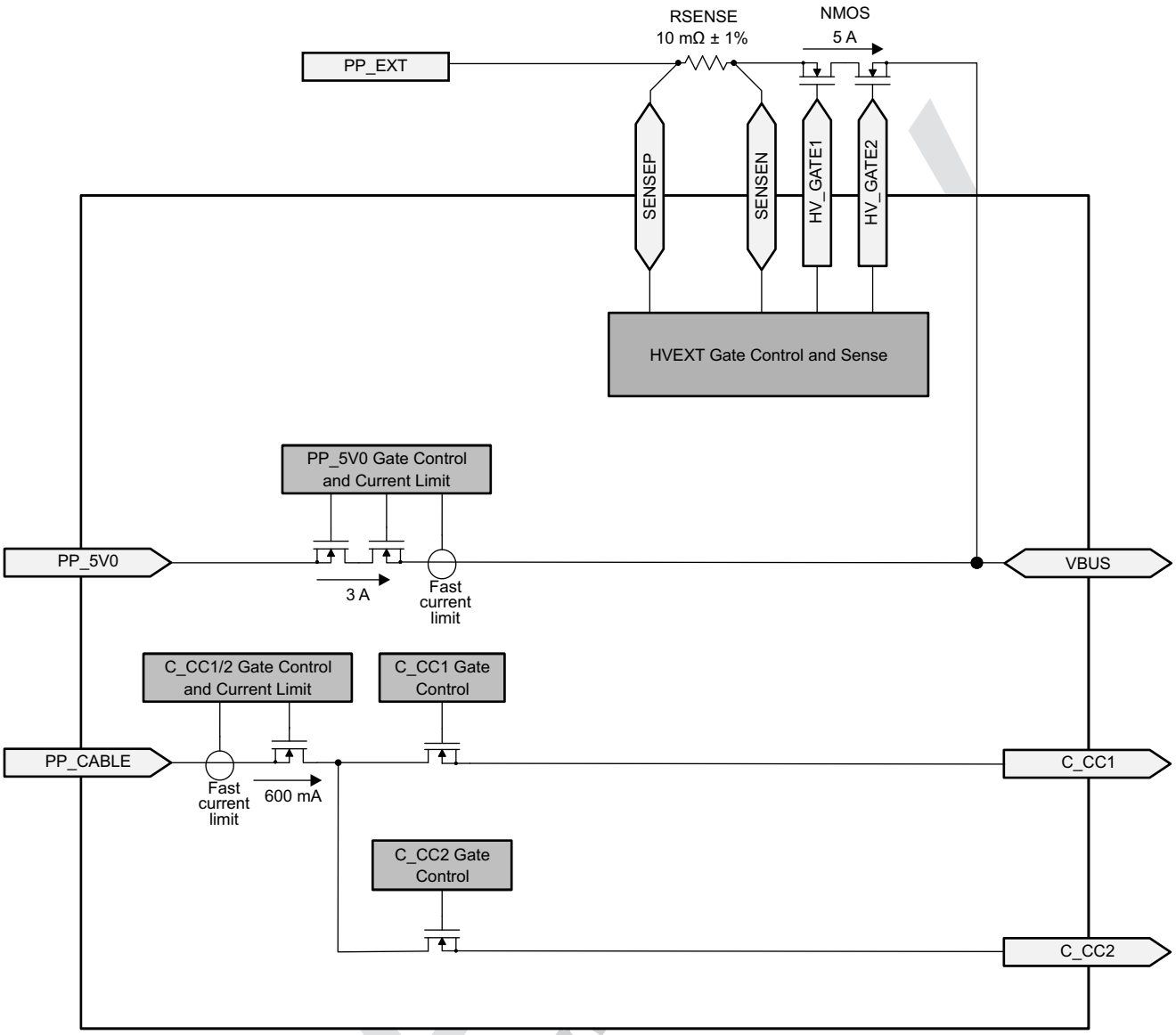


Figure 20. Port-Power Paths

8.3.3.1 5-V Power Delivery

The SN1804044ZBHR device provides port power to VBUS from PP_5V0 when a low voltage output is required. The switch path provides 5 V at up to 3 A to from PP_5V0 to VBUS. Figure 20 shows a simplified circuit for the switch from PP_5V0 to VBUS.

8.3.3.2 5-V Power Switch as a Source

The PP_5V0 path is unidirectional, only sourcing power from PP_5V0 to VBUS. When the switch is on, the protection circuitry limits reverse current from VBUS to PP_5V0. Figure 21 shows the I-V characteristics of the reverse-current protection feature. Figure 21 and the reverse-current limit can be approximated using Equation 2.

$$IREV5V0 = VREV5V0/RPP5V \quad (2)$$

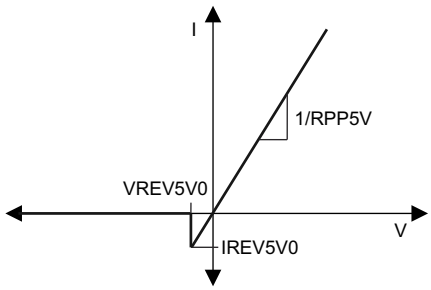


Figure 21. 5V Switch I-V Curve

8.3.3.3 PP_5V0 Current Sense

The current from PP_5V0 to VBUS is sensed through the switch and is available to be read digitally through the ADC.

8.3.3.4 PP_5V0 Current Limit

The current through PP_5V0 to VBUS is limited to ILIMPP5V and is controlled automatically by the digital core. When the current exceeds ILIMPP5V, the current-limit circuit activates. Depending on the severity of the overcurrent condition, the transient response reacts in one of two ways: and Figure 23 show the approximate response time and clamping characteristics of the circuit for a hard short while Figure 24 shows the shows the approximate response time and clamping characteristics for a soft short with a load of 2 Ω.

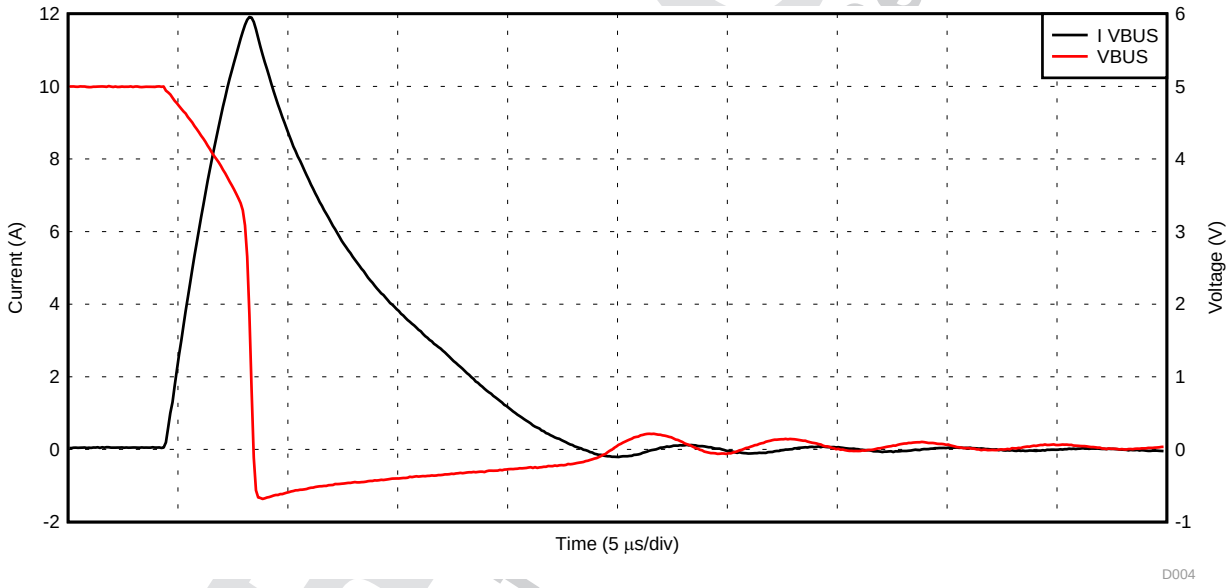


Figure 22. PP_5V0 Current Limit With a Hard Short

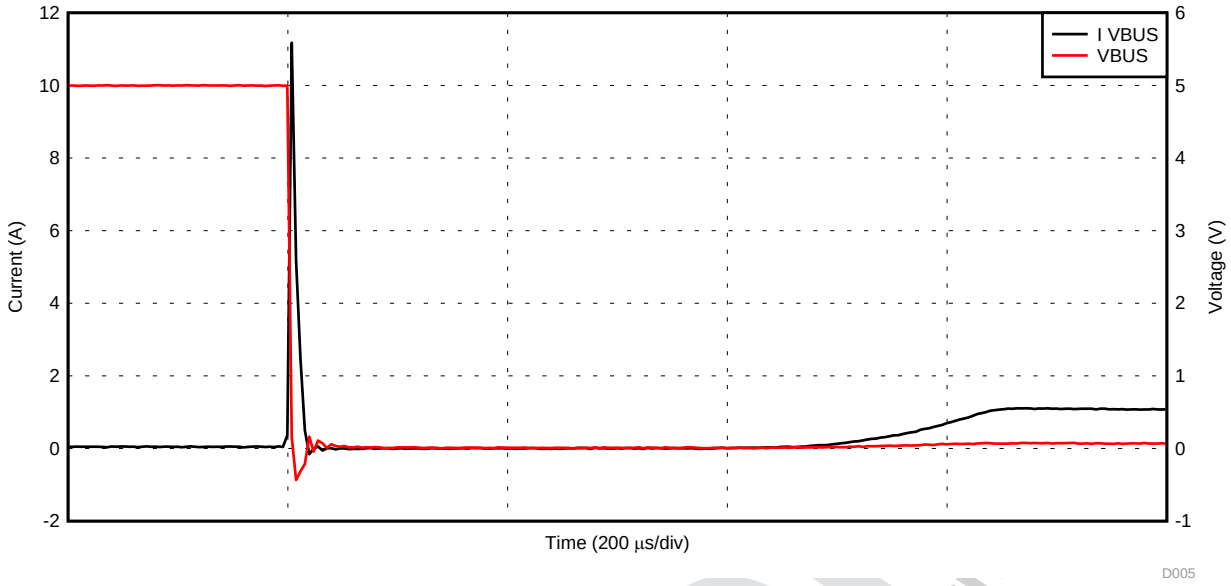


Figure 23. PP_5V0 Current Limit With a Hard Short (Extended Time Base)

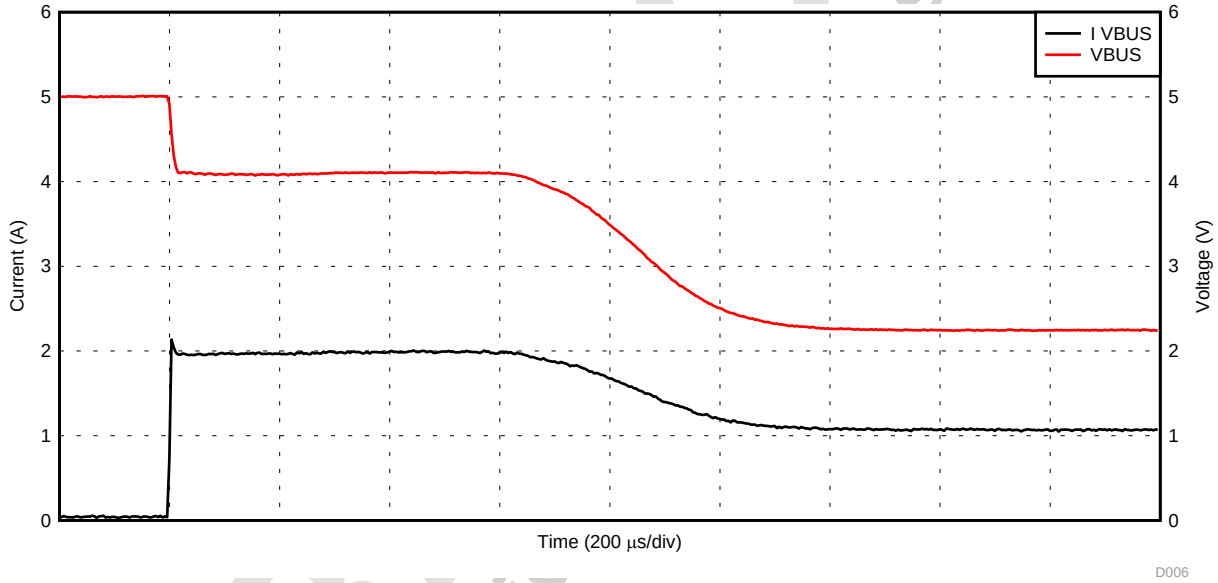


Figure 24. PP_5V0 Current Limit With a Soft Short (2 Ω)

8.3.3.5 12.4 Fast Role Swap

The PD Controller supports the USB PD fast role swap capability as either the Source or the Sink. When in a Fast Role Swap mode as a Source and the system indicates the need to perform a fast role swap, the PD Controller will send the Fast Role Swap signal to the sink for TFRSTX time while pulling the Type-C CC line low with a RFRSTX resistance. When this signal is sent, the PD Controller will cease operating as the Source and switch to operating as the Sink.

The PD Controller supports the USB PD fast role swap capability as either the Source or the Sink. When in a Fast Role Swap mode as a Source and the system indicates the need to perform a fast role swap, the PD Controller will send the Fast Role Swap signal to the sink for TFRSTX time while pulling the Type-C CC line low with a RFRSTX resistance. When this signal is sent, the PD Controller will cease operating as the Source and switch to operating as the Sink.

8.3.3.6 External HV Power Delivery

The SN1804044ZBHR device is capable of controlling an external high-voltage, common-drain back-to-back NMOS FET switch path to source or sink power up to the maximum limit of the USB PD specification which is 20 V at 5 A of current. The SN1804044ZBHR device provides external control and sense to external NMOS power switches for currents greater than 3 A. This path is bidirectional for either sourcing current to VBUS or sinking current from VBUS. The external NMOS switches are back-to-back to protect the system from a large voltage differential across the FETs as well as blocking reverse current flow. Each NFET has a separate gate control. HV_GATE2 is always connected to the VBUS side and HV_GATE1 is always connected to the opposite side, referred to as PP_EXT. Two sense pins, SENSEP and SENSEN, are used to implement reverse-current blocking, overcurrent protection, and current sensing.

8.3.3.7 External HV Power Switch as a Source With RSENSE

Figure 20 shows the configuration when the SN1804044ZBHR device acts as a source for the external switch path. The external FETs must be connected in a common-drain configuration and do not work in a common source configuration. In this mode, current is sourced to VBUS. RSENSE provides an accurate current measurement and is used to initiate the current limiting feature of the external power path. The voltage between SENSEP (PP_EXT) and SENSEN (VBUS) is sensed to block reverse current flow. This measurement is also digitally readable through the ADC.

8.3.3.8 External HV Power Switch as a Sink With RSENSE

Figure 25 shows the configuration when the SN1804044ZBHR device is acting as a sink for the external switch path with RSENSE used to sense current. Acting as a sink, the voltage between SENSEP (VBUS) and SENSEN (PP_EXT) is sensed to provide an accurate current measurement and initiate the current limiting feature of the external power path. This measurement is also digitally readable through the ADC.

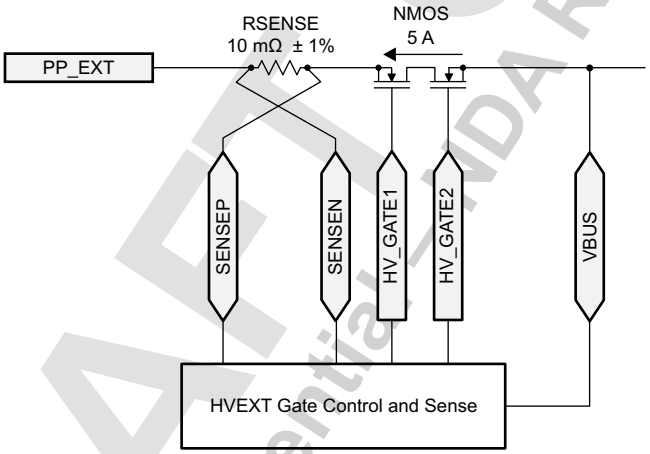


Figure 25. External HV Switch as a Sink with RSENSE

8.3.3.9 External HV Power Switch as a Sink Without RSENSE

Figure 26 shows the configuration when the SN1804044ZBHR device is acting as a sink for the external switch path without an RSENSE resistor. In this mode, current is sunk from VBUS to an internal system-power node, referred to as PP_EXT. This node is used for charging a battery or for providing a supply voltage for a bus-powered device. To block the reverse current, the VBUS and SENSEP pins monitor the voltage across the NFETs. To ensure that SENSEN does not float, tie SENSEP to SENSEN in this configuration. When configured in this mode, the digital readout from current from the ADC is approximately zero.

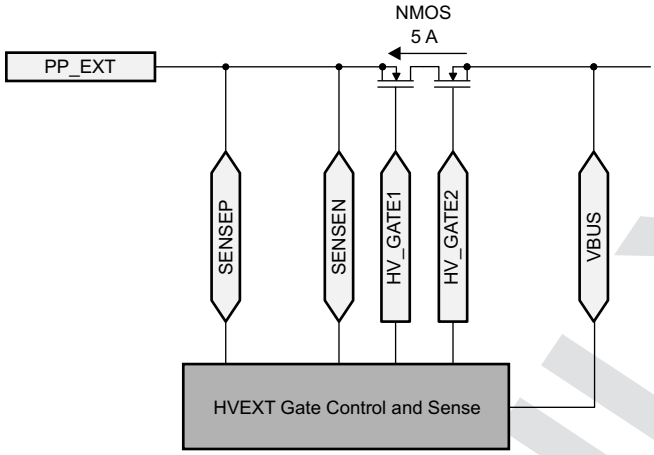


Figure 26. External HV Switch as a Sink Without RSENSE

8.3.3.10 External Current Sense

The current through the external NFETs to VBUS is sensed through the RSENSE resistor and is available to be read digitally through the ADC. When acting as a source, the readout from the ADC only accurately reflects the current through the external NFETs when the connection of SENSEP and SENSEN adheres to Figure 20. When acting as a sink, the readout from the ADC only accurately reflects the current through the external NFETs when the connection of SENSEP and SENSEN adheres to Figure 25.

8.3.3.11 External Current Limit

The current through the external NFETs to VBUS is current limited when acting as a source or a sink. The current is sensed across the external RSENSE resistance. The current limit is set by a combination of the RSENSE magnitude and configuration settings for the voltage across the resistance. When the voltage across the RSENSE resistance exceeds the automatically set-voltage limit, the current-limit circuit is activated.

8.3.3.12 Soft Start

When configured as a sink, the SS pin provides a soft-start function for each of the high-voltage power-path supplies (P_HV and external PP_EXT path) up to 5.5 V. The SS circuitry is shared for each path and only one path turns on as a sink at a time. The soft-start function is enabled by application code or through the host processor. The SS pin is initially discharged through a resistance RSS_DIS. When the switch is turned on, a current, ISS, is sourced from the pin to a capacitance, CSS. This current into the capacitance generates a slow ramping voltage. This voltage is sensed and the power-path FETs turn on and the voltage follows this ramp. When the voltage reaches the threshold, VTHSS, the power-path FET is close to being completely turned on, the output voltage is completely charged. At time, TSSDONE, a signal to the digital core indicates that the soft-start function has completed. Use Equation 3 to calculate the ramp rate of the supply.

$$\text{Ramp Rate} = 9 \times \frac{\text{ISS}}{\text{CSS}} \tag{3}$$

The maximum ramp voltage for the supply is approximately 16.2 V. For any input voltage higher than this, the ramp stops at 16.2 V until the firmware disables the soft start. At this point, the voltage steps to the input voltage at a ramp rate defined by approximately 7 μA into the gate capacitance of the switch. The TSSDONE time is independent of the actual final ramp voltage.

8.3.3.13 BUSPOWERZ

At power-up, when VIN_3V3 is not present and a dead-battery condition is supported as described in the *Dead-Battery or No-Battery Support* section, the SN1804044ZBHR device appears as a USB Type-C sink (device) causing a connected USB Type-C source (host) to provide 5 V on VBUS. The SN1804044ZBHR device receives power from the 5-V VBUS rail (see *Power Management*) and executes boot code (see the *Boot Flow* section). The boot code observes the BUSPOWERZ voltage, which falls into one of two voltage ranges: VBPZ_DIS and VBPZ_EXT (defined in the *BUSPOWERZ Configuration Characteristics* section). These two voltage ranges configure how the SN1804044ZBHR device routes the 5 V present on VBUS to the system in a dead-battery or no-battery scenario.

When the voltage on BUSPOWERZ is in the VBPZ_DIS range (when BUSPOWERZ is tied to LDO_3V3 as in Figure 27), the device does not route the 5 V present on VBUS to the entire system. This configuration disables the PP_EXT high-voltage switches and only uses VBUS to power the SN1804044ZBHR device. In this case, both the PP_HV_EN and PP_HVEXT_EN GPIO remain low.

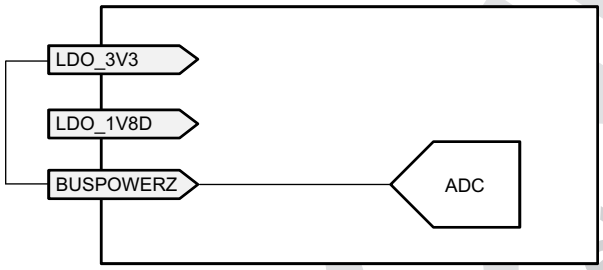


Figure 27. BUSPOWERZ Configured to Disable Power from VBUS

The BUSPOWERZ pin can also alternately configure the SN1804044ZBHR device to power the entire system through the PP_EXT external load switch when the voltage on BUSPOWERZ is in the VBPZ_EXT range (when BUSPOWERZ is tied to GND as in Figure 28). In this case, the PP_HVEXT_EN GPIO is asserted high and the PP_HV_EN GPIO remains low.

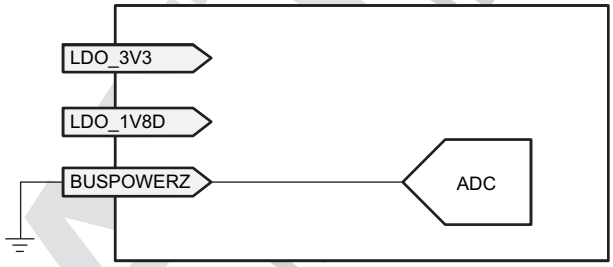


Figure 28. BUSPOWERZ Configured With PP_EXT as Input Power Path

Lastly, BUSPOWERZ pin can configure the SN1804044ZBHR to assert the PP_HV_EN GPIO. This assertion allows the entire system to power through an external through the load switch, controlled by the PP_HV_EN signal, when the voltage on BUSPOWERZ is in the VBPZ_HV_EN range (when a 100-kΩ pullup resistor is tied from BUSPOWERZ to LDO_1V8D as shown in Figure 29). In this case, the PP_HV_EN GPIO is asserted high and the PP_HVEXT_EN GPIO remains low.

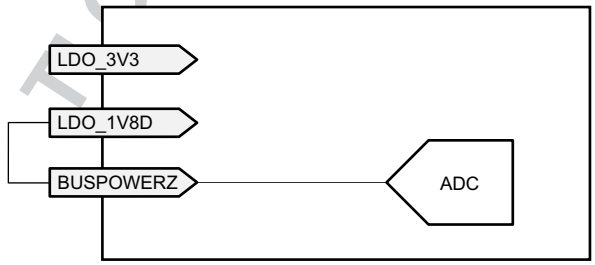


Figure 29. BUSPOWERZ Configured With PP_HV_EN GPIO Assertion

8.3.3.14 Voltage Transitions on VBUS Through Port Power Switches

Figure 30 shows the waveform for a positive voltage transition. The timing and voltages apply to both a transition from 0 V to PP_5V0 as well as a transition from PP_5V0 to a PP_EXT. When a switch is closed to transition the voltage, a maximum slew rate of SRPOS occurs on the transition. The voltage ramp remains monotonic until the voltage reaches VSRCVALID within the final voltage. The voltage may overshoot the new voltage by VSRCVALID. After a time, TSTABLE, from the start of the transition, the voltage falls within VSRCNEW of the new voltage. During the time, TSTABLE, the voltage may fall lower than the new voltage, but remains within VSRCNEW of this voltage.

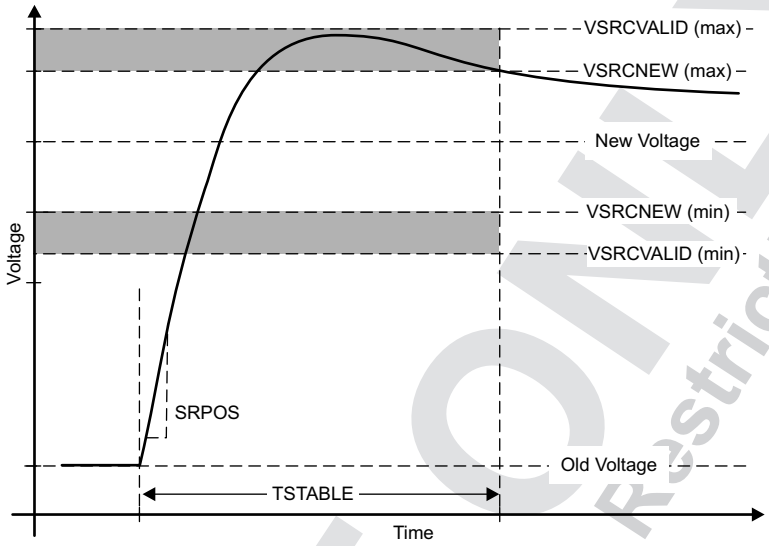


Figure 30. Positive Voltage Transition on VBUS

Figure 31 shows the waveform for a negative voltage transition. The timing and voltages apply to a transition from PP_5V0 to 0 V as well as a transition from PP_EXT to PP_5V0. When a switch is closed to transition the voltage, a maximum slew-rate of SRNEG occurs on the transition. The voltage ramp remains monotonic until the voltage reaches TOLTRANUN within the final voltage. The voltage may overshoot the new voltage by TOLTRANLN. After a time, TSTABLE, from the start of the transition, the voltage falls within VSRCNEW of the new voltage. During the time, TSTABLE, the voltage may fall lower then the new voltage, but remains within VSRCNEW of this voltage.

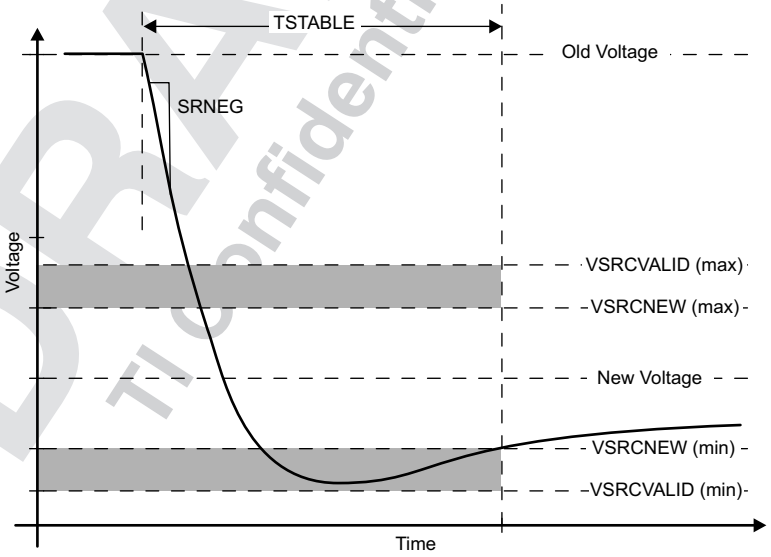


Figure 31. Negative Voltage Transition on VBUS

8.3.3.15 HV Transition to PP_5V0 Pull-Down on VBUS

The SN1804044ZBHR device has an integrated active pulldown on VBUS when transitioning from PP_EXT to PP_5V0 (see Figure 32). When the PP_EXT switch is disabled and VBUS > PP_5V0 + VHVDISPD, amplifier turns on a current source and pulls down on VBUS. The amplifier implements active slew -rate control by adjusting the pulldown current to prevent the slew rate from exceeding the specification. When VBUS falls to within VHVDISPD of PP_5V0, the pulldown is turned off. The load on VBUS then continues to pull VBUS down until the ideal diode-switch structure turns on connecting it to PP_5V0. When switching from PP_EXT to PP_5V0, PP_EXT must be greater than VSO_HV to follow the switch-over shown in Figure 31.

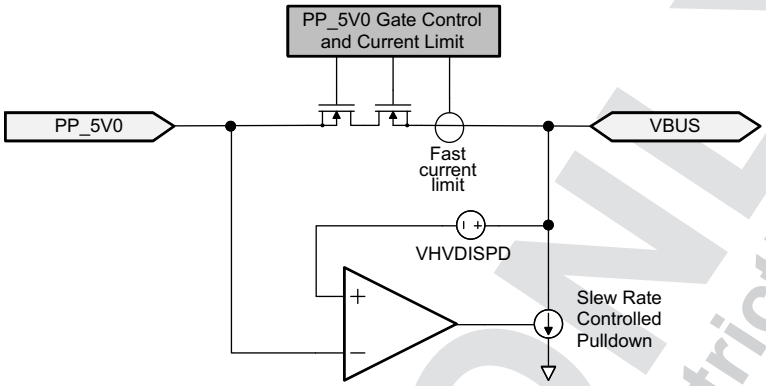


Figure 32. PP_5V0 Slew-Rate Control

8.3.3.16 VBUS Transition to VSAFE0V

When VBUS transitions to almost 0 V (VSAFE0V), the pulldown circuit in Figure 32 turns on until VBUS reaches VSAFE0V. This transition occurs within the time, TSAFE0V.

8.3.3.17 C_CC1 and C_CC2 Power Configuration and Power Delivery

The C_CC1 and C_CC2 pins are used to deliver power to active circuitry inside a connected cable and output USB-PD data to the cable and connected device. Figure 20 shows the C_CC1, and C_CC2 outputs to the port. Only one of these pins is used to deliver power at a time depending on the cable orientation. The other pin is used to transmit USB-PD data through the cable to a connected device.

Figure 33 shows a high-level flow of connecting these pins based on the cable orientation. See the *Cable-Plug and Orientation Detection* section for more detailed information on plug and orientation detection.

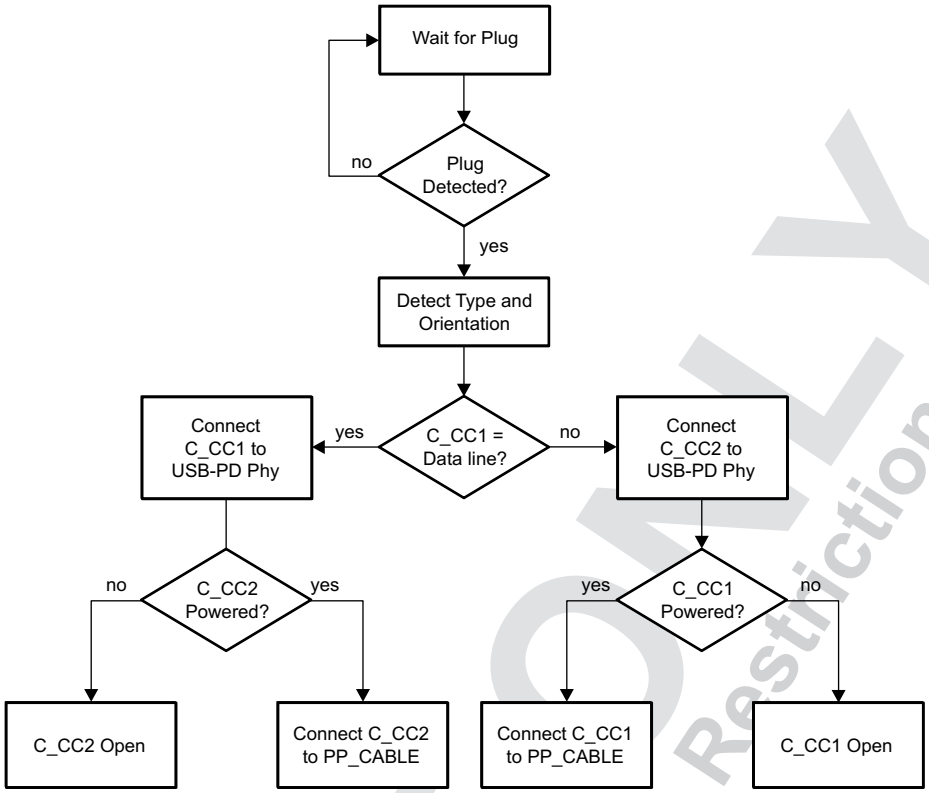


Figure 33. Port C_CC and VCONN Connection Flow

Figure 34 and Figure 35 show the two paths from PP_CABLE to the C_CCn pins. When one C_CCn pin is powered from PP_CABLE, the other is connected to the USB-PD BMC modem.

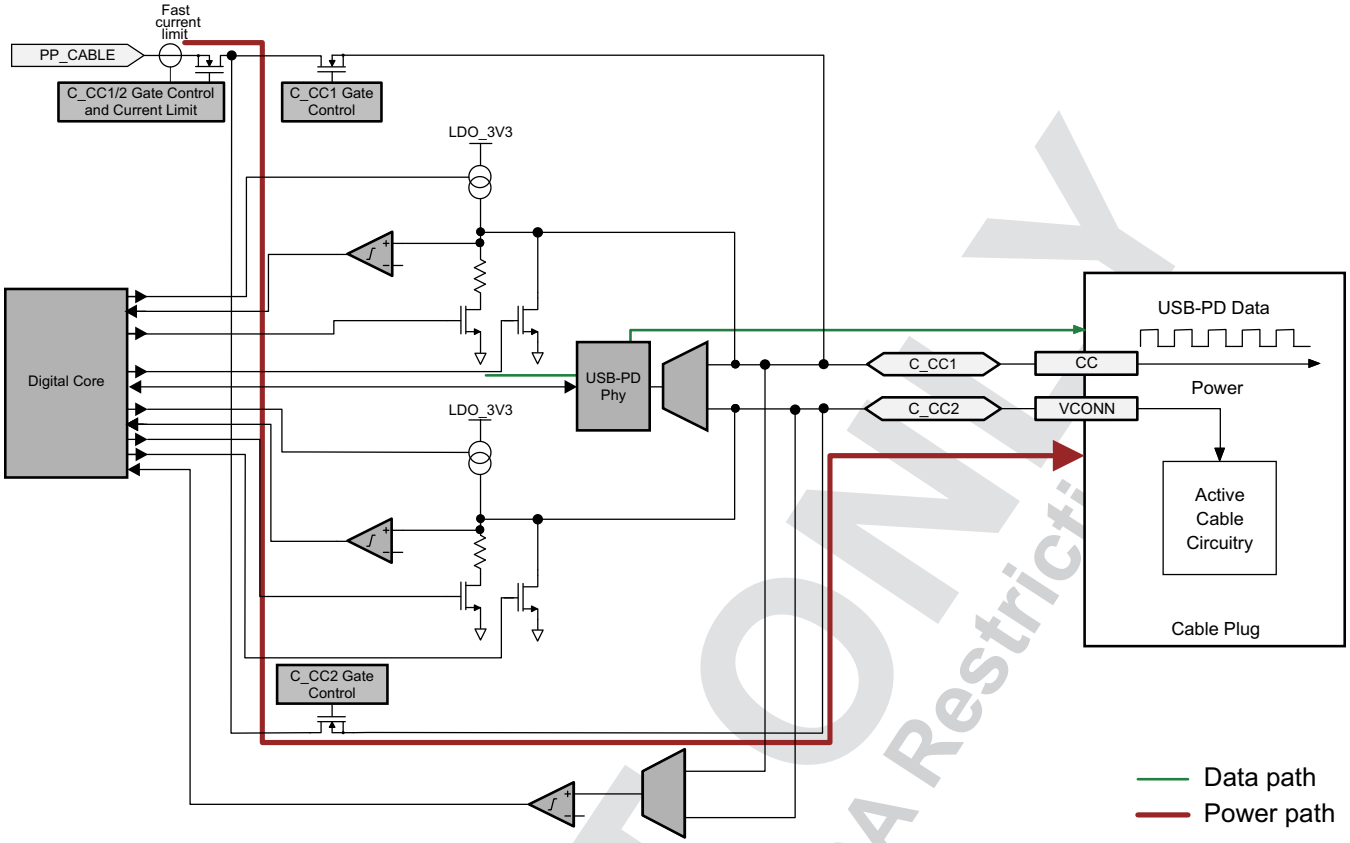


Figure 34. Port C_CC1 and C_CC2 Normal Orientation Power from PP_CABLE

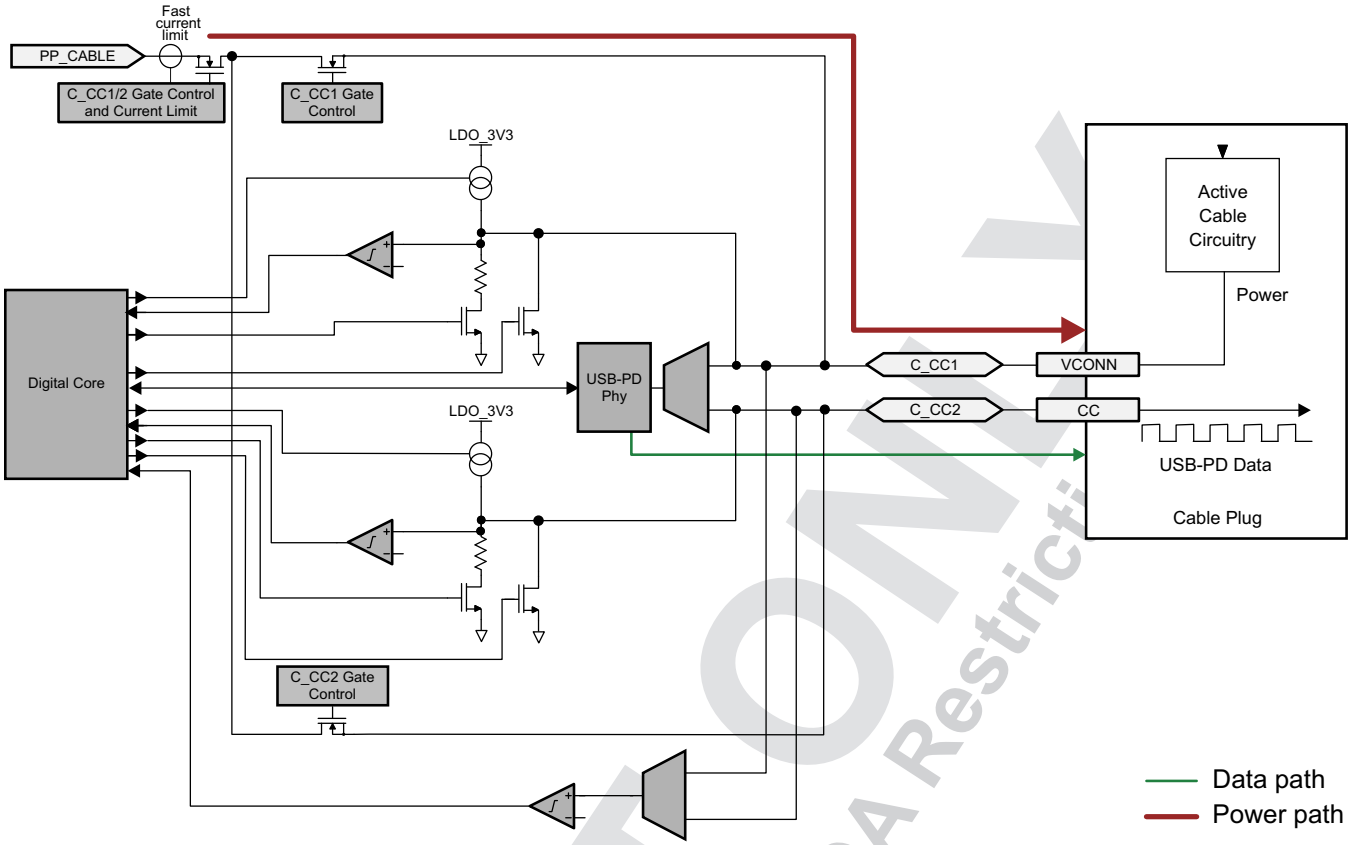


Figure 35. Port C_CC1 and C_CC2 Reverse Orientation Power from PP_CABLE

8.3.3.18 PP_CABLE to C_CC1 and C_CC2 Switch Architecture

Figure 20 shows the switch architecture for the PP_CABLE switch path to the C_CCc pins. Each path provides a unidirectional current from PP_CABLE to C_CC1 and C_CC2. The switch structure blocks reverse current from C_CC1 or C_CC2 to PP_CABLE.

8.3.3.19 PP_CABLE to C_CC1 and C_CC2 Current Limit

The PP_CABLE to C_CC1 and C_CC2 share current limiting through a single FET on the PP_CABLE side of the switch. The current limit, ILIMPPCC, is adjustable between two levels. When the current exceeds ILIMPPCC, the current-limit circuit activates. Depending on the severity of the overcurrent condition, the transient response reacts in one of two ways: Figure 36 and Figure 37 show the approximate response time and clamping characteristics of the circuit for a hard short while Figure 38 shows the approximate response time and clamping characteristics for a soft short. The switch does not have reverse current blocking when the switch is enabled and current is flowing to either C_CC1 or C_CC2.

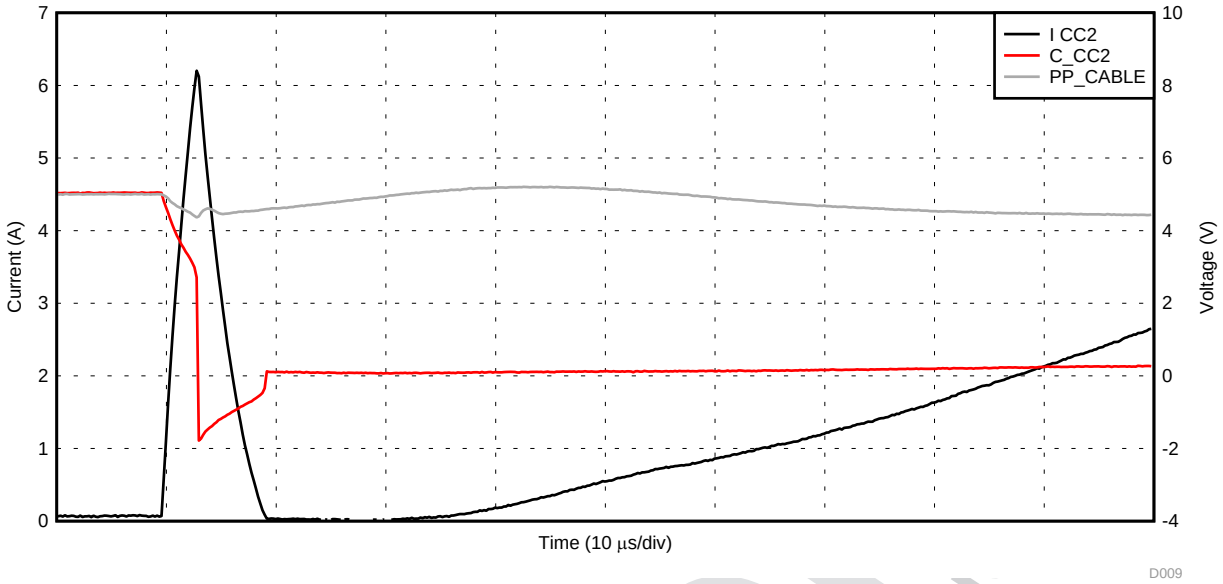


Figure 36. PP_CABLE to C_CCn Current Limit With a Hard Short

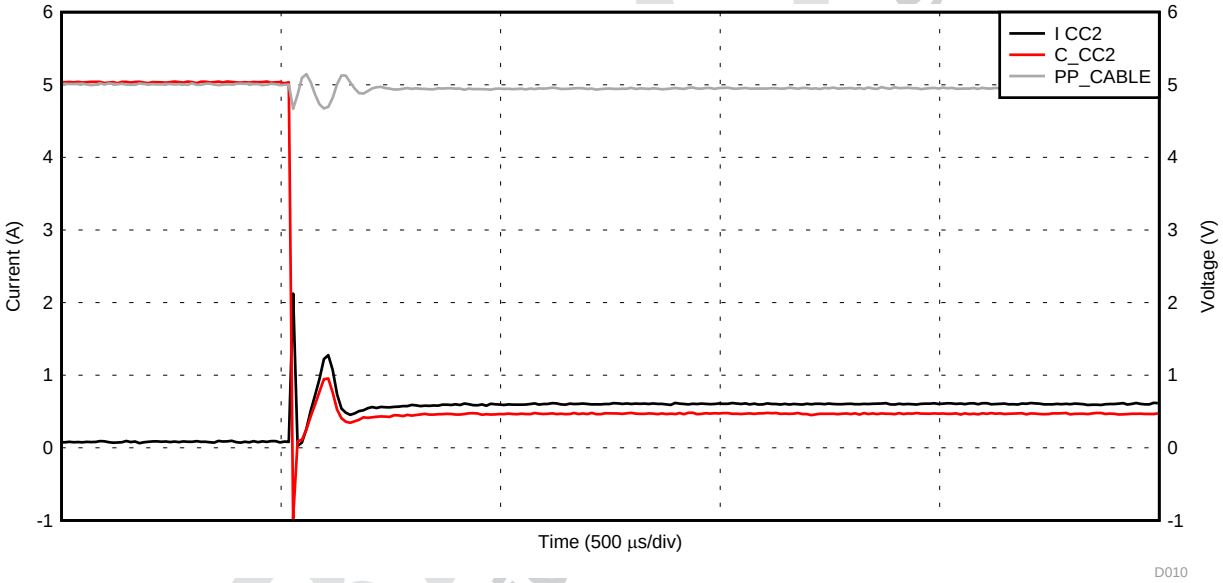


Figure 37. PP_CABLE to C_CCn Current Limit With a Hard Short (Extended Time Base)

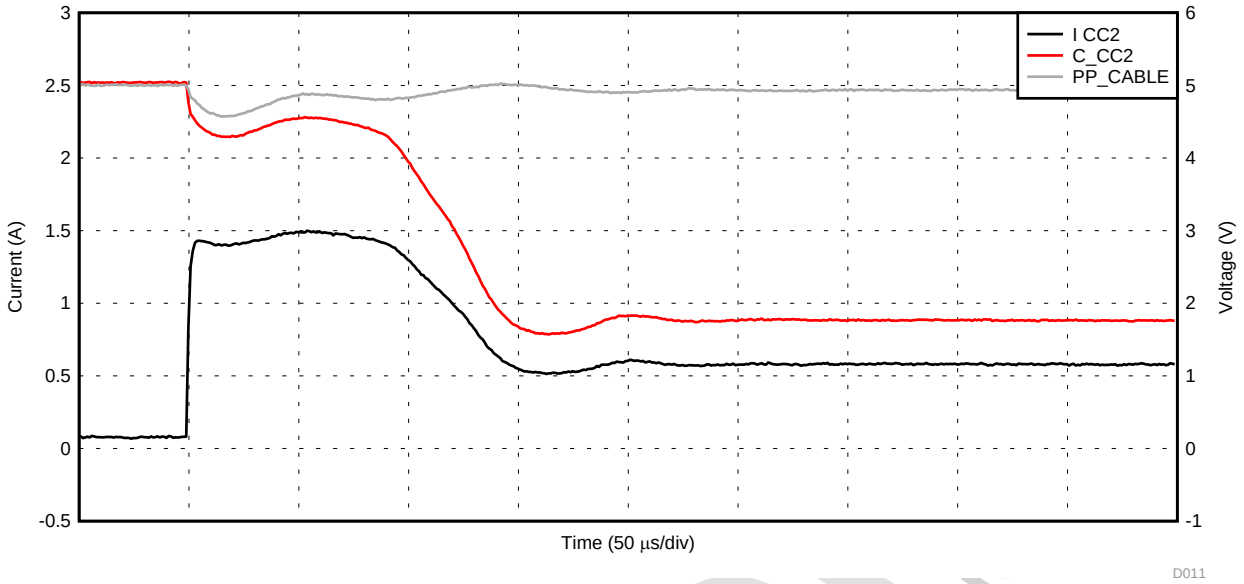


Figure 38. PP_CABLE to C_CCn Current Limit Response With a Soft Short (2 Ω)

8.3.4 USB Type-C Port-Data Multiplexer

Table 2 shows the USB Type-C receptacle pin configuration. Not all signals shown are required for all platforms or devices. The basic functionality of the pins deliver USB 2.0 (D+ and D–) and USB 3.1 (TX and RX pairs) data buses, USB power (VBUS) and ground (GND). The configuration channel signals (CC1 and CC2), and two *reserved for future use* (SBU) signal pins. The data bus pins (top and bottom D+/D– and the SBU pins) are available to be used in non-USB applications as an Alternate Mode (for example, DisplayPort, Thunderbolt™, and others).

Table 2. USB Type-C Receptacle Pin Configuration

A1	A2	A3	A4	A5	A6	A7	A8	A9	A11	A11	A12
GND	TX1+	TX1–	VBUS	CC1	D+	D–	SBU1	VBUS	RX2–	RX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1
GND	RX1+	RX1–	VBUS	SBU2	D–	D+	CC2	VBUS	TX2–	TX2+	GND

Table 3 shows the USB Type-C interface multiplexers of the SN1804044ZBHR device. The outputs are determined based on detected cable orientation as well as the identified interface that is connected to the port. Two USB output ports are present which may or may not be passing USB data. When an Alternate Mode is connected, these same ports can also pass that data (such as DisplayPort or Thunderbolt).

NOTE

Table 3 is the SN1804044ZBHR pin-to-receptacle mapping. The high-speed RX and TX pairs are not mapped through the SN1804044ZBHR device because this places extra resistance and stubs on the high-speed lines and degrade signal performance.

Table 3. SN1804044ZBHR to USB Type-C Receptacle Mapping

DEVICE PIN	Type-C RECEPTACLE PIN
VBUS	VBUS (A4, A9, B4, B9)
C_CC1	CC1 (A5)
C_CC2	CC2 (B5)
C_USB_TP	D+ (A6)
C_USB_TN	D– (A7)
C_USB_BP	D+ (B6)
C_USB_BN	D– (B7)
C_SBU1	SBU1 (A8)
C_SBU2	SBU2 (B8)

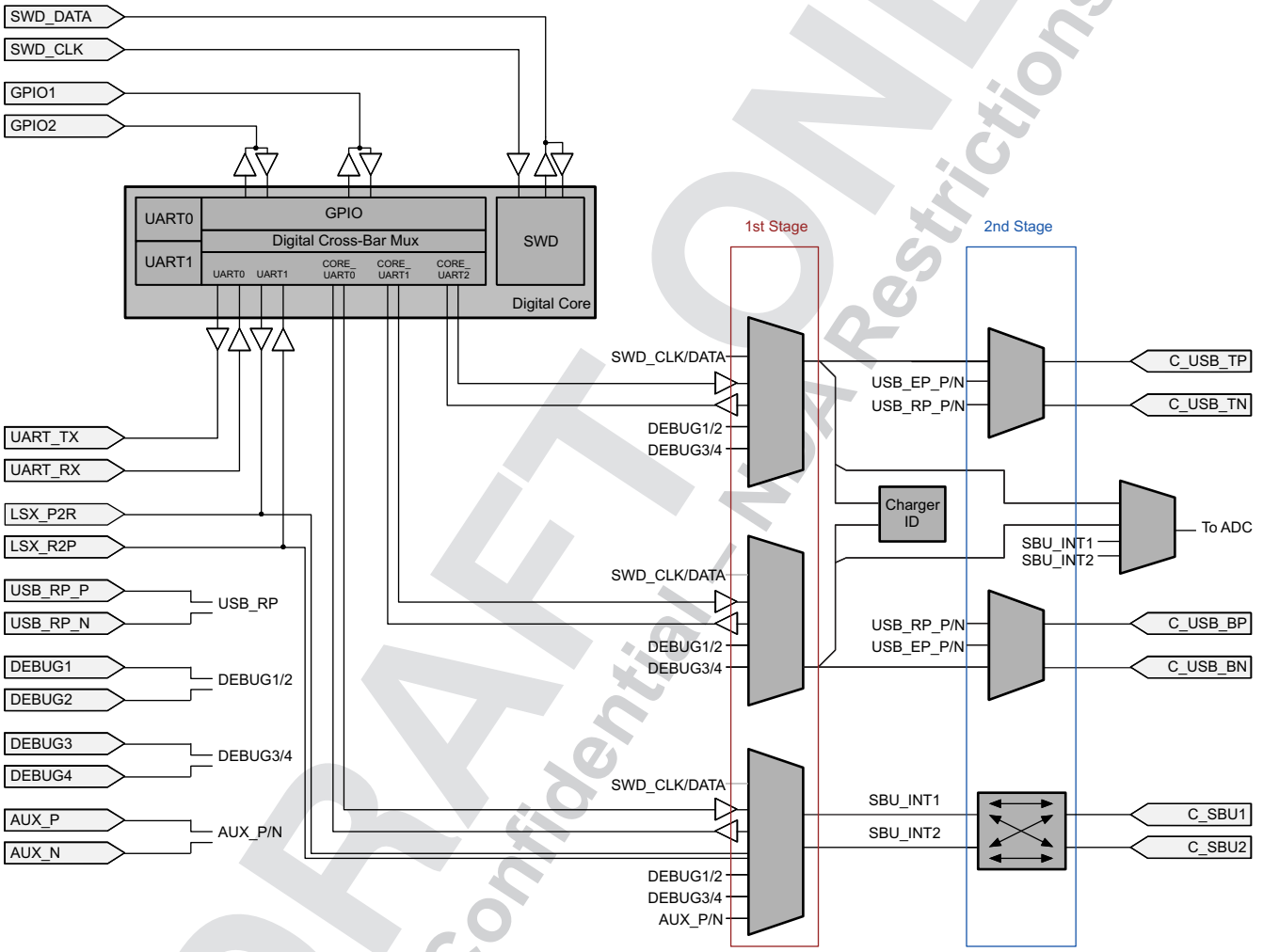


Figure 39. Port-Data Multiplexers

Table 4 shows the typical signal types through the switch path. The UART_RX/TX and LSX_P2R/R2P paths are digitally buffered to allow tri-state control for these paths. All other switches are analog pass switches. The LSX_P2R/R2P pair is also configurable to be analog pass switches. These switch paths are not limited to the specified signal type. For the signals that interface with the digital core, the maximum data rate is dictated by the clock rate at which the core is running.

Table 4. Typical Signals through Analog Switch Path

INPUT PATH	SIGNAL TYPE	SIGNAL FUNCTION
SWD_DATA/CLK	Single ended	Data, clock
UART_RX/TX	Single ended TX or Rx	UART
LSX_P2R/R2P	Single Ended TX or Rx	UART
DEBUG1/2/3/4	Single ended	Debug
AUX_P/N	Differential	DisplayPort and Thunderbolt AUX channel
USB_EP_P/N	Differential	USB 2.0 low-speed endpoint
USB_RP_P/N	Differential	USB 2.0 high-speed data-root port

8.3.4.1 USB Top and Bottom Ports

The top (C_USB_TP and C_USB_TN) and bottom (C_USB_BP and C_USB_BN) ports that correspond to the Type-C top and bottom USB D+/D– pairs are swapped based on the detected cable orientation. The symmetric pin order shown in Table 2 from the A-side to the B-side allows the pins to connect to equivalent pins on the opposite side when the cable orientation is reversed.

8.3.4.2 Multiplexer Connection Orientation

Table 5 shows the multiplexer connection orientation. For the USB D+/D– pair top and bottom port connections, these connections are fixed. For the SBU port connections, the SBU crossbar multiplexer enables flipping of the signal pair and the connections shown are for the upside-up orientation. The CORE_UARTn connections come from a digital crossbar multiplexer that allows the UART_RX/TX, LSX_P2R/R2P, and GPIO1/2 to be mapped to any of the 1st stage multiplexers.

Table 5. Data Multiplexer Connections

SYSTEM PIN	USB TOP PIN	USB BOTTOM PIN	SBU MULTIPLEXER PIN
USB_RP_P	C_USB_TP	C_USB_BP	
USB_RP_N	C_USB_TN	C_USB_BN	
USB_EP_P	C_USB_TP	C_USB_BP	
USB_EP_N	C_USB_TN	C_USB_BN	
SWD_CLK	C_USB_TP	C_USB_BP	SBU1
SWD_DATA	C_USB_TN	C_USB_BN	SBU2
DEBUG1	C_USB_TP	C_USB_BP	SBU1
DEBUG2	C_USB_TN	C_USB_BN	SBU2
DEBUG3	C_USB_TP	C_USB_BP	SBU1
DEBUG4	C_USB_TN	C_USB_BN	SBU2
AUX_P	C_USB_TP	C_USB_BP	SBU1
AUX_N	C_USB_TN	C_USB_BN	SBU2
LSX_R2P			SBU1
LSX_P2R			SBU2
CORE_UART0_TX	C_USB_TP		
CORE_UART0_RX	C_USB_TN		
CORE_UART1_TX		C_USB_BP	
CORE_UART1_RX		C_USB_BN	
CORE_UART2_TX			SBU1
CORE_UART2_RX			SBU2

8.3.4.3 Digital Crossbar Multiplexer

The SN1804044ZBHR UART paths (UART_RX, UART_TX, LSX_P2R, or LSX_R2P) and GPIO1/2 all have digital inputs that pass through a cross-bar multiplexer inside the digital core. Each of these pins is configurable as an input or output of the cross-bar multiplexer. The digital cross-bar multiplexer then connects to the port-data multiplexers as shown in Figure 39. The connections are configurable with firmware. The default state at power-up is to connect a buffered version of UART_RX to UART_TX providing a bypass through the SN1804044ZBHR device for daisy chaining during power on reset.

8.3.4.4 SBU Crossbar Multiplexer

The SBU crossbar multiplexer provides pins (C_SBU1 and C_SBU2) for future USB functionality as well as Alternate Modes. The multiplexer swaps the output pair orientation based on the cable orientation. For more information on Alternate Modes, refer to the USB PD Specification.

8.3.4.5 Signal Monitoring and Pullup and Pulldown

The SN1804044ZBHR device has comparators that can be enabled to interrupt the core when a switching event occurs on any of the port inputs. *Port-Data Multiplexer Signal Monitoring Pullup and Pulldown Characteristics* describes the input parameters for the detection. These comparators are disconnected by the application code when these pins are not digital signals but an analog voltage.

The SN1804044ZBHR device has pullups and pulldowns between the first and second stage multiplexers of the port switch for each port output (C_SBU1/2, C_USB_TP/N, and C_USB_BP/N). Figure 40 shows the configurable pullup and pulldown resistances between each multiplexer.

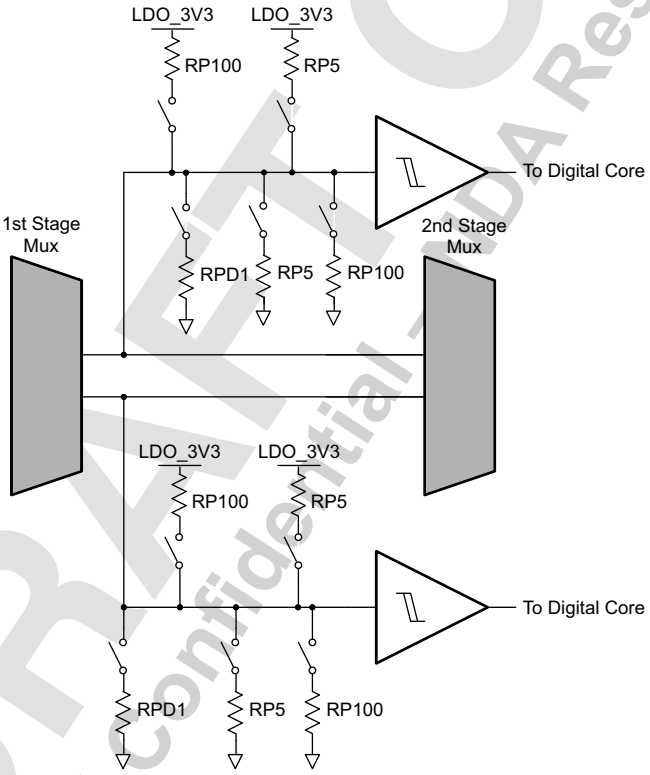


Figure 40. Port Detect and Pullup and Pulldown

8.3.4.6 Port Multiplexer Clamp

Each input to the 2nd stage multiplexer is clamped to prevent voltages on the port from exceeding the safe operating voltage of circuits attached to the system side of the port data multiplexer. Figure 41 shows the simplified clamping circuit. When a path through the 2nd stage multiplexer is closed, the clamp is connected to the one of the port pins (C_USB_TP/N, C_USB_BP/N, C_SBU1/2). When a path through the 2nd stage multiplexer is not closed, then the port pin is not clamped. As the pin voltage rises above the VCLMP_IND voltage, the clamping circuit activates, and sinks current to ground, preventing the voltage from rising further.

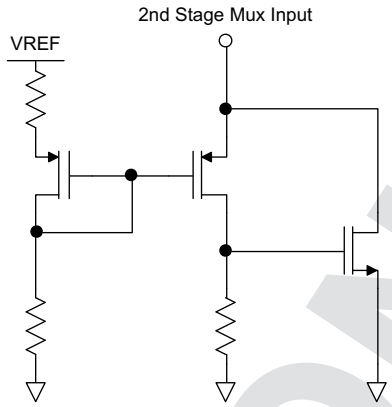


Figure 41. Port Mux Clamp

8.3.4.7 USB2.0 Low-Speed Endpoint

The USB low-speed endpoint is a USB 2.0 low-speed (1.5 Mbps) interface used to support HID class-based accesses. The SN1804044ZBHR device supports control of endpoint EP0. This endpoint enumerates to a USB 2.0 bus to provide USB-Billboard information to a host system as defined in the USB Type-C standard. EP0 is used for advertising the Billboard Class. When a host is connected to a device that provides Alternate Modes that cannot be supported by the host, the Billboard class allows a means for the host to report back to the user without any silent failures.

Figure 42 shows the physical layer of the USB endpoint. The physical layer consists of the analog transceiver, the serial interface engine, and the endpoint FIFOs. The physical layer supports low-speed operation.

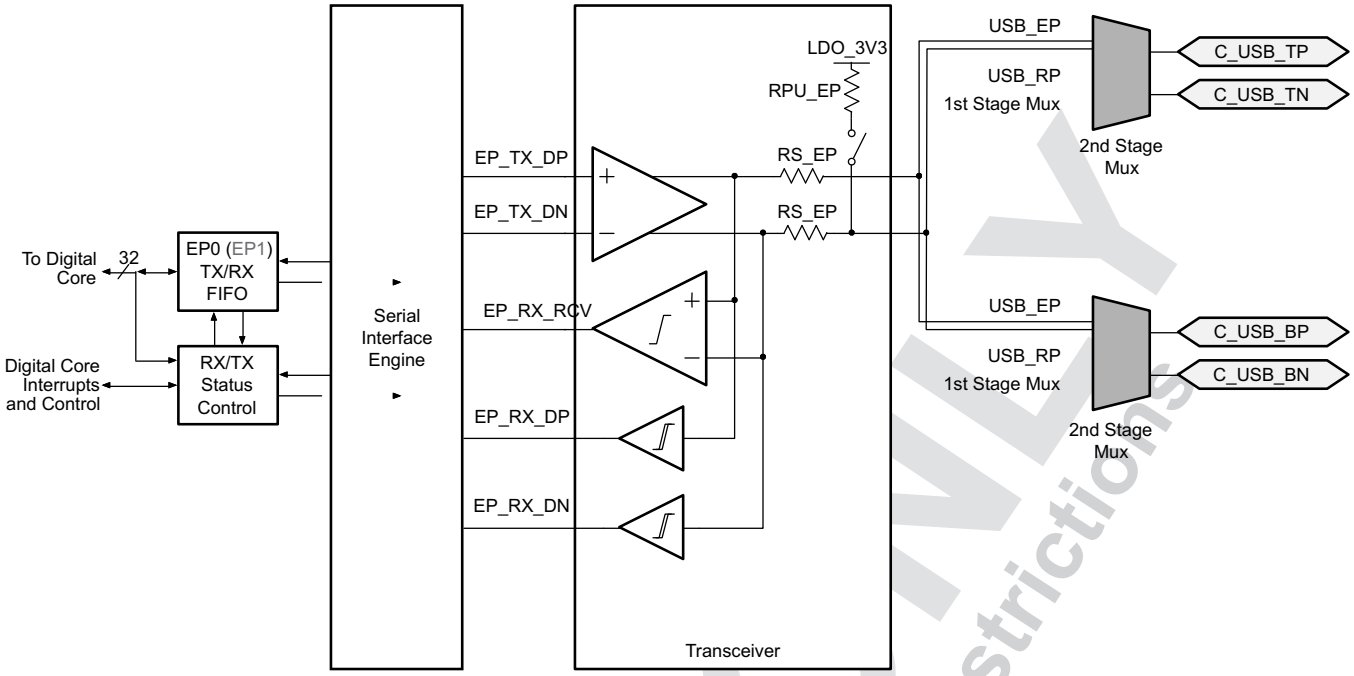


Figure 42. USB Endpoint PHY

The transceiver is made up of a fully-differential output driver, a differential to single-ended receive buffer and two single-ended receive buffers on the D+/D– independently. The output driver drives the D+/D– of the selected output of the port multiplexer. The signals pass through the 2nd-stage port-data multiplexer to the port pins. When driving, the signal is driven through a source resistance RS_EP. RS_EP is shown as a single resistor in the USB endpoint PHY but this resistance also includes the resistance of the 2nd -stage port-data multiplexer defined in the *Port-Data Multiplexer Characteristics* table. RPU_EP is disconnected during transmit mode of the transceiver.

When the endpoint is in receive mode, the resistance RPU_EP is connected to the D– pin of the top or bottom port (C_USB_TN or C_USB_BN) depending on the detected orientation of the cable. The RPU_EP resistance advertises low-speed mode only.

8.3.4.8 Battery-Charger (BC1.2) Detection Block

The battery-charger (BC1.2) detection block integrates circuitry to detect when the connected entity on the USB D+/D– pins is a charger. To enable the required detection mechanisms, the block integrates various voltage sources, currents, and resistances to the port-data multiplexers. Figure 43 shows the connections of these elements to the port-data multiplexers.

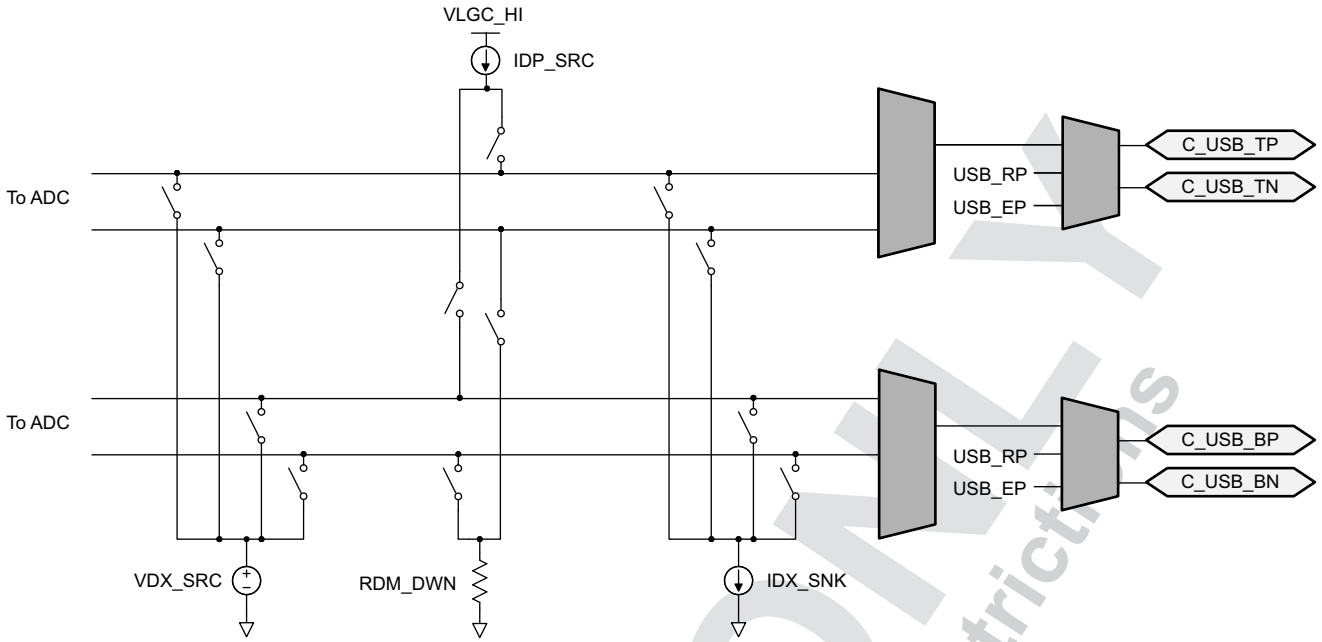


Figure 43. BC1.2 Detection Circuitry

8.3.4.9 BC1.2 Data-Contact Detect

Data-contact detect follows the definition in the USB BC1.2 specification. The detection scheme sources a current, IDP_SRC, into the D+ pin of the USB connection. The current is sourced into either the C_USB_TP (top) or C_USB_BP (bottom) D+ pin based on the determined cable or device orientation. A resistance, RDM_DWN, is connected between the D– pin and GND. Again, this resistance is connected to either the C_USB_TN (top) or C_USB_BN (bottom) D– pin based on the determined cable or device orientation. The middle section of Figure 43, the current source, IDP_SRC, and the pulldown resistance, RDM_DWN, are activated during data-contact detection.

8.3.4.10 BC1.2 Primary and Secondary Detection

The primary and secondary detection follow the USB BC1.2 specification. This detection scheme looks for a resistance between the D+ and D– lines by forcing a known voltage on the first line, forcing a current sink on the second line and then reading the voltage on the second line using the general purpose ADC integrated in the SN1804044ZBHR device. To provide complete flexibility, 12 independent switches are connected to allow firmware to force the voltage, sink current, and read voltage on any of the C_USB_TP, C_USB_TN, C_USB_BP, and C_USB_BN. The left and right sections of Figure 43, the voltage source (VDX_SRC), and the current source (IDX_SNK) are activated during primary and secondary detection.

8.3.5 Power Management

The SN1804044ZBHR power management block receives power and generates voltages to provide power to the SN1804044ZBHR internal circuitry. These generated power rails are LDO_3V3, LDO_1V8A, and LDO_1V8D. The LDO_3V3 power rail is also a low power output to load an optional external flash memory. The VOUT_3V3 power rail is a low-power output that does not power internal circuitry that is controlled by the application code and can be used to power other ICs in some applications. Figure 44 shows the power-supply path.

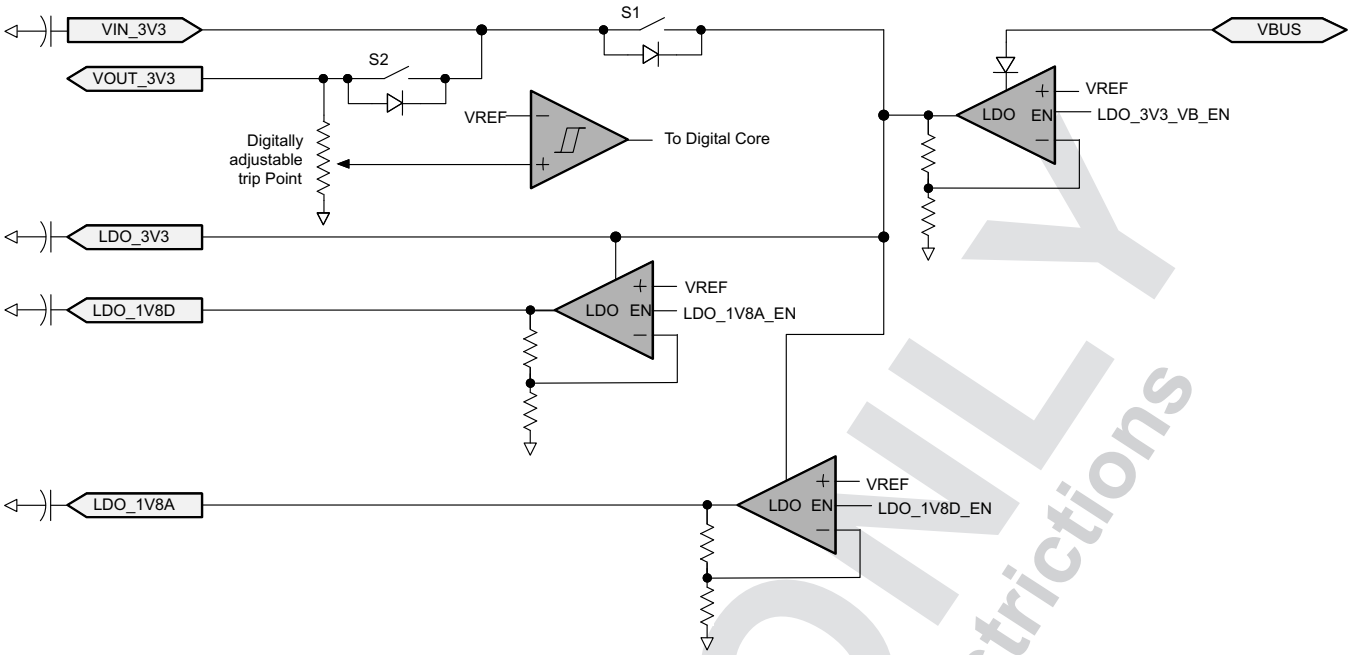


Figure 44. Power Supply Path

The SN1804044ZBHR device is powered from either VIN_3V3 or VBUS. The normal power supply input is VIN_3V3. In this mode, current flows from VIN_3V3 to LDO_3V3 to power the core 3.3-V circuitry and the 3.3-V I/Os. A second LDO steps the voltage down from LDO_3V3 to LDO_1V8D and LDO_1V8A to power the 1.8-V core digital circuitry and 1.8-V analog circuits. When VIN_3V3 power is unavailable and power is available on the VBUS, the SN1804044ZBHR device is powered from VBUS. In this mode, the voltage on VBUS is stepped down through an LDO to LDO_3V3. The S1 switch in Figure 44 is unidirectional and no current flows from LDO_3V3 to VIN_3V3 or VOUT_3V3. When VIN_3V3 is unavailable, this switch is an indicator that a dead-battery or no-battery condition exists.

8.3.5.1 Power-On and Supervisory Functions

A power-on-reset (POR) circuit monitors each supply. This POR allows the active circuitry to turn on only when a good supply is present. In addition to the POR and supervisory circuits for the internal supplies, a separate programmable voltage supervisor monitors the VOUT_3V3 voltage.

8.3.5.2 Supply Switch-Over

VIN_3V3 takes precedence over VBUS, meaning that when both supply voltages are present the SN1804044ZBHR device powers from VIN_3V3. See Figure 44 for a diagram showing the block for the power-supply path. A power-supply switchover occurs in one of two ways. The first way is when VBUS is present first and then VIN_3V3 becomes available. In this case, the supply automatically switches over to VIN_3V3 and brown-out prevention is verified by design. The other way is when both supplies are present and VIN_3V3 is removed and falls below 2.85 V.

8.3.5.3 RESETZ and MRESET

The VIN_3V3 voltage is connected to the VOUT_3V3 output by a single FET switch (S2 in Figure 44).

The enabling of the switch is controlled by the core digital circuitry and the conditions are programmable. A supervisor circuit monitors the voltage at VOUT_3V3 for an undervoltage condition and sets the external indicator RESETZ. The RESETZ pin is active low (low when an undervoltage condition occurs). The RESETZ output is also asserted when the MRESET input is asserted. The MRESET input is active-high by default, but is configurable to be active low. Figure 4 shows the RESETZ timing with MRESET set to active high. When VOUT_3V3 is disabled, a resistance of RPDOUT_3V3 pulls down on the pin.

8.3.6 Digital Core

Figure 45 shows a simplified block diagram of the digital core. This diagram shows the interface between the digital and analog portions of the SN1804044ZBHR device.

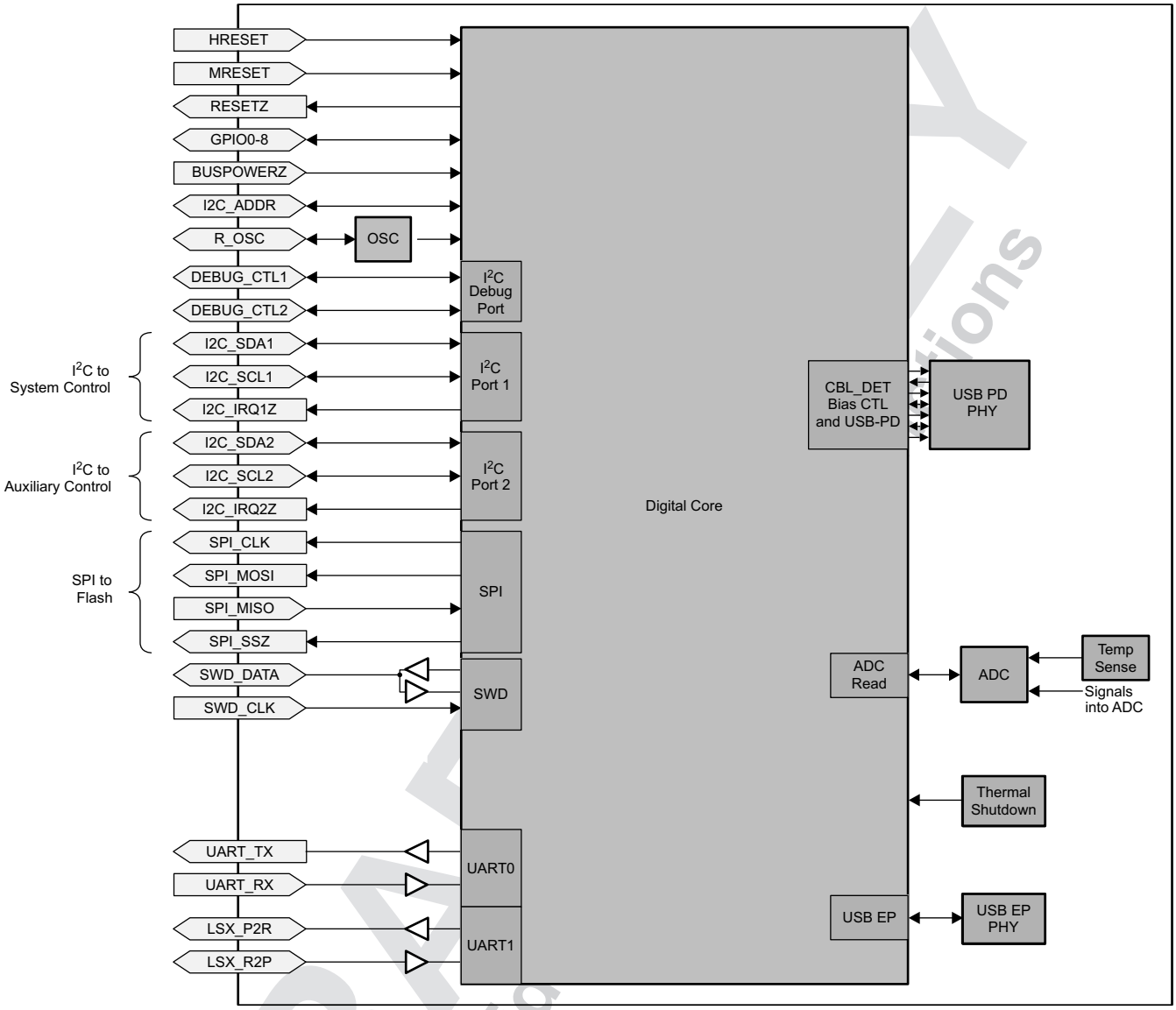


Figure 45. Digital Core Block Diagram

8.3.7 Memory Map

The device contains ROM, SRAM, and OTP memory regions as defined in Table 6:

Table 6. Memory Map

MEMORY TYPE	Size	START ADDRESS	END ADDRESS	USAGE
ROM	92KB	1000_0000h	1001_6FFFh	Application and boot
SRAM	16KB	2000_0000h	2000_3FFFh	Data, stack, scratch, and patch(1)
OTP	128B (1024 bits)	1001_8000h	1001_807Fh	Factory and user

(1) Assumes 8 KB is available for ROM patch (Address locations 2000_0000h through 2000_1FFFh).

8.3.8 USB-PD BMC Modem Interface

The USB-PD BMC modem interface is a fully USB-PD compliant Type-C interface. The modem contains the BMC encoder, BMC decoder, the TX/Rx FIFOs, and the packet engine for construction and deconstruction of the USB-PD packet. This module contains programmable SOP values and processes all SOP headers. The modem supports PD2.0 and PD3.0 specifications.

8.3.9 System Glue Logic

The system glue-logic module performs various system interface functions such as control of the system interface for RESETZ, MRESET, and VOUT_3V3. This module supports various hardware timers for digital control of analog circuits.

8.3.10 Power Reset-Control Module (PRCM)

The PRCM implements all clock management, reset control, and sleep-mode control.

8.3.11 Interrupt Monitor

The interrupt control module handles all interrupt from the external GPIO as well as interrupts from internal analog circuits.

8.3.12 ADC Sense

The ADC sense module is a digital interface to the SAR ADC. The ADC converts various voltages and currents from the analog circuits. The ADC converts up to 11 channels from analog levels to digital signals. The ADC can be programmed to convert a single sampled value.

8.3.13 UART

Two digital UARTs are provided for serial communication. The inputs to the UART are selectable by a programmable digital-crossbar multiplexer. The UART can act as pass-through between the system and the Type-C port or can filter through the digital core. The UART_RX/TX pins are typically used to daisy chain multiple SN1804044ZBHR devices in series to share code patch and configurations at startup.

8.3.14 I^2C Slave

Two I^2C interfaces provide interface to the digital core from the system. These interfaces are master and slave configurable and support low-speed and full-speed signaling. See the *I^2C Slave Interface* section for more information.

8.3.15 SPI Master

The SPI master provides a serial interface to an optional, external flash memory. The optional flash memory can be used to store code patches and or device configurations. The recommended memory is the W25X05CL (64 KB) serial-flash memory. A memory of at least (24 KB) is required for the SN1804044ZBHR device (shared or unshared) if device configuration and patch memory features are used. See the*SPI Master Interface* section for more information.

8.3.16 Single-Wire Debugger Interface

The SWD interface provides a mechanism to directly master the digital core.

8.3.17 DisplayPort HPD Timers

To enable DisplayPort HPD signaling through PD messaging, two GPIO pins (GPIO4, GPIO5) are used as the HPD input and output. When events occur on this pins during a DisplayPort connection through the Type-C connector (configured in firmware), hardware timers trigger and interrupt the digital core to indicate the required PD messaging. Table 7 shows each I/O function when GPIO4/5 are configured in HPD mode. When HPD is not enabled through firmware, both GPIO4 and GPIO5 remain generic GPIOs and can be programmed for other functions (seeFigure 46 and Figure 47).

Table 7. HPD GPIO Configuration

HPD (BINARY) CONFIGURATION	GPIO4	GPIO5
00	HPD TX	Generic GPIO
01	HPD RX	Generic GPIO
10	HPD TX	HPD RX
11	HPD TX/RX (bidirectional)	Generic GPIO

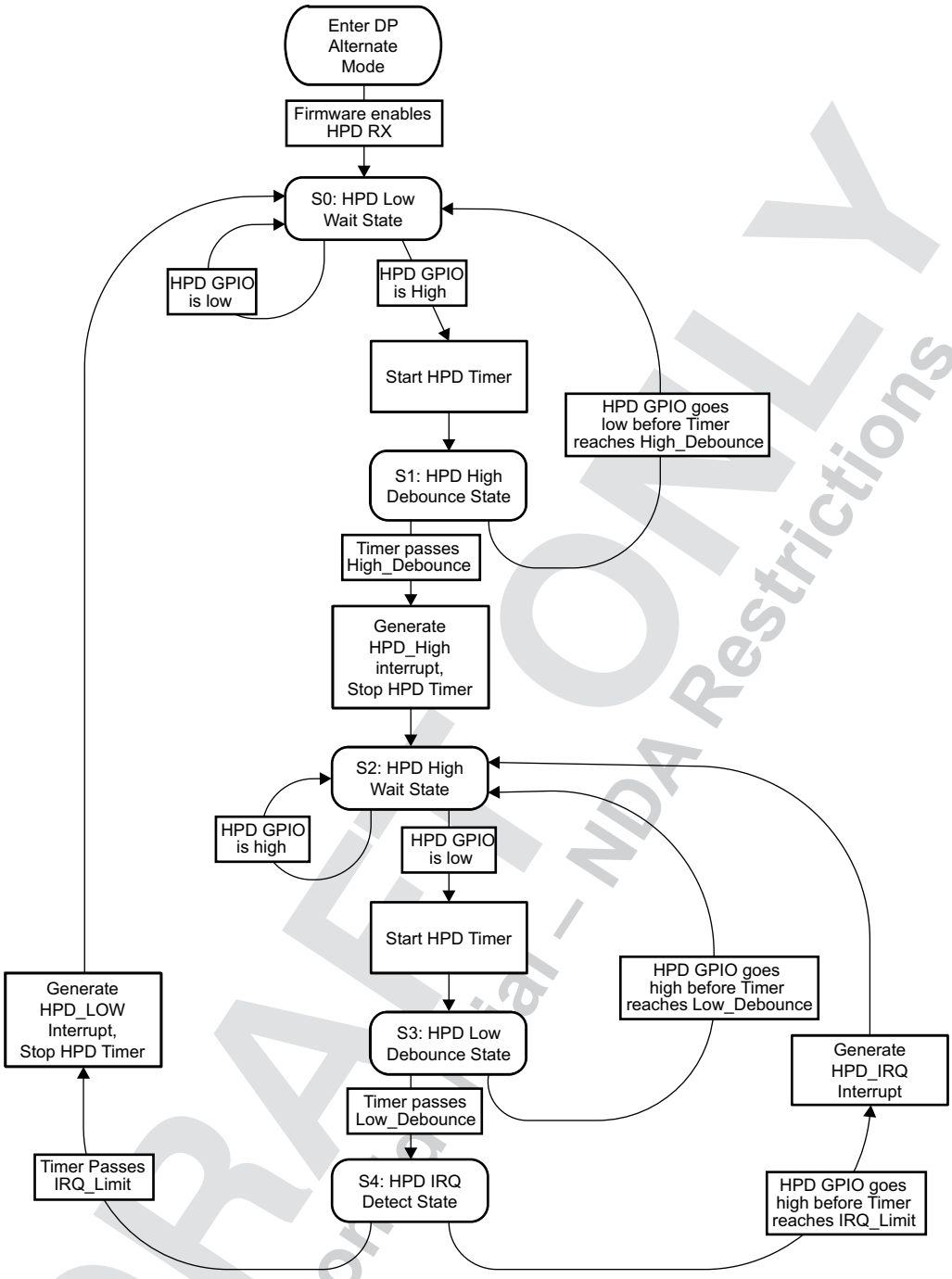


Figure 46. HPD RX Flow

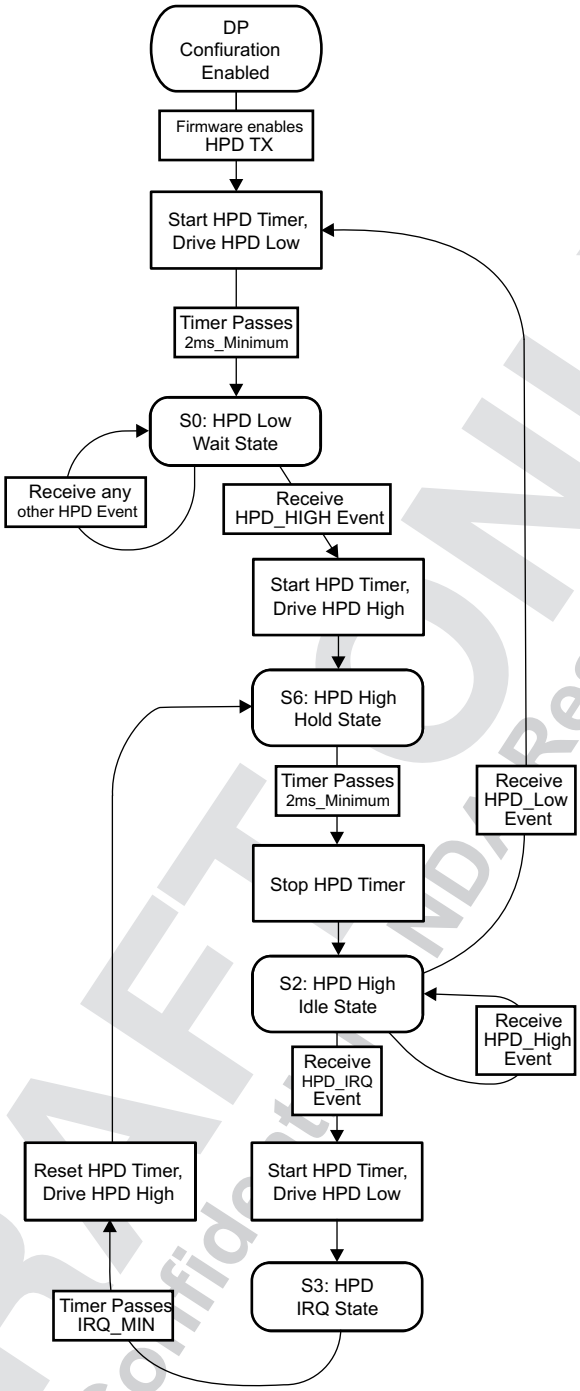


Figure 47. HPD TX Flow Diagram

8.3.18 ADC

Figure 48 shows the SN1804044ZBHR ADC. The ADC is a 10-bit successive-approximation ADC. The input to the ADC is an analog input multiplexer that supports multiple inputs from various voltages and currents in the device. The output from the ADC is available to be read and used by application firmware. Each supply voltage into the SN1804044ZBHR device is available to be converted including the port-power path inputs and outputs. All GPIO, the C_CCn pins, the charger-detection voltages are also available for conversion. To read the port-power path current sourced to VBUS, the high-voltage and low-voltage power paths are sensed and converted to voltages to be read by the ADC. For the external FET path, the difference in the SENSEP and SENSEN voltages is converted to detect the current (I_PP_EXT) that is sourced through this path.

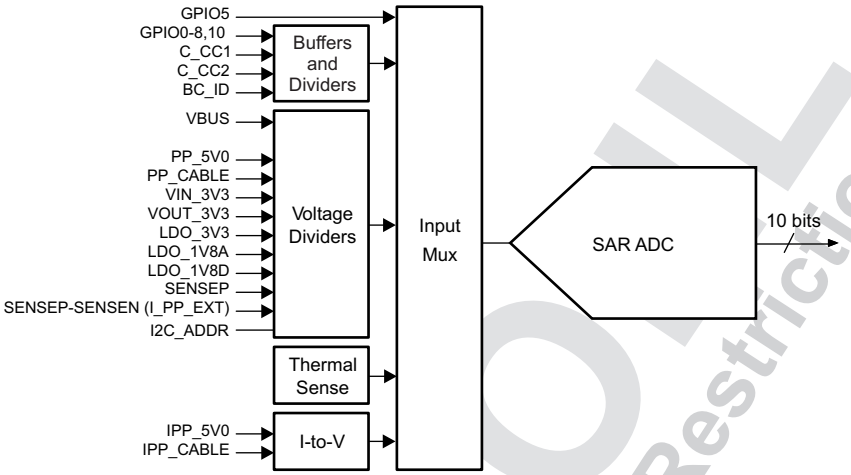


Figure 48. SAR ADC

8.3.18.1 ADC Divider Ratios

The ADC voltage inputs are each divided down to the full-scale input of 1.2 V. The ADC current-sensing elements are not divided.

Table 8 lists the divider ratios for each ADC input. Table 8 also lists which inputs are auto-sequenced in the *round-robin* automatic-readout mode. The C_CC1 and C_CC2 pin voltages each have two conversions values. The divide-by-5 (CCn_BY5) conversion is intended for use when the C_CCn pin is configured as VCONN output and the divide-by-2 (CCn_BY2) conversion is intended for use when C_CCn pin is configured as the CC data pin.

Table 8. ADC Divider Ratios

CHANNEL NO.	SIGNAL	TYPE	AUTO-SEQUENCED	DIVIDER RATIO	BUFFERED
0	Thermal sense	Temperature	Yes	N/A	No
1	VBUS	Voltage	Yes	25	No
2	SENSEP	Voltage	Yes	25	No
3	IPP_EXT	Current	Yes	N/A	No
4	Reserved	Voltage	Yes	25	No
5	Reserved	Current	Yes	N/A	No
6	PP_5V0	Voltage	Yes	5	No
7	IPP_5V0	Current	Yes	N/A	No
8	CC1_BY5	Voltage	Yes	5	Yes
9	IPP_CABLE	Current	Yes	N/A	No
10	CC2_BY5	Voltage	Yes	5	Yes
11	GPIO5	Voltage	No	1	No
12	CC1_BY2	Voltage	No	2	Yes
13	CC2_BY2	Voltage	No	2	Yes
14	PP_CABLE	Voltage	No	5	No

Table 8. ADC Divider Ratios (continued)

CHANNEL NO.	SIGNAL	TYPE	AUTO-SEQUENCED	DIVIDER RATIO	BUFFERED
15	VIN_3V3	Voltage	No	3	No
16	VOUT_3V3	Voltage	No	3	No
17	BC_ID_SBU	Voltage	No	3	Yes
18	LDO_1V8A	Voltage	No	2	No
19	LDO_1V8D	Voltage	No	2	No
20	LDO_3V3	Voltage	No	3	No
21	I2C_ADDR	Voltage	No	3	Yes
22	GPIO0	Voltage	No	3	Yes
23	GPIO1	Voltage	No	3	Yes
24	GPIO2	Voltage	No	3	Yes
25	GPIO3	Voltage	No	3	Yes
26	GPIO4	Voltage	No	3	Yes
27	GPIO5	Voltage	No	3	Yes
28	GPIO6	Voltage	No	3	Yes
29	GPIO7	Voltage	No	3	Yes
30	GPIO8 (CONFIG)	Voltage	No	3	Yes
31	GPIO10 (BUSPOWERZ)	Voltage	No	3	Yes

8.3.18.2 ADC Operating Modes

The ADC is configured into one of three modes: single-channel readout, round-robin automatic readout, or one-time automatic readout.

8.3.18.3 Single-Channel Readout

In single-channel readout mode, the ADC reads a single channel only. When the channel is selected by firmware, a conversion takes place followed by an interrupt back to the digital core. Figure 5 shows the timing diagram for a conversion starting with an ADC enable. When the ADC is disabled and then enabled, an enable time, T_ADC_EN (programmable), must occur before sampling occurs. Sampling of the input signal then occurs for a time, T_SAMPLE (programmable), and the conversion process takes a time, T_CONVERT (12 clock cycles). After the time, T_CONVERT, the output data is available for read and an Interrupt is sent to the digital core for a time, T_INTA (2 clock cycles).

In single-channel readout mode, the ADC can be configured to continuously convert that channel. Figure 6 shows the ADC repeated conversion process. In this case, when the interrupt time has passed after a conversion, a new sample and conversion occurs.

8.3.18.4 Round-Robin Automatic Readout

When this mode is enabled, the ADC state machine reads from channel 0 to channel 11 and place the converted data into registers. The host interface can request to read from the registers at any time. During round-robin automatic readout, the channel averaging must be set to 1 sample.

When the SN1804044ZBHR device runs a round-robin readout, approximately 696 µs (11 channels × 63.33 µs conversion) must pass to fully convert all channels. Because the conversion is continuous, when a channel is converted, it overwrites the previous result. Therefore, when all channels are read, any given value can be 649 µs out of sync with any other value.

8.3.18.5 One-Time Automatic Readout

The one-time automatic-readout mode is identical to the round-robin automatic readout except the conversion process halts after the final channel is converted. When all 11 channels are converted, an interrupt occurs to the digital core.

8.3.18.6 ADC Equations

ADC conversion values can be used to compute the measured voltage, current, or temperature. Use Equation 4, Equation 5, and Equation 6 to convert the ADC result.

$$T = \frac{1.2\ V \times ADC\_CODE_{dec} + 0.6 - THERM\_V0}{\frac{THERM\_GAIN}{1000}} \quad (4)$$

where

- T is the temperature (°C).
- ADC_CODEdec is the ADC value in decimal.
- THERM_V0 is the zero degree voltage (V).
- THERM_GAIN is the thermal slope (mV/°C).

$$V = \frac{1.2\ V}{1023} \times ADC\_CODE_{dec} \times DIVIDER\_RATIO \quad (5)$$

where

- V is the voltage (V).

$$I = \frac{1.2\ V}{1023} \times ADC\_CODE_{dec} \times IX\_ACC \quad (6)$$

where

- I is the current (A).
- IX_ACC is the current-sense multiplier (IPP5V_ACC, IHVEXT_ACC, or IPPCBL_ACC) [A/V].

8.3.19 I/O Buffers

Table 9 lists the I/O buffer types and descriptions. Table 10 lists the pin to I/O buffer mapping for cross-referencing the particular I/O structure of a pin. The following sections show a simplified version of the architecture of each I/O buffer type.

Table 9. I/O Buffer Type Description

BUFFER TYPE	DESCRIPTION
IOBUF_GPIOHSSWD	General-purpose high-speed I/O
IOBUF_GPIOHSSPI	General-purpose high-speed I/O
IOBUF_GPIOLS	General-purpose low-speed I/O
IOBUF_GPIOLSI2C	General-purpose low-speed I/O with I^2C deglitch time
IOBUF_I2C	I^2C compliant clock and data buffers
IOBUF_OD	Open-drain output
IOBUF_UTX	Push-pull output buffer for UART
IOBUF_URX	Input buffer for UART
IOBUF_PORT	Input buffer between the 1st and 2nd stage port-data mux

Table 10. Pin to I/O Buffer Mapping

I/O GROUP/PIN	BUFFER TYPE	SUPPLY CONNECTION (DEFAULT FIRST)
DEBUG1/2/3/4	IOBUF_GPIOLS	LDO_3V3, VDDIO
DEBUG_CTL1/2	IOBUF_GPIOLSI2C	LDO_3V3, VDDIO
BUSPOWERZ	IOBUF_GPIOLS	LDO_3V3, VDDIO
GPIO0-8	IOBUF_GPIOLS	LDO_3V3, VDDIO
I2C_IRQ1/2Z	IOBUF_OD	LDO_3V3, VDDIO
I2C_SDA1/2/SCL/1/2	IOBUF_I2C	LDO_3V3, VDDIO
LSX_P2R	IOBUF_UTX	LDO_3V3, VDDIO
LSX_R2P	IOBUF_URX	LDO_3V3, VDDIO
MRESET	IOBUF_GPIOLS	LDO_3V3, VDDIO

Table 10. Pin to I/O Buffer Mapping (continued)

I/O GROUP/PIN	BUFFER TYPE	SUPPLY CONNECTION (DEFAULT FIRST)
RESETZ	IOBUF_GPIOLS	LDO_3V3, VDDIO
UART_RX	IOBUF_URX	LDO_3V3, VDDIO
UART_TX	IOBUF_UTX	LDO_3V3, VDDIO
PORT_INT	IOBUF_PORT	LDO_3V3
SPI_MOSI/MISO/CLK/SSZ	IOBUF_GPIOHSSPI	LDO_3V3
SWD_CLK/DATA	IOBUF_GPIOHSSWD	LDO_3V3

8.3.19.1 IOBUF_GPIOLS and IOBUF_GPIOLSI2C

Figure 49 shows the GPIO I/O buffer for all GPIOn pins listed in the table (GPIO0 through GPIO17). GPIOn pins can be mapped to USB Type-C, USB PD, and application-specific events to control other ICs, interrupt a host processor, or receive input from another IC. This buffer is configurable to be a push-pull output, a weak push-pull, or open drain output. When configured as an input, the signal can be a deglitched digital input or an analog input to the ADC. The push-pull output is a simple CMOS output with independent pulldown control allowing open-drain connections. The weak push-pull is also a CMOS output, but with GPIO_RPU resistance in series with the drain. The supply voltage to this buffer is configurable to be LDO_3V3 by default or VDDIO. For simplicity, the connection to VDDIO is not shown in Figure 49, but the connection to VDDIO is fail-safe and a diode is nonexistent from GPIOn to VDDIO in this configuration. The pullup and pulldown output drivers are independently controlled from the input and are enabled or disabled through application code in the digital core.

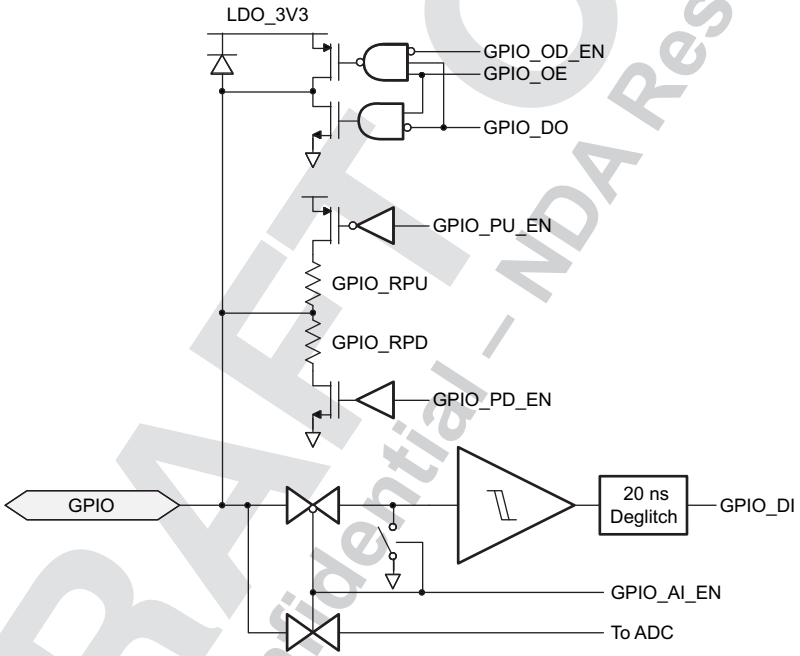


Figure 49. IOBUF_GPIOLS (General GPIO) I/O

Figure 50 shows the IOBUF_GPIOLSI2C that is identical to IOBUF_GPIOLS with an extended deglitch time.

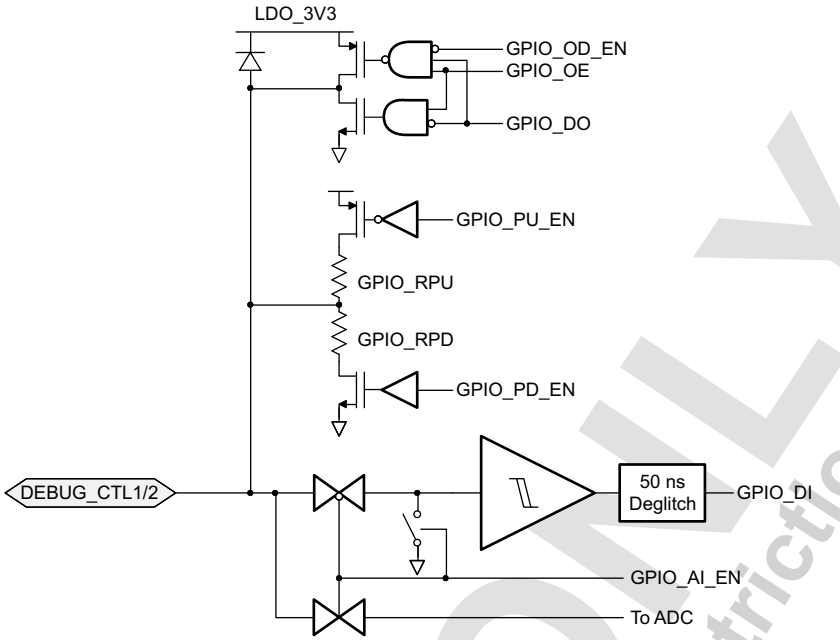


Figure 50. IOBUF_GPIOLSI2C (General GPIO) I/O with I²C Deglitch

8.3.19.2 IOBUF_OD

Figure 51 shows the open-drain output driver and is the same push-pull CMOS output driver as the GPIO buffer. The output has independent pulldown control allowing open-drain connections.

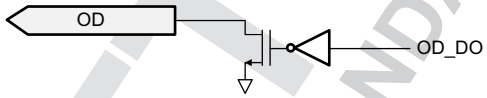


Figure 51. IOBUF_OD Output Buffer

8.3.19.3 IOBUF_UTX

Figure 52 shows the push-pull output driver. The output buffer has a UARTTX_RO source resistance. The supply voltage to the system side buffer is configurable to be LDO_3V3 by default or VDDIO, and is not shown in Figure 52. The supply voltage to the port-side buffers remains LDO_3V3.

Figure 52. IOBUF_UTX Output Buffer

8.3.19.4 IOBUF_URX

Figure 53 shows the input buffer. The supply voltage to the system side buffer is configurable to be LDO_3V3 by default or VDDIO, and is not shown in Figure 53. The supply voltage to the port-side buffers remains LDO_3V3.

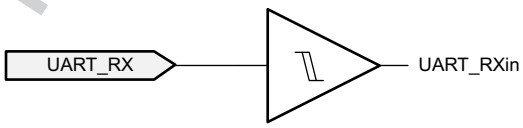


Figure 53. IOBUF_URX Input

8.3.19.5 IOBUF_PORT

Figure 54 shows the input buffer. This input buffer is connected to the intermediate nodes between the 1st stage switch and the 2nd stage switch for each port output (C_SBU1/2, C_USB_TP/N, C_USB_BN/P). The input buffer is enabled with firmware when monitoring digital signals and disabled when an analog signal is desired. See theFigure 40 section for more detail on the pullup and pulldown resistors of the intermediate node.

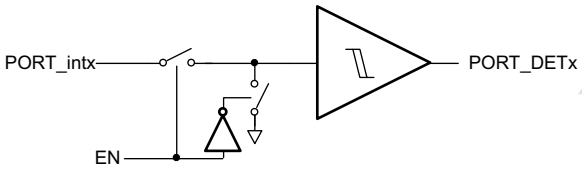


Figure 54. IOBUF_PORT Input Buffer

8.3.19.6 IOBUF_I2C

Figure 55 shows the I2C I/O driver. This I/O consists of an open-drain output and an input comparator with deglitching. The supply voltage to this buffer is configurable to be LDO_3V3 by default or VDDIO, and is not shown in Figure 55. See the *I2C Slave Characteristics* table for parameters for the I2C clock and data I/Os.

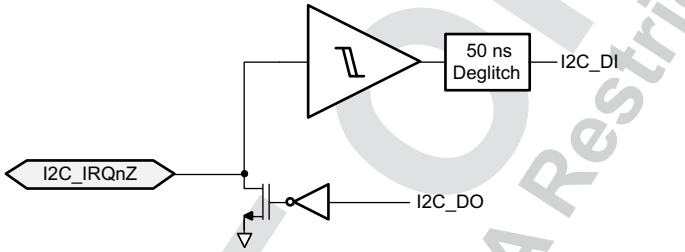


Figure 55. IOBUF_I2C I/O

8.3.19.7 IOBUF_GPIOHSPI

Figure 56 shows the I/O buffers for the SPI.

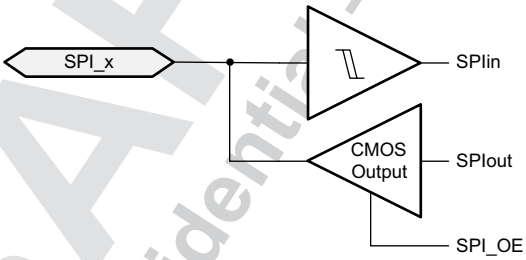


Figure 56. IOBUF_GPIOHSSPI

8.3.19.8 IOBUF_GPIOHSSWD

Figure 57 shows the I/O buffers for the SWD interface. The CLK input path is a comparator with a pullup, SWD_RPU, on the pin. The data I/O consists of an identical input structure as the CLK input but with a tri-state CMOS output driver.

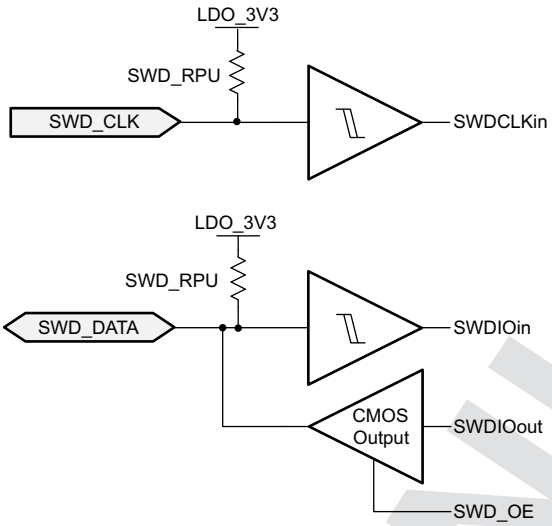


Figure 57. IOBUF_GPIOHSSWD

8.3.20 Thermal Shutdown

The SN1804044ZBHR device has both a central thermal shutdown to the chip and a local thermal shutdown for the power-path block. The central thermal shutdown monitors the temperature of the center of the die and disables all functions except for supervisory circuitry. This shutdown also halts digital core when die temperature goes above a rising temperature of TSD_MAIN. The temperature shutdown has a hysteresis of TSDH_MAIN and when the temperature falls back below this value, the device resumes normal operation. The power-path block has a local thermal-shutdown circuit to detect an overtemperature condition because of overcurrent, and quickly turns off the power switches. The power-path thermal shutdown values are TSD_PWR and TSDH_PWR. The output of the thermal shutdown circuit is deglitched by TSD_DG before triggering. The thermal shutdown circuits generate interrupt events to the digital core.

8.3.21 Oscillators

The SN1804044ZBHR device has two independent oscillators for generating internal clock domains. A 48-MHz oscillator generates clocks for the core during normal operation and clocks for the USB 2.0 endpoint physical layer. An external resistance is placed on the R_OSC pin to set the oscillator accuracy. A 100-kHz oscillator generates clocks for various timers and clocking the core during low-power states.

8.4 Device Functional Modes

8.4.1 Device Configurations and ROM Patch Code

The SN1804044ZBHR application and boot code are stored in the read only memory (ROM.) An optional external flash memory can be used for storing ROM code patches and device configurations, called a patch bundle. The flash memory can be shared with other devices in the system to reduce overall system cost. The flash memory organization shown in Figure 58..

The flash is divided into two separate regions: the low region and the high region. The size of each region is 8 KB. The two regions are used to allow updating the patch bundle in the memory without writing over the previous code which ensures that the new updated code is valid before switching to the new code. For example, if a power loss occurred while writing a new patch bundle, the original patch bundle is still in place and is used at the next boot.

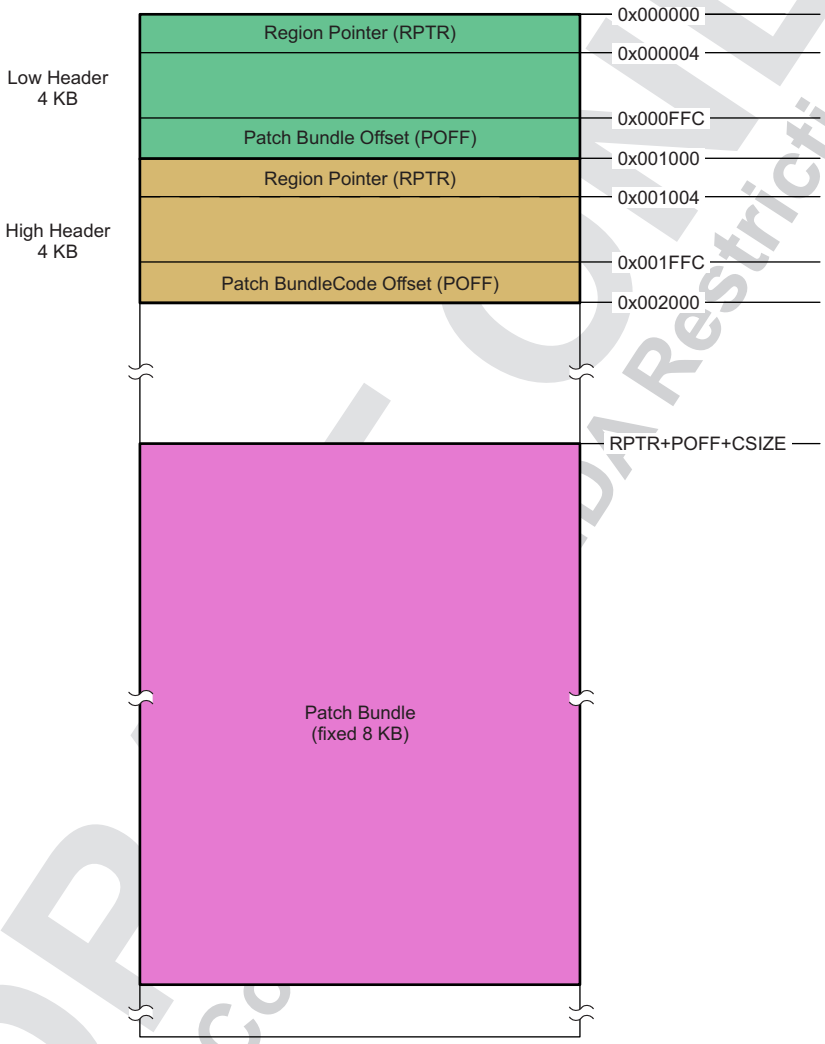


Figure 58. Patch and Configuration Flash Memory Organization

The blocks starting at address 0x000000h, have two 4-KB headers. The low-header 4-KB block is at address 0x000000h and the high-header 4-KB block is at 0x001000h. Each header contains a region pointer (RPTR) that holds the address of the physical location in memory where the low-region application code resides. Each also contains an patch code offset (POFF) that contains the physical offset inside the region where the SN1804044ZBHR configuration and patch code resides. The SN1804044ZBHR firmware physical location in the memory is RPTR + POFF. The first section contains the device configuration settings for up to four

Device Functional Modes (continued)

SN1804044ZBHR devices at 256 B each. These configurations determine each the default behavior after power-up of each device and can be customized using the TPS6598x Configuration Tool. The flash-read flow handles reading and determining whether a region is valid, and contains good patch and configuration code. The SPI flash is assumed to have 4-KB memory sectors and at least 24 KB of total memory. The W25X05CL device or similar is recommended.

8.4.2 Supported System Use Cases

The device firmware supports one primary device in the system and an optional secondary device in the system. In the case of one primary device, a single SN1804044ZBHR device resides in the system. In the case of one primary and one secondary device, two SN1804044ZBHR devices reside in the system. Both SN1804044ZBHR devices must have the same ROM verison. The primary and secondary devices are connected with a UART chain which then forms a communication path between the primary and secondary device for patch bundle updates.

The device can support a minimum of four system use cases which are defined as follows:

Case A External SPI flash is in the system, but host is not present.

Case B No external SPI flash is in the system, but host is present.

Case C External SPI flash and a host are present in the system.

Case D No external flash nor host are present in the system

8.4.2.1 Case A—External SPI Flash

Figure 59 shows use case A. In this case, no host is available in the system. A primary device and an optional secondary device are present in the system. The patch bundle resides in the external SPI flash.

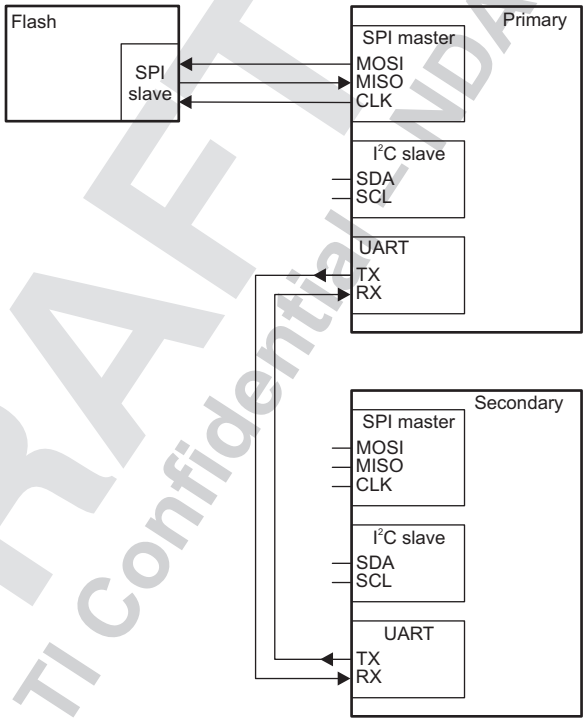


Figure 59. Use Case A

Device Functional Modes (continued)

8.4.2.2 Case B—Host Only

Figure 60 shows use case B. In this case, only a host is available in the system. A primary device and an optional secondary device are present in the system. The patch bundle resides in the host system memory and is used to update both the primary and secondary (when available) devices.

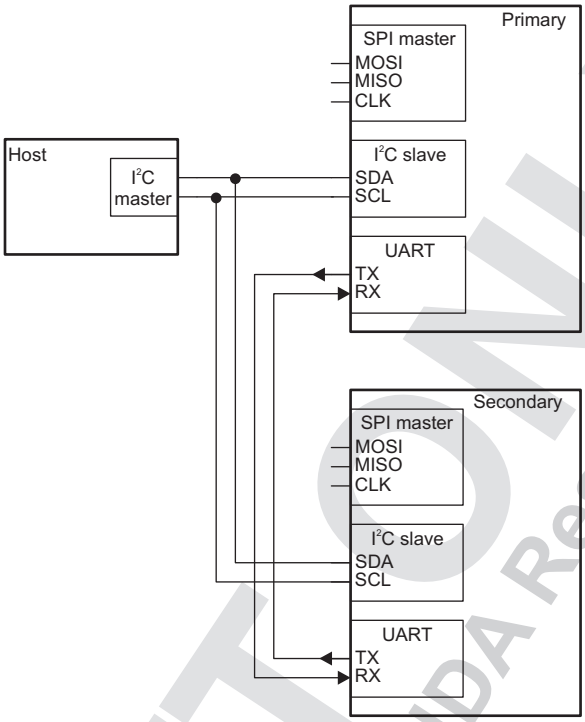


Figure 60. Use Case B

Device Functional Modes (continued)

8.4.2.3 Case C—External SPI Flash and Host Present

Figure 61 shows use case C. In this case, a host is available in the system, as well as, an external SPI flash. A primary device and an optional secondary device are present in the system. The patch bundle can reside in the external SPI flash, the host, or both.

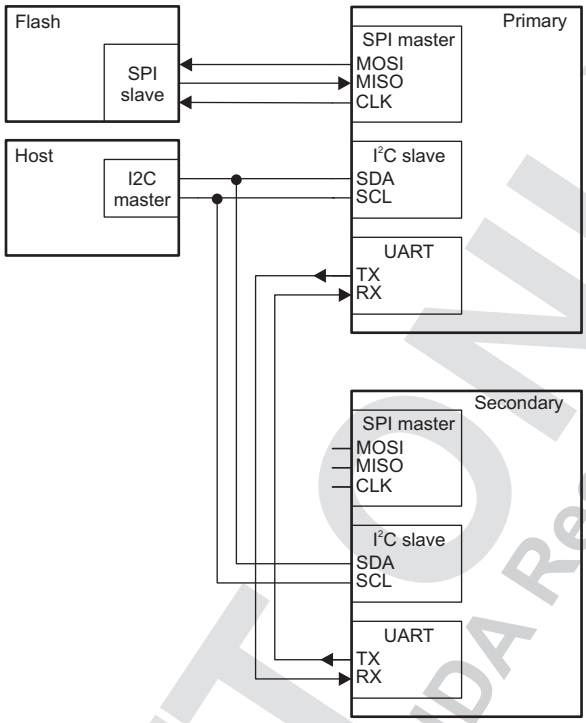


Figure 61. Use Case C

Device Functional Modes (continued)

8.4.2.4 Case D—No External Flash Nor Host

Figure 62 shows use case D. In this case, no host nor external flash is available in the system. A primary device and an optional secondary device are present in the system. Because no host or flash exists in the system, no patch bundle can be applied and both devices default to the device configurations set by the GPIO8 pin. For this case, both devices are treated independently and behave as primary devices with respect to the boot flows.

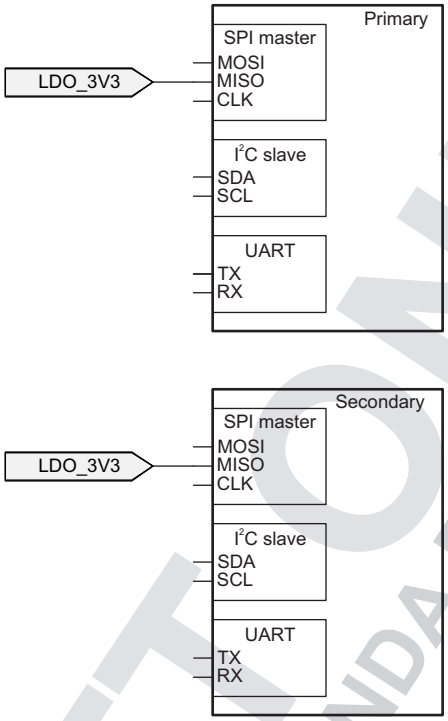


Figure 62. Use Case D

Device Functional Modes (continued)

8.4.3 Boot Flow

The SN1804044ZBHR device has a power-on-reset (POR) circuit that monitors LDO_3V3 and issues an internal reset signal. The digital core, memory banks, and peripherals receive a clock. Then a RESET interrupt is issued to the digital core, and the boot code begins execution. Figure 63 shows the SN1804044ZBHR boot code sequence. As shown, when the primary device or optional secondary device are identified, the respective boot flows as shown in Figure 64 and Figure 65.

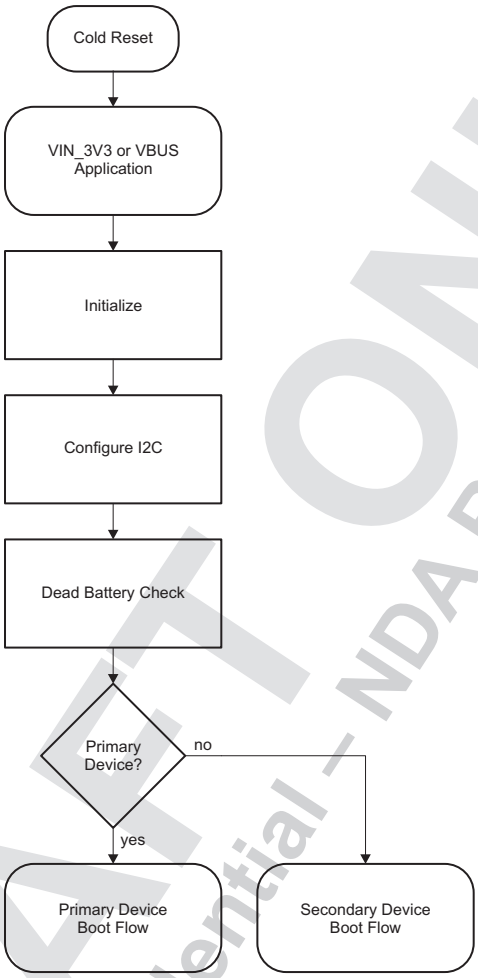


Figure 63. Flow Diagram for Boot Firmware Sequence

Device Functional Modes (continued)

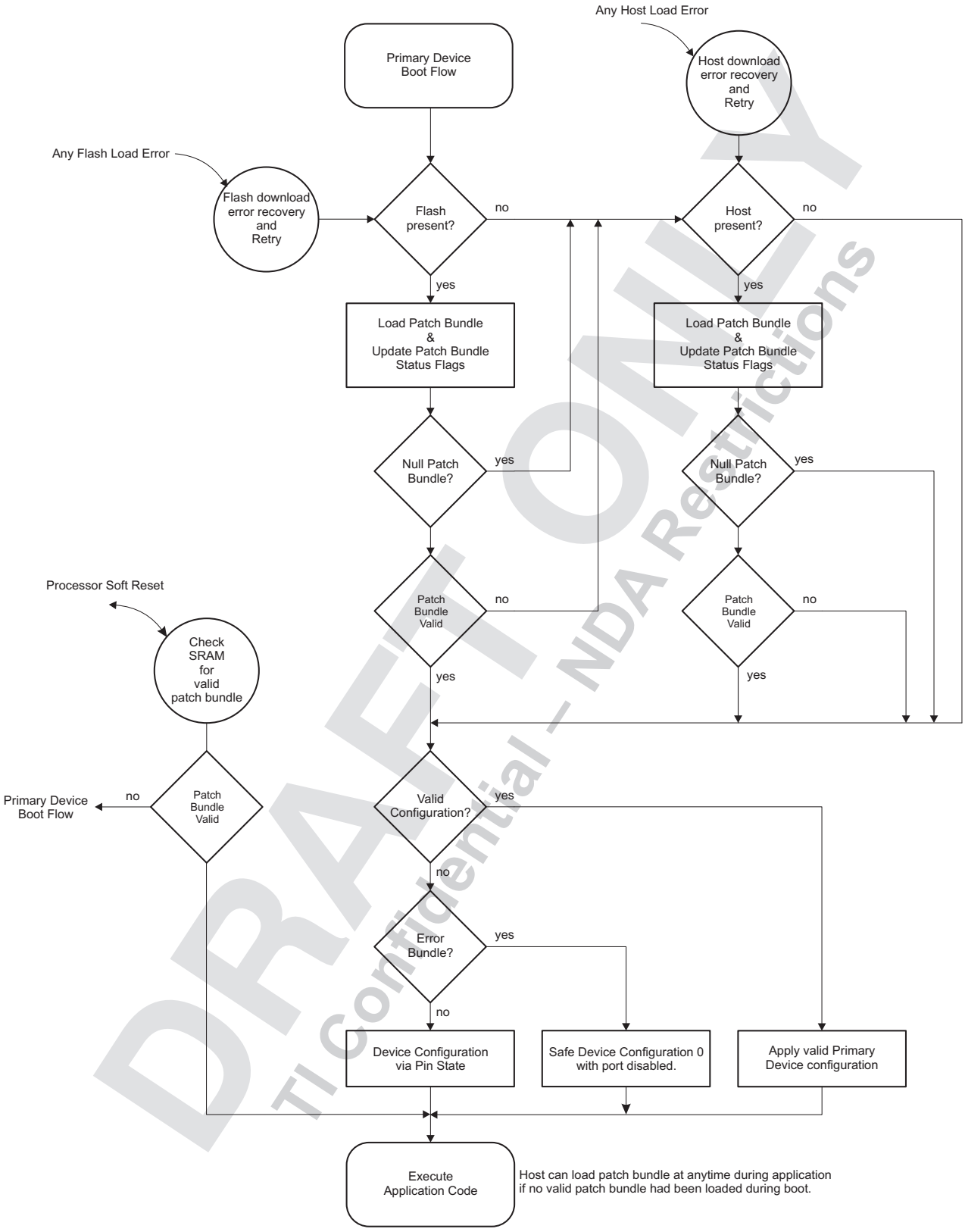


Figure 64. Primary-Device Boot Flow

Device Functional Modes (continued)

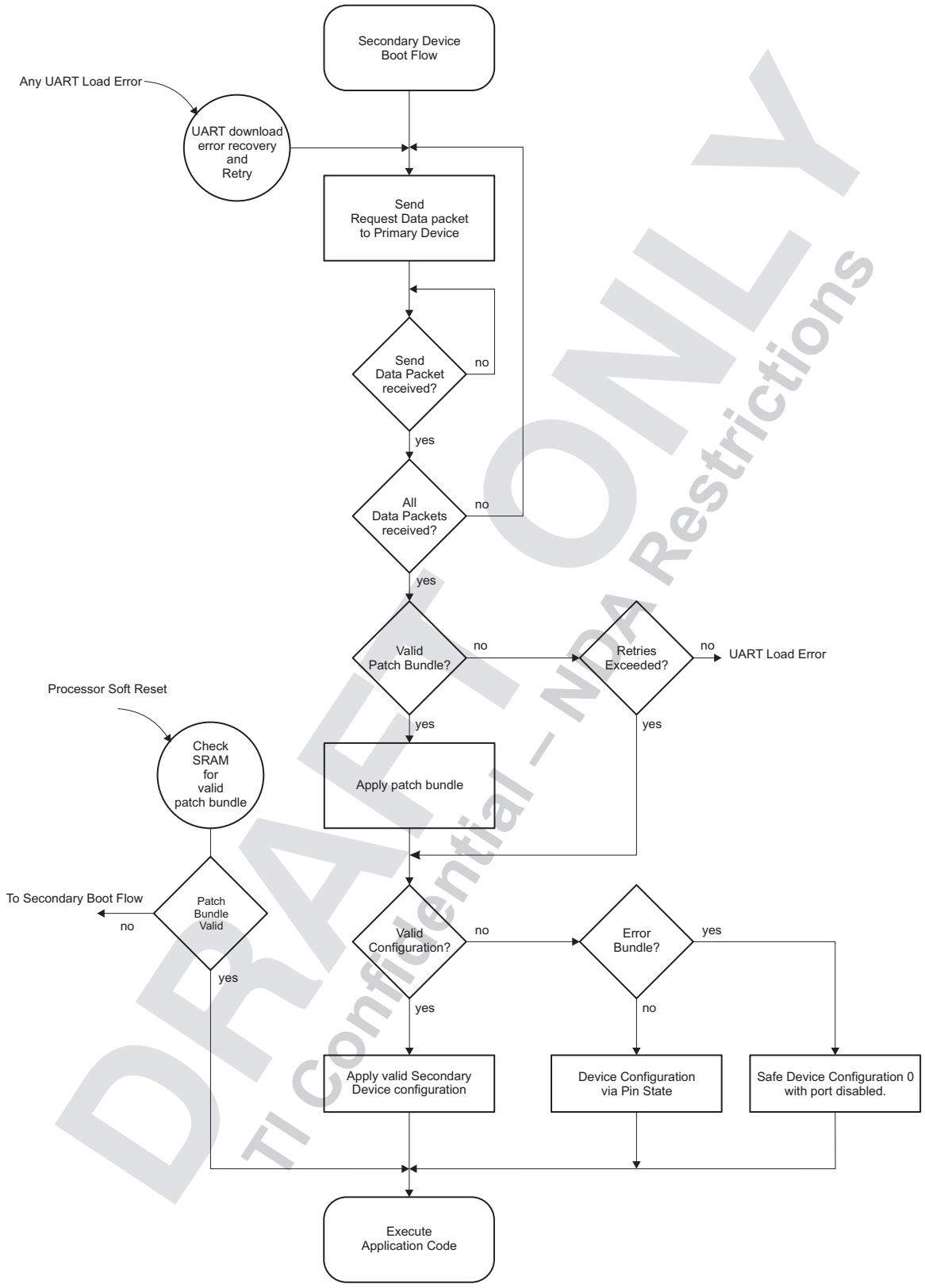


Figure 65. Secondary-Device Boot Flow

Device Functional Modes (continued)

The boot code has three primary functions:

- Device initialization
- Patch bundle download to the primary device
- Patch bundle transfer to the optional secondary device

The boot code checks the system for an available patch bundle in a sequential fashion. The boot code first checks to see if an external flash is present. If an external flash is present, the boot code checks for a valid patch bundle and, if available, the patch bundle is loaded into the SN1804044ZBHR SRAM. If no patch bundle is available, or no external flash is present, the boot code then checks for the presence of a host. If the host is present, the boot code checks for an available patch bundle, and if available, the patch bundle is loaded. If no host is present or a patch bundle is unavailable, then no patch bundle is assumed to be loaded. At this point, the device uses the application code that exists in the current ROM version. When a valid patch bundle is loaded, the boot code proceeds to the application. For example, if a valid patch bundle is found in the external flash, the boot code proceeds to the application. The only exception to this process is when the patch bundle is a null patch bundle. In this case, the boot proceeds to the next phase.

NOTE

The device also supports a boot sequence that cycles through the primary boot flow checking for an external flash followed by checking for a host. This cycle repeats indefinitely until a flash or host is found and a valid patch bundle has been successfully loaded. This mode can be selected by the factory device-configuration 7 described in the *Factory Set Device Configurations* section.

8.4.4 Initialization

During initialization, the SN1804044ZBHR device enables device internal hardware and loads the default configurations. The 48-MHz clock is enabled and the SN1804044ZBHR persistence counters begin monitoring VBUS and VIN_3V3. These counters ensure the supply powering the SN1804044ZBHR device is stable before continuing the initialization process. The initialization concludes by enabling the thermal monitoring blocks and thermal shutdown protection, along with the ADC, CRC, GPIO and NVIC blocks.

8.4.5 I²C Configuration

The SN1804044ZBHR device features dual I²C busses with configurable addresses. The I²C addresses are determined according to the flow shown in Figure 66. The address is configured by reading the device GPIO states at boot (refer to the *I²C Pin Address Setting* section for details). When the I²C addresses are established, the SN1804044ZBHR device enables a limited host interface to allow for communication with the device during the boot process.

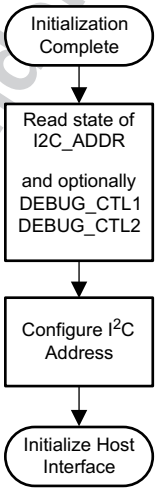


Figure 66. I²C Address Configuration

Device Functional Modes (continued)

8.4.6 Dead-Battery Condition

After I²C configuration is complete, the SN1804044ZBHR device checks VIN_3V3 to determine the cause of device boot. If the device is booting from a source other than VIN_3V3, the dead-battery flow is followed to allow for the rest of the system to receive power. The state of the BUSPOWERZ pin is read to determine power path configuration for dead-battery operation. After the power path is configured, the SN1804044ZBHR device continues through the boot process. Figure 67 shows the full dead-battery process.

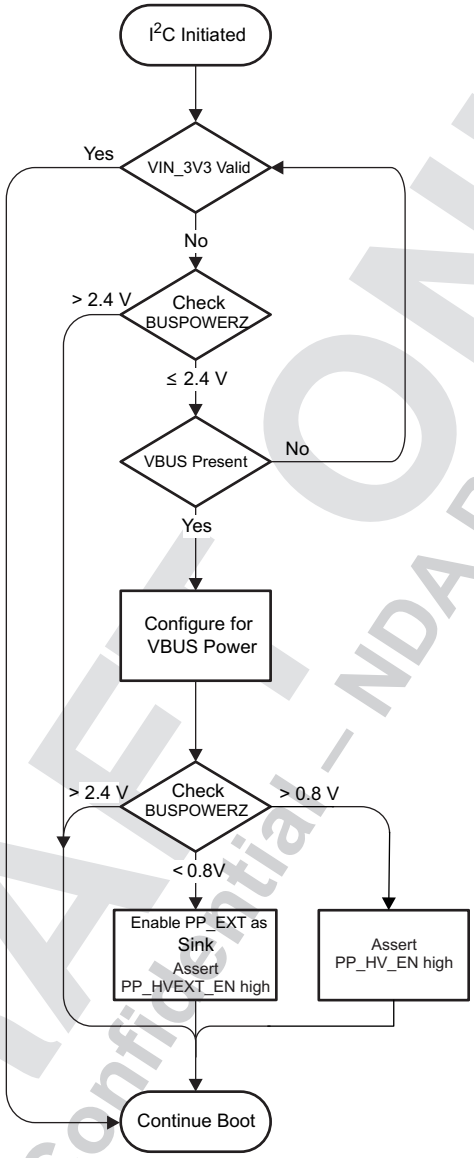


Figure 67. Dead-Battery Condition Flow Diagram

Device Functional Modes (continued)

8.4.7 Flash Memory Read

The SN1804044ZBHR device first attempts to load patch and configuration code from the low region of the optional attached flash memory. If any part of the read process yields invalid data, the SN1804044ZBHR device aborts the low-region read and attempt to read from the high region. If both regions contain invalid data the device carries out the invalid memory flow. Figure 68 shows the flash-memory read flow.

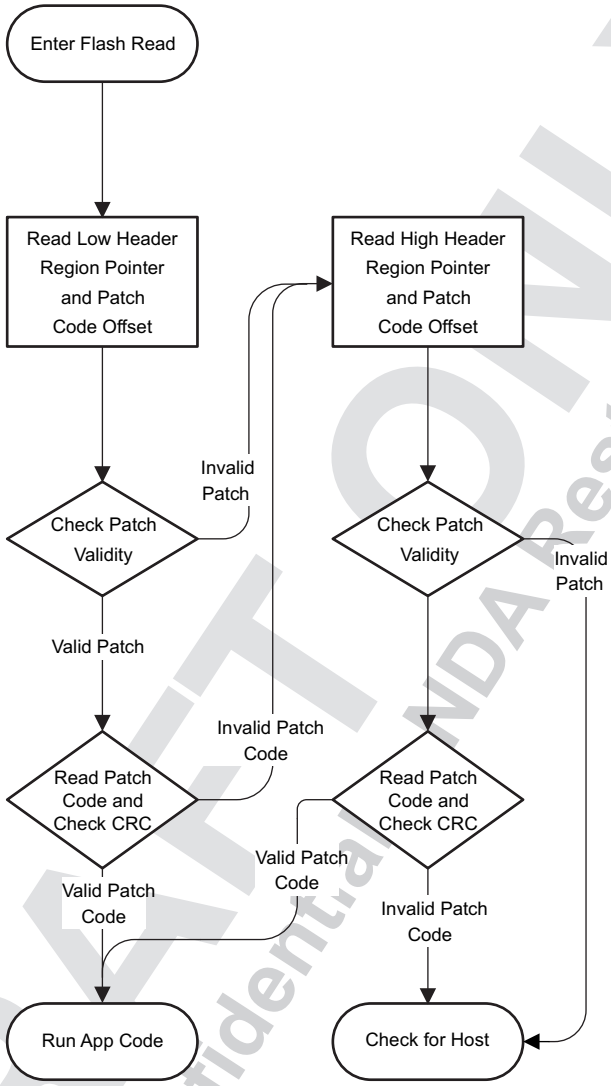


Figure 68. Flash Read Flow

Device Functional Modes (continued)

8.4.8 UART Download

The secondary SN1804044ZBHR device downloads the required application code from the primary SN1804044ZBHR device through UART. Figure 69 shows the UART download process.

Currently, the SN1804044ZBHR firmware only supports two-device (1 primary and 1 secondary) systems.

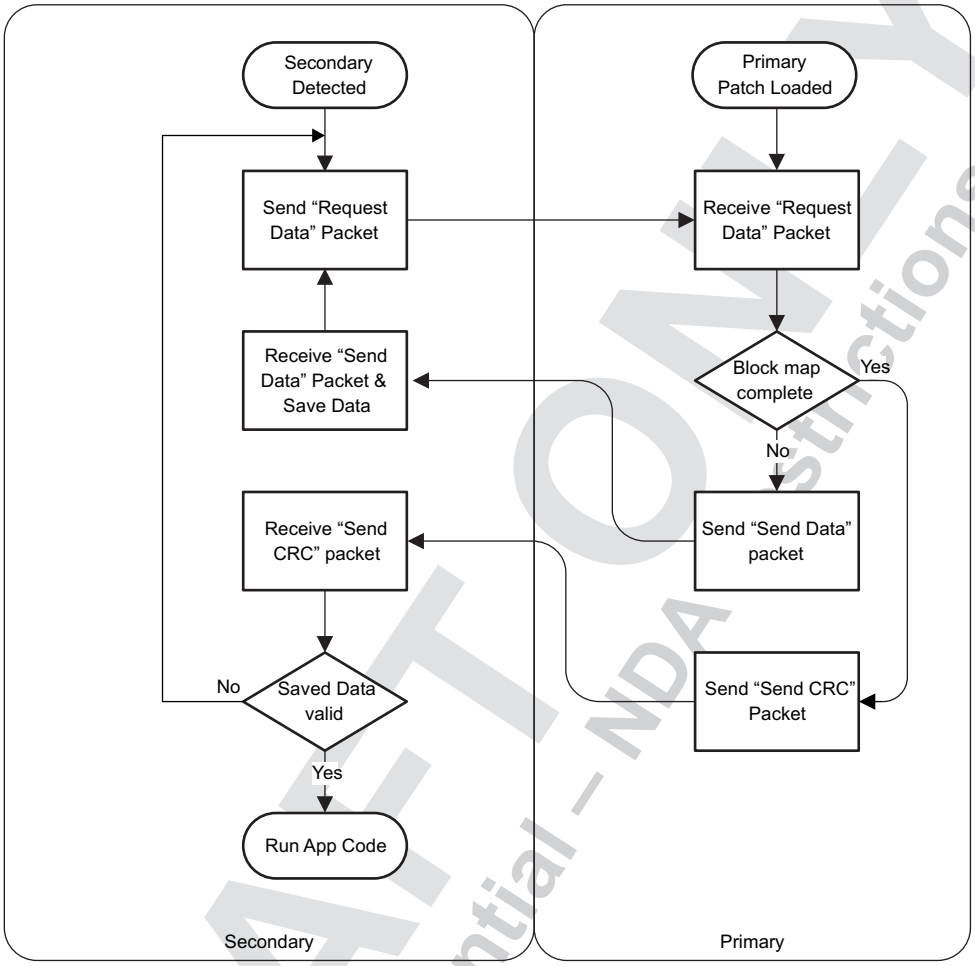


Figure 69. UART Download Process

8.5 Programming

8.5.1 Programming the Optional External Flash

8.5.1.1 SPI Master Interface

The SN1804044ZBHR device loads any ROM patch, configuration or both from flash memory during the *Boot Flow* sequence. The SPI master electrical characteristics are defined in *SPI Master Switching Characteristics* and timing characteristics are defined in Figure 8. The SN1804044ZBHR device is designed to power the flash from LDO_3V3 to support dead-battery or no-battery conditions, and therefore pullup resistors used for the flash memory must be tied to LDO_3V3. The flash memory IC must support a 12-MHz SPI clock frequency. The size of the flash must be at least 24 KB to hold the maximum ROM patch and configuration code outlined in the *Device Configurations and ROM Patch Code* section. The SPI master of the SN1804044ZBHR device supports SPI Mode 0. For Mode 0, data delay is defined such that data is output on the same cycle as the chip select (SPI_SSZ pin) becomes active. The chip select polarity is active-low. The clock phase is defined such that data (on the SPI_MISO and SPI_MOSI pins) is shifted out on the falling edge of the clock (SPI_CLK pin) and data is

Programming (continued)

sampled on the rising edge of the clock. The clock polarity for chip select is defined such that when data is not being transferred the SPI_CLK pin is held (or idling) low. The minimum erasable sector size of the flash must be 4 KB. The W25X05CL device or similar is recommended. Refer to *Host Interface Technical Reference Manual* for instructions for programming and erasing the attached flash memory over SPI using the host interface of the SN1804044ZBHR device.

8.5.1.2 I²C Slave Interface

The SN1804044ZBHR device has three I²C interface ports. I²C port 1 is comprised of the I2C_SDA1, I2C_SCL1, and I2C_IRQ1Z pins. I²C port 2 is comprised of the I2C_SDA2, I2C_SCL2, and I2C_IRQ2Z pins. These interfaces provide general-status information about the SN1804044ZBHR device and about the ability to control the SN1804044ZBHR behavior. These interfaces also provide information about connections detected at the USB-C receptacle and supporting communications to and from a connected device or cable supporting BMC USB-PD. The third port is comprised of the DEBUG_CTL1 and DEBUG_CTL2 pins. This third port is a firmware-emulated I²C master. The pins are generic GPIO and do not contain any dedicated hardware for I²C such as detecting starts, stops, acknowledges, or other protocol normally associated with I²C. This third port is always a master and has no interrupt. This port is intended to master another device that has simple control based on mode and multiplexer orientation. The DEBUG_CTL1 pin is the serial clock and the DEBUG_CTL2 pin is serial data.

The first two ports can be a master or a slave, but the default behavior is to be a slave. Port 1 and port 2 are interchangeable. Each port operates the same way and has the same access in and out of the core. An interrupt mask is set for each that determines what events are interrupted on that given port.

8.5.1.2.1 I²C Interface Description

The SN1804044ZBHR device supports standard and fast mode I²C interface. The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a supply through a pullup resistor. The data transfer can only be initiated when the bus is not busy.

A master sending a start condition (a high-to-low transition on the SDA I/O) while the SCL input is high initiates I²C communication. After the Start Condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA I/O during the high of the ACK-related clock pulse. On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period as changes in the data line at this time are interpreted as control conditions (START or STOP). The master sends a Stop Condition, a low-to-high transition on the SDA I/O while the SCL input is high.

Any number of data bytes can be transferred from the transmitter to receiver between the start and the stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges, must pull down the SDA line during the ACK clock pulse, so that the SDA line remains low during the high pulse of the ACK-related clock period. When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. The master receiver holding the SDA line high does this. In this event, the transmitter must release the data line to enable the master to generate a stop condition.

Figure 70 shows the start and stop conditions of the transfer. Figure 71 shows the SDA and SCL signals for transferring a bit. Figure 72 shows a data transfer sequence with the ACK or NACK at the last clock pulse.

Programming (continued)

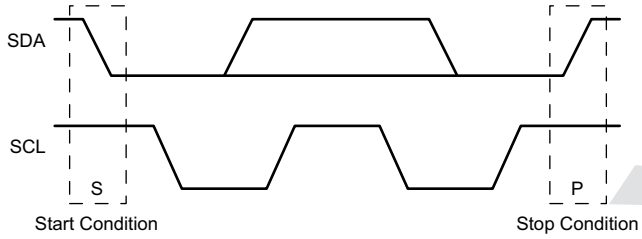


Figure 70. I²C Definition of Start and Stop Conditions

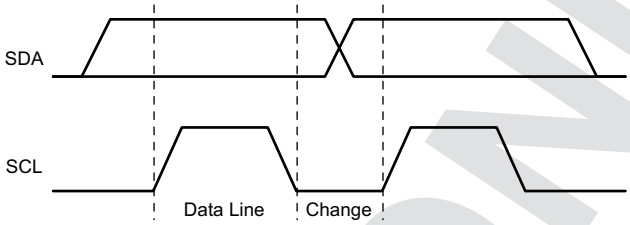


Figure 71. I²C Bit Transfer

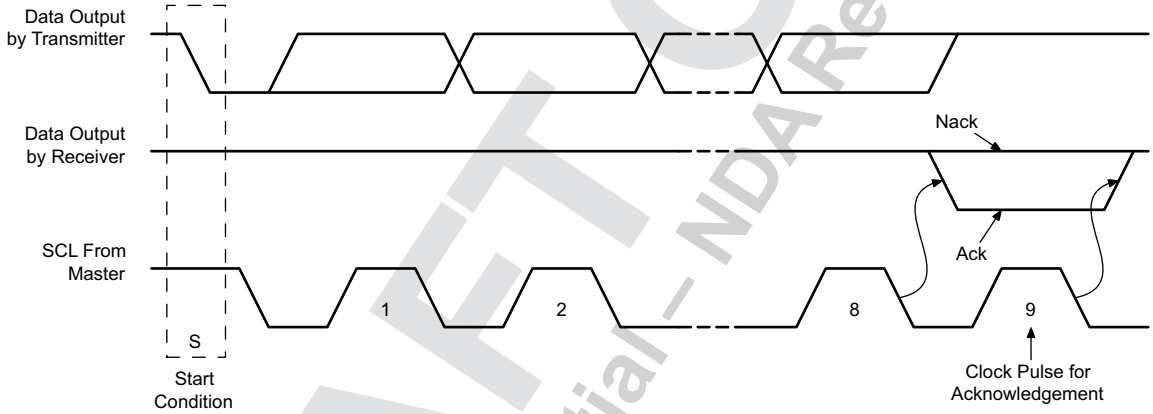


Figure 72. I²C Acknowledgment

8.5.1.2.2 I²C Clock Stretching

The SN1804044ZBHR device features clock stretching for the I²C protocol. The SN1804044ZBHR slave I²C port can hold the clock line (SCL) low after receiving (or sending) a byte, indicating that the slave is not yet ready to process more data. The master communicating with the slave must not finish the transmission of the current bit and must wait until the clock line actually goes high. When the slave is clock stretching, the clock line remains low.

The master must wait until it observes the clock line transitioning high plus an additional minimum time (4 μs for standard 100 kbps I²C) before pulling the clock low again.

Any clock pulse can be stretched but typically it is the interval before or after the acknowledgment bit.

8.5.1.2.3 I²C Address Setting

The boot code sets the hardware configurable unique I²C address of the SN1804044ZBHR device before the port is enabled to respond to I²C transactions. For the I2C1 interface, the unique I²C address is determined by the analog level set by the analog I2C_ADDR strap pin (three bits) as listed in Table 11.

Programming (continued)

Table 11. I²C Default Unique Address I2C1 (1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	1	I2C_ADDR_DECODE[2:0]			R/W

(1) Any bit is maskable for each port independently providing firmware override of the I²C address.

For the I2C2 interface, the unique I²C address is determined by the analog level set by the analog I2C_ADDR strap pin (three bits), along with the DEBUG_CTL2 and DEBUG_CTL1 logic values sensed during boot as listed in Table 12.

Table 12. I²C Default Unique Address I2C2 (1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	DEBUG_CTL2	DEBUG_CTL1	I2C_ADDR_DECODE[2:0]			R/W

(1) ny bit is maskable for each port independently, providing firmware override of the I²C address.

8.5.1.2.4 Unique-Address Interface

The unique-address interface allows for complex interaction between an I²C master and a single SN1804044ZBHR device. The I²C slave sub-address is used to receive or respond to the protocol commands of the host interface. Figure 73 and Figure 74 show the write and read protocol for the I²C slave interface. Figure 75 provides a key to explain the terminology used. The key to the protocol diagrams is in the SMBus specification and is repeated here in part.

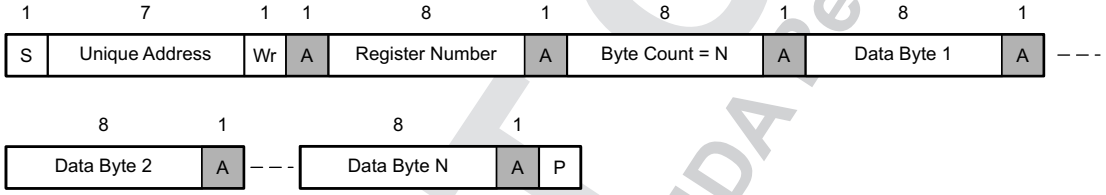


Figure 73. I²C Unique Address-Write Register Protocol

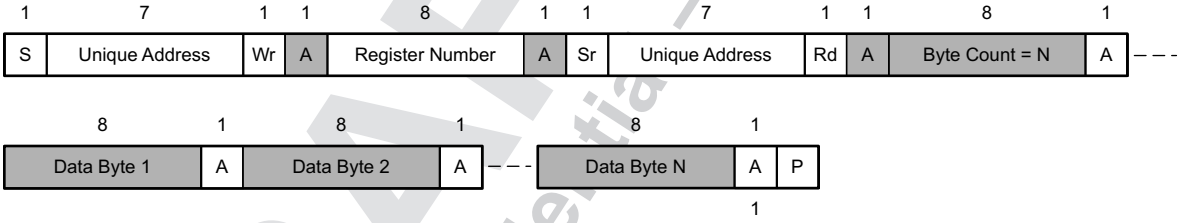


Figure 74. I²C Unique Address-Read Register Protocol

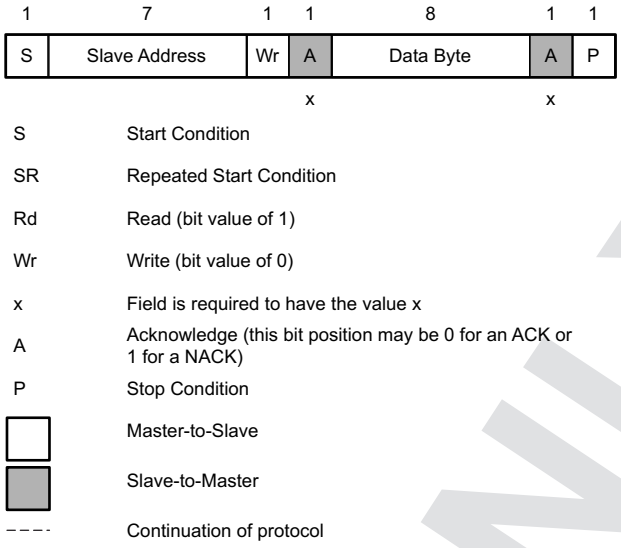


Figure 75. I²C Read/Write Protocol Key

8.5.1.2.5 I²C Pin Address Setting

To enable the setting of multiple I²C addresses using a single SN1804044ZBHR pin, a resistance is placed externally on the I2C_ADDR pin. The internal ADC then decodes the address from this resistance value. Figure 76 shows the decoding. For I2C2, the DEBUG_CTL1/2 are checked at the same time for the DC condition on this pin (high or low) for setting other bits of the address described previously. DEBUG_CTL1/2 are GPIO and the address decoding is done by firmware in the digital core. For I2C1, the DEBUG_CTL1/2 pin conditions are not checked.

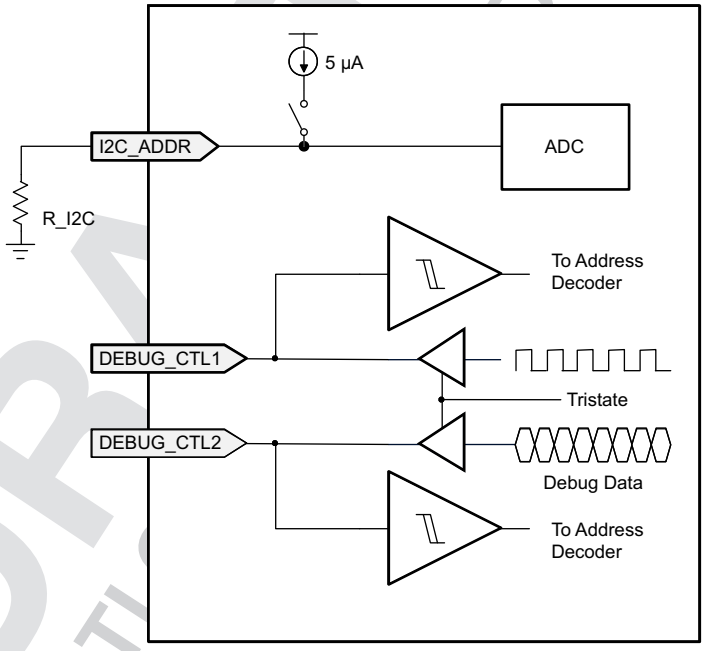


Figure 76. I²C Address Decode

Table 13 lists the external resistance required to set bits [3:1] of the I²C unique address. For the master SN1804044ZBHR device, the pin is grounded.

Table 13. I²C Address Resistance

SN1804044ZBHR DEVICE	EXTERNAL RESISTANCE (1%)	I²C UNIQUE ADDRESS [3:1]
Primary device slave 0	0	0x00
Secondary device slave 7	38.3k	0x01
Secondary device slave 6	84.5k	0x02
Secondary device slave 5	140k	0x03
Secondary device slave 4	205k	0x04
Secondary device slave 3	280k	0x05
Secondary device slave 2	374k	0x06
Secondary device slave 1	Open	0x07

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The typical applications of the SN1804044ZBHR device include chargers, notebooks, tablets, ultrabooks, docking systems, dongles, and any other product supporting USB Type-C, USB-PD, or both as a power source, power sink, data DFP, data UFP, or dual-role port (DRP). The typical applications outlined in the following sections detail a *Fully-Featured USB Type-C and PD Charger Application* and a *Dual-Port Notebook Application Supporting USB-PD Charging and DisplayPort*.

9.1.1 Device Configuration Content

The SN1804044ZBHR device leverages the device configuration selections that are currently available using the TPS6598x Configuration Tool. The device configurations allow for changing the following for a specific application:

1. Source capabilities
2. Sink capabilities
3. GPIO mappings
4. System configuration
5. Control configuration
6. Thunderbolt support
7. DisplayPort support
8. Alternate mode entry sequence
9. Identity descriptors
10. Interrupt event masks

9.1.2 Factory Set Device Configurations

The SN1804044ZBHR device supports factory-set device configurations. This option can be useful for devices that do not have a requirement for an external host or flash. These configurations are selectable by placing an external voltage on the GPIO8 ADC channel which is accomplished with a simple resistor divider from the LDO_3V3 terminal to ground as shown in Figure 77. Table 14 lists the voltage requirements to select the respective factory device configuration. The ADC channel on GPIO8 contains an integrated divide by 3 which ensures the voltage presented is within the range of the ADC reference.

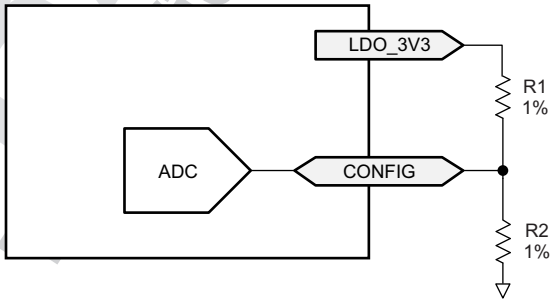


Figure 77. Factory Configuration Resistor Divider

Application Information (continued)

Table 14. Factory Device Configuration Selection

DIV = R2 / (R1 + R2)(1)		FACTORY DEVICE CONFIGURATION	DESCRIPTION
DIV_min	DIV_max		
0.00	0.08	0	UFP only 5-V at 0.9-A sink capability with *Ask for Max/* for anything from 0.9 to 3 A TBT Alternate Modes not supported DisplayPort alternate modes not supported
0.10	0.18	1	UFP only 5-V at 0.9-A sink capability with *Ask for Max/* for anything from 0.9 to 3 A TBT alternate modes not supported DisplayPort alternate modes: sink, C and D pin configurations
0.20	0.28	2	DFP only 5-V at 3-A source capability TBT alternate modes not supported DisplayPort alternate modes: source, C, D, and E pin configurations.
0.30	1.00	3	Infinite boot retry from flash to host I/F cycles.

(1) External resistor tolerance of 1% is required. Resistor values should be chosen to yield a DIV value centered nominally between listed minimum and maximum values.

The factory-set device configurations are only evaluated at boot of the device. The voltage on the GPIO8 is ignored on any device that was successfully loaded previously with a valid device configuration via an external flash or a host. Refer to the *Boot Flow* section. In addition, when the device completes the boot process, the GPIO8 can be reconfigured for reuse by the application.

9.2 Typical Applications

9.2.1 Fully-Featured USB Type-C and PD Charger Application

The SN1804044ZBHR device controls two separate power paths making it a flexible option for Type-C PD charger applications. In addition, the SN1804044ZBHR device supports VCONN power for *e-marked* cables which are required for applications that require greater than 3 A of current on VBUS. Figure 78 shows the high-level block diagram of a Type-C PD charger that is capable of supporting 5 V at 3 A and 20 V at 5 A. The 5-V output is supported by the SN1804044ZBHR internal FETs and the 20-V output uses the external FET path controlled by the SN1804044ZBHR NFET drive. This Type-C PD charger uses a receptacle for flexibility on cable choice.

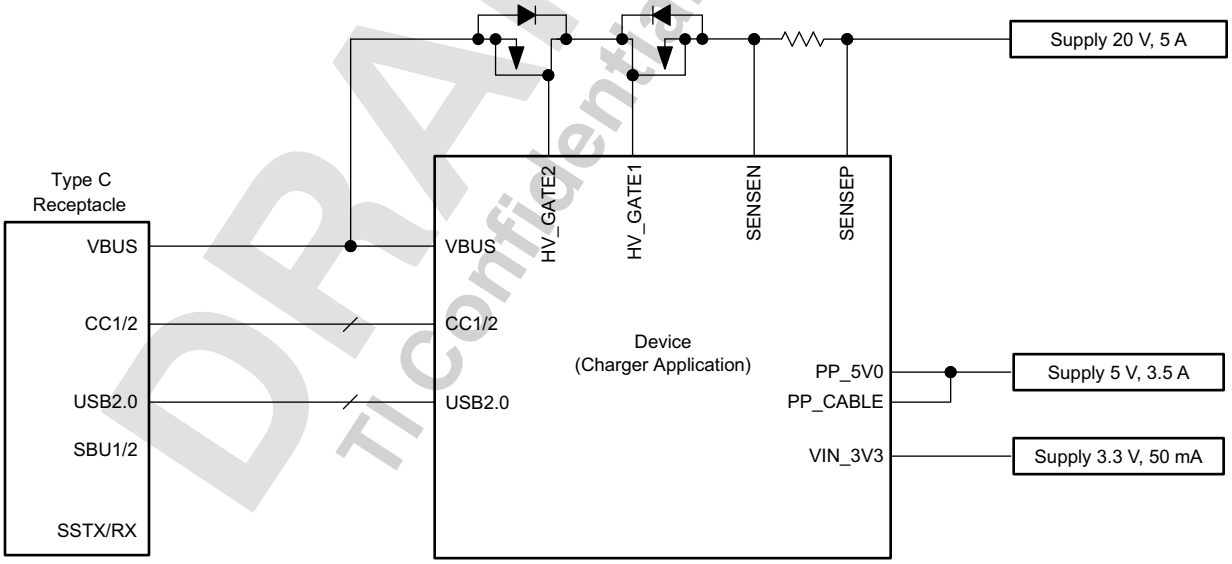


Figure 78. Type-C and PD Charger Application

Typical Applications (continued)

9.2.1.1 Design Requirements

For a USB Type-C and PD Charger application, Table 15 shows the input voltage requirements and expected current capabilities.

Table 15. Charging Application Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE	DIRECTION OF CURRENT
PP_5V0 input voltage and current capabilities	5 V, 3 A	Sourcing to VBUS
PP_CABLE input voltage and current capabilities	5 V, 500 mA	Sourcing to VCONN
EXT FET path input voltage and current capabilities	20 V, 5 A	Sourcing to VBUS
VIN_3V3 voltage and current requirements	2.85 through 3.45 V, 50 mA	Internal SN1804044ZBHR circuitry

9.2.1.1.1 External FET Path Components (PP_EXT and RSENSE)

The external FET path allows for the maximum PD power profile (20 V at 5 A) and design considerations must be taken into account for choosing the appropriate components to optimize performance.

Although a Type-C PD charger provides power, a condition could occur where a noncompliant device can be connected to the charger and force voltage back into the charger. To protect against this condition, the external FET path detects reverse current in both directions of the current path. The SN1804044ZBHR device uses two *back-to-back* NFETs to protect both sides of the system. Another design consideration is to rate the external NFETs above the Type-C and PD specification maximum which is 20 V. In this specific design example, 30-V NFETs are used that have an average $R_{DS,ON}$ of 5 mΩ to reduce losses.

The SN1804044ZBHR device supports either a 10-mΩ or a 5-mΩ sense resistor on the external FET path. This RSENSE resistor is used for current limiting and is used for the reverse-current protection of the power path. A 5-mΩ sense resistor is used in the design to minimize losses and I-R voltage drop. Table 16 lists the recommended parameters for the external NFET used. The total voltage drop across RSENSE and the external NFET could be determined by Equation 7. Consider the drop in the entire system and regulate accordingly to ensure that the output voltage is within the specification. Use Equation 8 to calculate the power lost through the external FET path.

Table 16. Recommended NFET Capabilities

VOLTAGE RATING	CURRENT RATING	$R_{DS,ON}$
30 V (minimum)	10 A (peak current)	< 10 mΩ

$$\text{Voltage Drop} = \text{DC Current (RSENSE} + \text{NFET1 } R_{DS,ON} + \text{NFET2 } R_{DS,ON} \quad (7)$$

$$\text{Power Loss} = \text{Voltage Drop} \times \text{DC Current} \quad (8)$$

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 SN1804044ZBHR External Flash

The external flash contains the SN1804044ZBHR application firmware and must be sized to 256 kB (minimum) when the flash is not shared with another device, but a recommended minimum of 1 MB is required when the flash memory of the SN1804044ZBHR device is shared with another device. This size allows for pointers and two copies of the firmware image to reside on the flash along with the required headers. The flash used is the W25Q80 device which is a 3.3-V flash and is powered from the LDO_3V3 output from the SN1804044ZBHR device.

9.2.1.2.2 I²C (I2C), Debug Control (DEBUG_CTL), and Single-Wire Debugger (SWD) Resistors

I2C_ADDR, DEBUG_CTL1/2 pins must be tied to GND through a 0-Ω resistor tied to GND directly if required to reduce solution size. Pullups on the I2C_CLK, I2C_SDA, and I2C_IRQ are used for debugging purposes. In most simple charger designs, I^2C communication may not be required. A 3.83-kΩ pullup resistor from SWD_DATA to LDO_3V3 and a 100-kΩ pulldown resistor from SWD_CLK to GND must also be used for debugging purposes.

9.2.1.2.3 Oscillator (R_OSC) Resistor

A 15-kΩ 0.1% resistor is required for key PD BMC communication and the USB2.0 endpoint timing. A 1% 15-kΩ resistor is not recommended to be used because the internal oscillators will not be controlled well enough by this loose resistor tolerance.

9.2.1.2.4 VBUS Capacitor and Ferrite Bead

A 1-µF ceramic capacitor is placed close to the SN1804044ZBHR VBUS pins. A 6-A ferrite bead is used in this design along with 4 high-frequency noise, 10-nF capacitors placed close to the Type-C connector to minimize noise.

9.2.1.2.5 Soft-Start (SS) Capacitor

The recommended 0.22-µF capacitor is placed on the SN1804044ZBHR SS pin.

9.2.1.2.6 USB Top (C_USB_T), USB Bottom (C_USB_B), and Sideband-Use (SBU) Connections

Although the charger is configured only as a power source, SBU1/2, USB top and bottom must be routed to the Type-C connector. This routing allows for debugging or for any specific alternate modes for power to be configured if required. ESD protection is used in the design on all of these nets as good design practice.

9.2.1.2.7 Port-Power Switch (PP_EXT, PP_5V0, and PP_CABLE) Capacitors

The design assumes that a DC-DC converter is connected to the paths where a significant output capacitance is on the DC-DCs to provide the additional capacitance for load steps. TI recommends to for the DC-DC converters for to be capable of supporting current spikes which can occur with certain PD configurations.

The PP_EXT path is capable of supporting up to 5 A which requires additional capacitance to support system loading by the device connected to the charger. A ceramic 10-µF (X7R/X5R) capacitor is used in this design. This capacitor must have at least a 25-V rating. TI recommends to have a 30-V or greater rated capacitor.

The PP_5V0 and PP_CABLE supplies are connected together, therefore a ceramic 22-µF (X7R/X5R) capacitor coupled with a 0.1-µF high-frequency capacitor is placed close to the SN1804044ZBHR device. The PP_5V0 path can support 3 A and the PP_CABLE path supports 600 mA for active Type-C PD cables.

The design assumes that a DC-DC converter is connected to the paths where there is significant output capacitance on the DC-DCs to provide the additional capacitance. It is recommended to for the DC-DC converters to be capable of supporting current spikes which can occur with certain PD configurations.

9.2.1.2.8 Cable Connection (CCn) Capacitors and RPD_Gn Connections

This charger application is designed to only be a source of power and does not support a dead-battery condition. The RPD_G1 and RPD_G2 resistor must be tied to GND and not connected to the CC1 and CC2 (respectively). The CC1 and CC2 lines require a 220-pF capacitor to GND.

9.2.1.2.9 LDO_3V3, LDO_1V8A, LDO_1V8D, LDO_BMC, VOUT_3V3, VIN_3V3, and VDDIO

For all capacitances, the DC-voltage derating of the ceramic capacitors must be considered. Generally the effective capacitance is halved with the applied voltage.

VIN_3V3 is connected to VDDIO which ensures that the I/Os of the SN1804044ZBHR device are configured to 3.3 V. A 1-µF capacitor is used and is shared between VDDIO and VIN_3V3. LDO_1V8D, LDO_1V8A, and LDO_BMC each have their own 1-µF capacitor. In this design, LDO_3V3 powers the external flash and various pullups of the SN1804044ZBHR device. A 10-µF capacitor was selected to support these additional connections. VOUT_3V3 is not used in this design and the capacitor is not required.

9.2.1.3 Application Curve

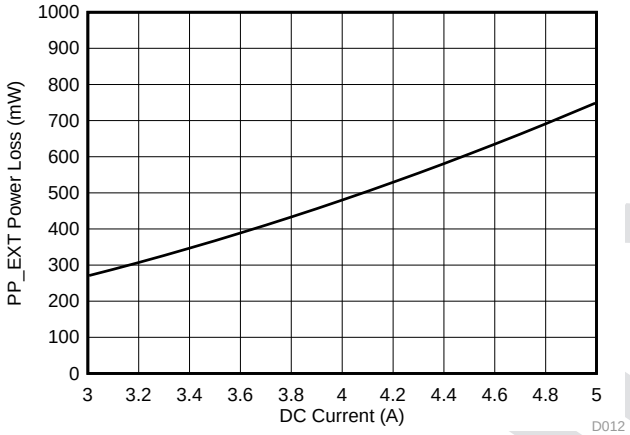


Figure 79. PP_EXT Power Loss

9.2.2 Dual-Port Notebook Application Supporting USB-PD Charging and DisplayPort

The SN1804044ZBHR device features support for DisplayPort over Type-C alternate mode and manages sinking and sourcing of power in power delivery. The block diagram (Figure 80) shows a two-port system that is capable of charging from either Type-C port over PD, DisplayPort alternate mode, and delivering battery power to a bus-powered device. With the DisplayPort support, the SN1804044ZBHR device controls an external SuperSpeed multiplexer, HD3SS460, to route the appropriate super-speed signals to the Type-C connector. The HD3SS460 is controlled through GPIOs configured by the SN1804044ZBHR application code and the HD3SS460 is designed to meet the timing requirements defined by the DisplayPort over Type-C specification. A system controller is also required to handle some of the dynamic aspects of power delivery such as reducing power capabilities when system battery power is low. An audio accessory device is supported by the design as well. Although USB_RP_P and USB_RP_N are not shown in the block diagram, they must be connected to the system-side IC that will receive and send USB2.0 high-speed data through the integrated multiplexer of the SN1804044ZBHR device.

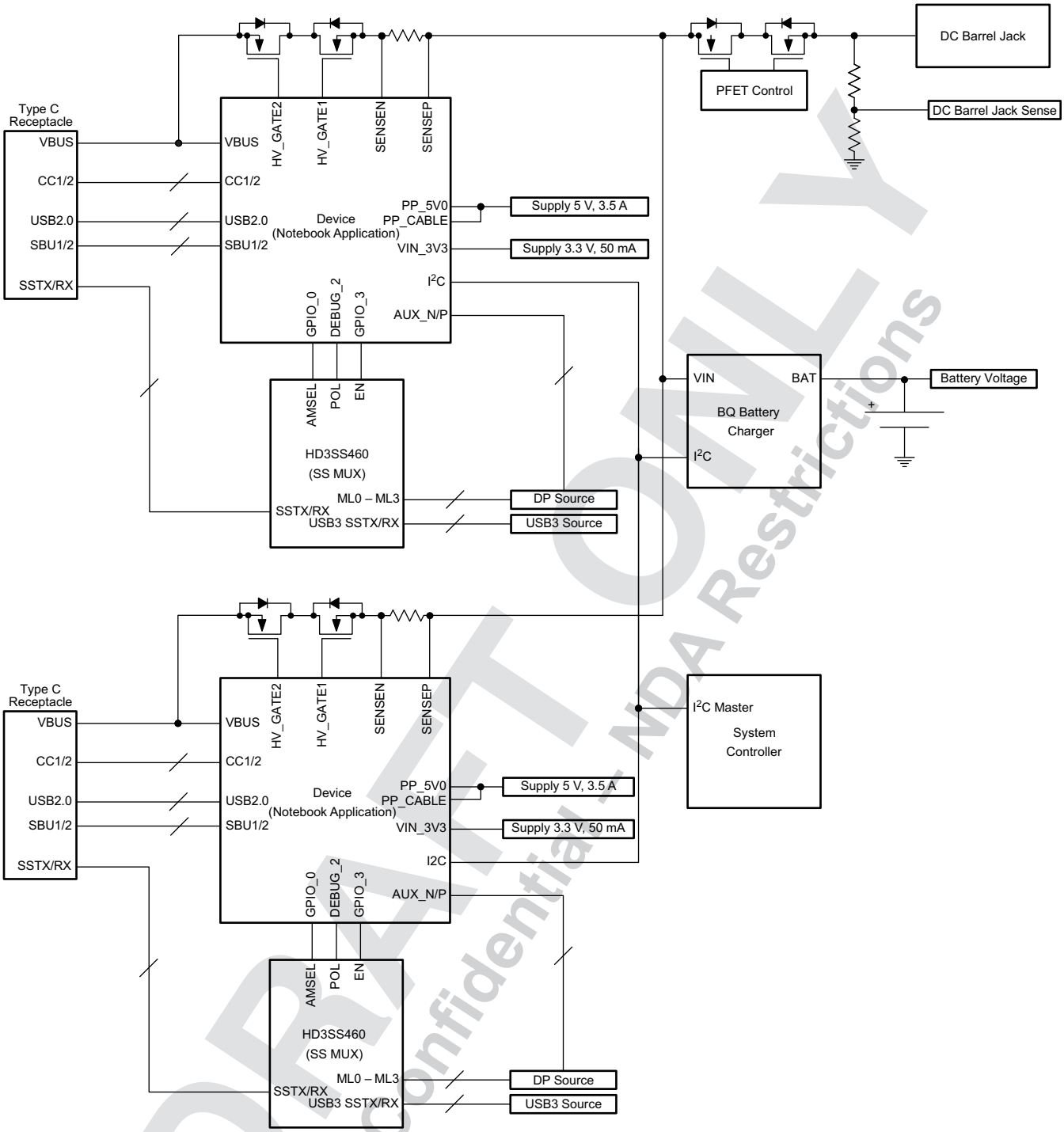


Figure 80. Dual-Port Notebook Application

9.2.2.1 Design Requirements

Table 17 lists the input voltage requirements and expected current capabilities for a dual-port notebook application.

Table 17. Dual-Port Notebook Application Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE	DIRECTION OF CURRENT
PP_5V0 input voltage and current capabilities	5 V, 3 A	Sourcing to VBUS
PP_CABLE input voltage and current capabilities	5 V, 500 mA	Sourcing to VCONN
EXT FET path voltage and current capabilities	20 V, 3 A	Sourcing to VBUS or sinking from VBUS
VIN_3V3 voltage and current requirements	2.85 through 3.45 V, 50 mA	Internal SN1804044ZBHR circuitry

9.2.2.1.1 Source-Power Delivery Profiles for Type-C Ports

Table 18 shows the summary of the source PD profiles that are supported for this specific design. PDO 1 and 2 are always be present in the system and are able to be negotiated without any other system interaction. When a DC barrel-jack voltage is sensed, PDO 3 becomes available for power delivery negotiation. The external sense resistor, RSENSE, is configured to only measure the current being sourced by the system. When operating as a sink of power the input current cannot be measured in this configuration.

Table 18. Source USB-PD Profiles

PDO	PDO TYPE	VOLTAGE	CURRENT	EXTERNALLY DEPENDENT
PDO1	Fixed Supply	5 V	3 A	No
PDO2	Fixed Supply	20 V	3 A	Yes

9.2.2.1.2 Sink-Power Delivery Profile for Type-C Ports

The two Type-C ports used in this design support power delivery and enable charging over a Type-C connection. Table 19 shows the sink profile supported by both of the ports. The reverse-current blocking of the SN1804044ZBHR device allows both of the Type-C ports to negotiate a power contract, but it is good system practice for the system controller to change the sink profile when a power contract is established. When the DC barrel jack is connected, the SN1804044ZBHR device renegotiates the PD contract to no longer charge through Type-C and have the DC barrel jack take precedence when connected.

Table 19. Sink USB-PD Profile

RDO Type	VOLTAGE	CURRENT	EXTERNALLY DEPENDENT
Fixed Supply	20 V	3 A	Yes

9.2.2.2 Detailed Design Procedure

The same passive components used in the *Fully-Featured USB Type-C and PD Charger Application* section are also applicable in this design to support all of the features of the SN1804044ZBHR device. Additional design information is provided in this section to explain the connections between the SN1804044ZBHR device and the system controller, and the SN1804044ZBHR device and the HD3SS460 SuperSpeed multiplexer.

9.2.2.2.1 SN1804044ZBHR and System-Controller Interaction

The SN1804044ZBHR device features two I^2C slave ports that can be used simultaneously, where the system controller can write to either of the I^2C slave ports. Each I^2C port has an I^2C interrupt that informs the system controller that a change has occurred in the system. This feature allows the system controller to dynamically budget power and reconfigures the capabilities of the port which are dependent on the current state of the system. For example, if a battery power contract is established and the system is running low on battery power, the system controller could notify the SN1804044ZBHR to renegotiate a power contract. The system controller is also used for updating the SN1804044ZBHR firmware over I^2C, where the operating system is able to load the firmware update to the system controller. Then the system controller can update the firmware update though I^2C.

9.2.2.2.2 HD3SS460 Control and DisplayPort Configuration

The two Type-C ports in this design support DisplayPort simultaneously on both ports. When a system is unable of supporting video on both ports, the system controller disables the DisplayPort on the second Type-C port through I^2C. Table 20 lists the DisplayPort configurations supported in the system. Table 21 shows the summary of the SN1804044ZBHR GPIO signals control for the HD3SS460 device. Although the HD3SS460 device is able to multiplex the required AUX_N/P signals to the SBU_1/2 pins, these signals are connected through the SN1804044ZBHR device for additional support of custom alternate mode configurations.

Table 20. Supported DisplayPort Configurations

CONFIGURATION	DisplayPort ROLE	DisplayPort PIN ASSIGNMENT	DisplayPort LANES
Configuration 1	DFP_D	Pin assignment C	4 lane
Configuration 2	DFP_D	Pin assignment D	2 lane and USB 3.1
Configuration 3	DFP_D	Pin assignment E	4 lane (dongle support)

Table 21. SN1804044ZBHR and HD3SS460 GPIO Control

SN1804044ZBHR GPIO	HD3SS460 CONTROL PIN	DESCRIPTION
GPIO_0	AMSEL	Alternate mode selection (DP/USB3)
GPIO_3	EN	Super-speed mux enable
DEBUG2	POL	Type-C cable

9.2.2.2.3 DC Barrel Jack and Type-C PD Charging

The system is designed to either charge over Type-C or from the DC barrel jack. The SN1804044ZBHR device detects that the DC barrel jack is connected to GPIOn. In the simplest form, a voltage divider can be set to the GPIO I/O level when the DC barrel-jack voltage is present as shown in Figure 81. A comparator circuit is recommend and used in this design for design robustness as shown in Figure 82.

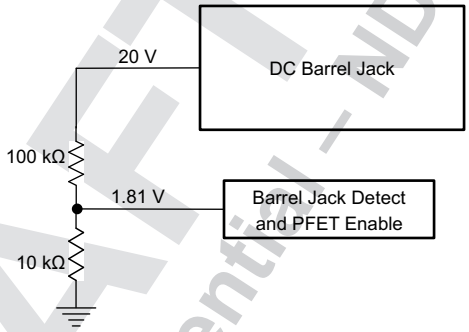


Figure 81. DC Barrel-Jack Voltage Divider

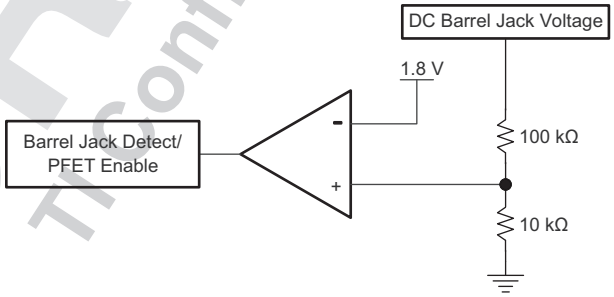


Figure 82. Barrel-Jack Detect Comparator

This detect signal is used to determine if the barrel jack is present to support the 20-V PD power contracts and to switch charging from the barrel jack to Type-C or Type-C to barrel jack. When the DC barrel jack is detected, the SN1804044ZBHR device at each Type-C port does not request 20 V for charging and the system is able to support a 20-V source power contract to another device. When the DC barrel jack is disconnected the SN1804044ZBHR device exits any 20-V source power contract and renegotiates a power contract. When the DC barrel jack is connected, the SN1804044ZBHR device sends updated source capabilities and renegotiates a power contract if required.

The PFET enable is controlled by the DC barrel-jack detect comparator shown in Figure 82. This control allows the system to power up from a dead battery through the barrel jack as well as the Type-C ports. Figure 84 shows the flow between changing from DC barrel-jack charging and USB-PD charging. The example uses back-to-back PFETs for disabling and enabling the power path for the DC barrel jack. PFETs that are rated above the specified parameters must be used to ensure robustness of the system. The DC barrel-jack voltage in this design is assumed to be 20 V at 5 A, so the PFETs are recommended to be rated at a minimum of 30 V and 10 A of current.

The SN1804044ZBHR device in this design also provides the GPIO control for the PFET gate drive that passes the DC barrel-jack voltage to the system. Figure 84 shows the flow between changing from DC barrel-jack charging and Type-C PD charging.

9.2.2.2.4 Primary SN1804044ZBHR Flash Master and Secondary Port

A single optional flash that contains code, device configuration, of both can be used for two SN1804044ZBHR devices in a system where the primary SN1804044ZBHR device is connected to the flash and the secondary SN1804044ZBHR device is connected to the primary through UART. UART data is used to pass the firmware from the primary SN1804044ZBHR device to the secondary SN1804044ZBHR device in the system. Figure 83 shows a simplified block diagram of how a primary and secondary SN1804044ZBHR device are connected using a single flash. The primary SN1804044ZBHR must have the I2C_ADDR pin tied to GND with a 0-Ω resistor to identify it as the primary SN1804044ZBHR device.

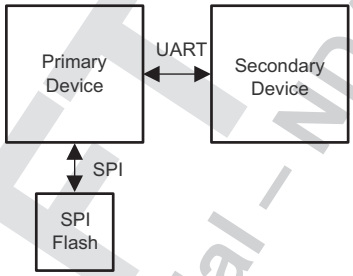


Figure 83. Primary and Secondary SN1804044ZBHR Sharing a Single Flash

9.2.2.2.5 SN1804044ZBHR Dead-Battery Support Primary and Secondary Port

The SN1804044ZBHR device supports dead-battery functionality to be able to power up from the Type-C port. This design supports dead battery using the PP_EXT path, where RPD_G1/2 and CC1/2 are connected respectively, and BUSPOWERZ is connected to GND to path 5 V VBUS into the system through the PP_EXT path. The SN1804044ZBHR device soft starts the PP_EXT path to comply with USB2.0 inrush-current requirements. The SN1804044ZBHR device boots and is then able communicate over PD and establish a power contract at the required 20 V. Figure 85 shows the boot-up sequence of the primary SN1804044ZBHR device.

When the SN1804044ZBHR device that is not connected to the flash is connected in a dead-battery condition, it passes the 5 V from VBUS into the battery charger where the battery can generate the required system 3.3-V rail to both of the SN1804044ZBHR devices. When the primary SN1804044ZBHR device has a valid 3.3-V supply (VBUS = 0 V on the primary SN1804044ZBHR device), the device loads any code patch or device configurations from the flash and pass it to the secondary SN1804044ZBHR device that is connected. When the secondary SN1804044ZBHR device has loaded the code patch and the device configuration over UART, the device can negotiate a 20-V power contract. Figure 86 shows the dead-battery sequence of the secondary SN1804044ZBHR device.

9.2.2.2.6 Debugging Methods

The SN1804044ZBHR device has methods of debugging a Type-C and PD system. In addition to the resistances recommended in the *I²C (I2C), Debug Control (DEBUG_CTL), and Single-Wire Debugger (SWD) Resistors* section, additional series resistors are used for debugging. The two I²C channels allow a designer to check the system state through the host-interface specification. By attaching 0-Ω series resistors between the I²C master and the SN1804044ZBHR device, and additionally adding 0-Ω series resistors between the SN1804044ZBHR device and test points, a multi-master scenario can be avoided. Avoiding this scenario allows breaking the connection between the I²C channels and the system to allow I²C access to the SN1804044ZBHR device from an external tool. A header is used to allow for connections without soldering; however, SMT test pads can be used to provide a place to solder *blue-wires* for testing.

Exposing the SWD_DAT and SWD_CLK pins allows for more advanced debugging if required. A header or SMT test point is also used for the SWD_DATA and SWD_CLK pins.

9.2.2.3 Application Curves

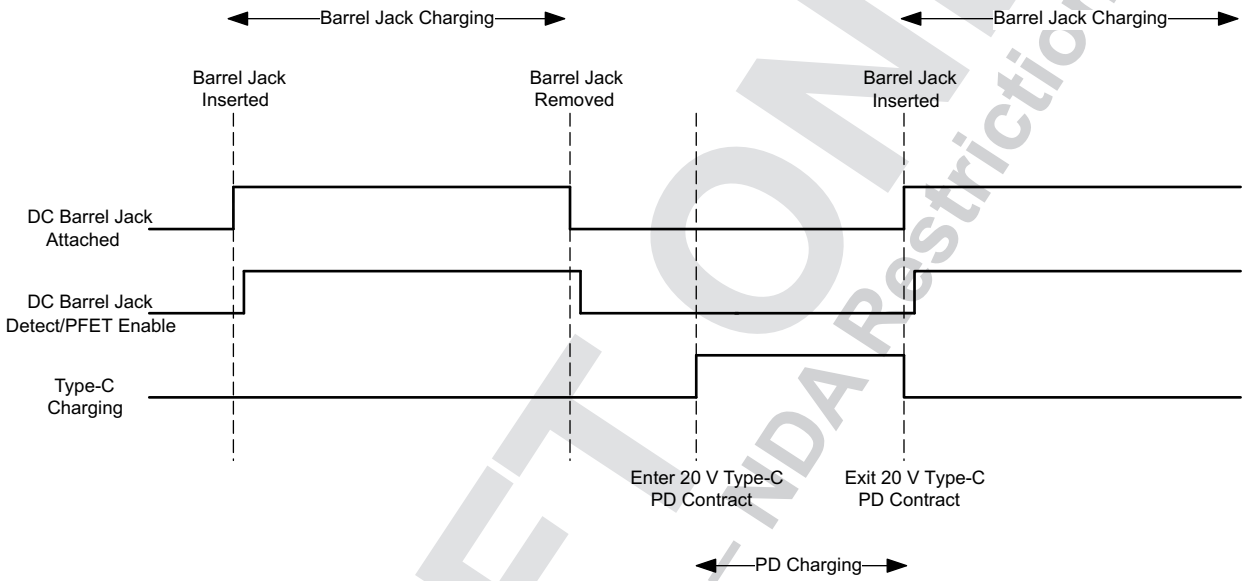


Figure 84. DC Barrel Jack and Type-C PD Charging Hand-Off

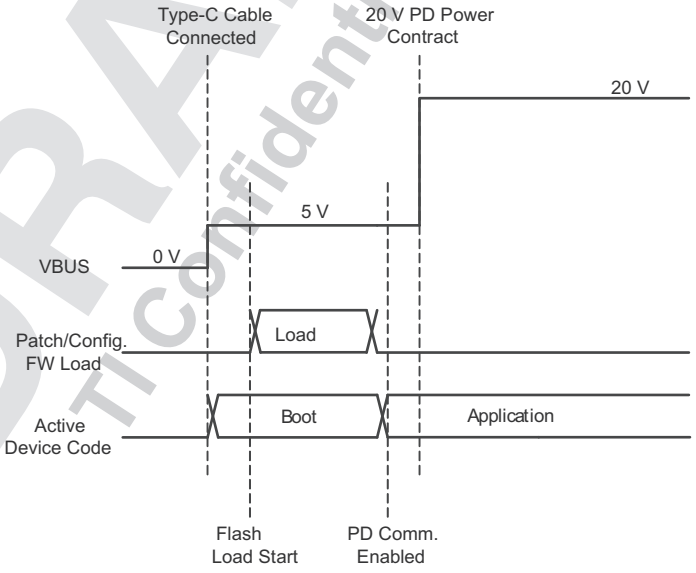


Figure 85. Primary SN1804044ZBHR Dead-Battery Sequence

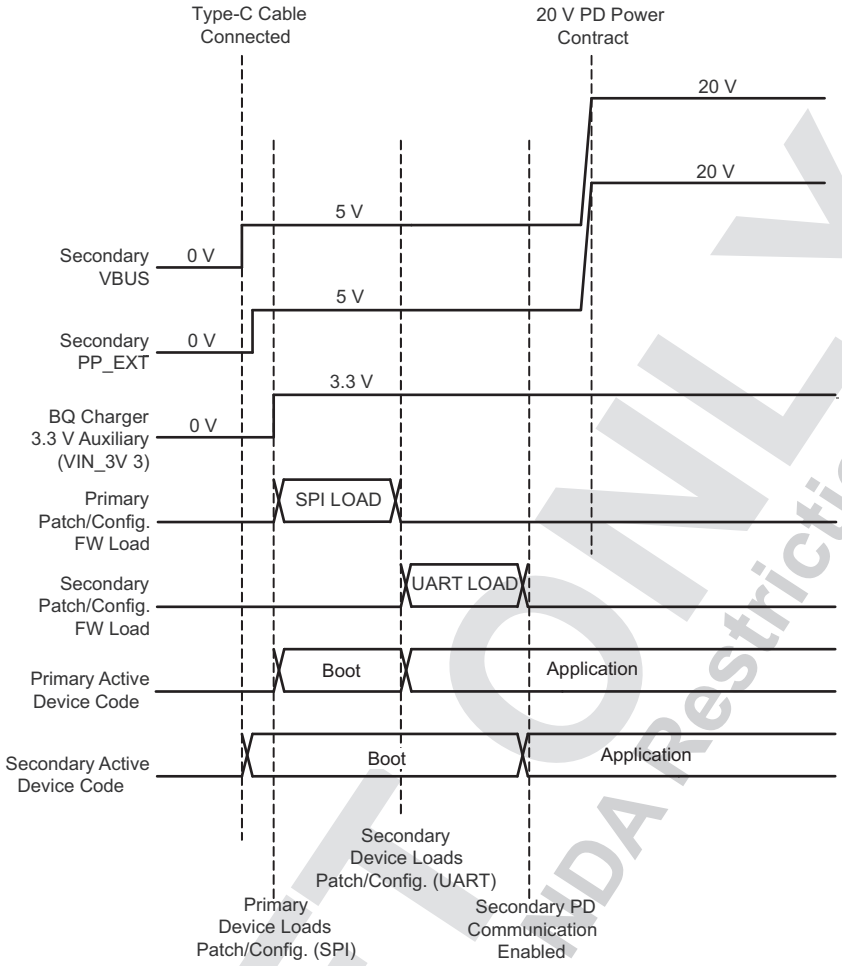


Figure 86. Secondary SN1804044ZBHR Dead-Battery Sequence

10 Power Supply Recommendations

10.1 3.3-V Power

10.1.1 1VIN_3V3 Input Switch

The VIN_3V3 input is the main supply to the SN1804044ZBHR device. The VIN_3V3 switch (S1 in Figure 44) is a unidirectional switch from VIN_3V3 to LDO_3V3, not allowing current to flow backwards from LDO_3V3 to VIN_3V3. This switch is on when 3.3 V is available. See Table 22 for the recommended external capacitance on the VIN_3V3 pin.

10.1.2 VOUT_3V3 Output Switch

The VOUT_3V3 output switch (S2 in Figure 44) enables a low-current auxiliary supply to an external element. This switch is controlled by and is off by default. The VOUT_3V3 output has a supervisory circuit that drives the RESETZ output as a POR signal to external elements. RESETZ is also asserted by the MRESET pin or a host controller. See RESETZ and MRESET for more details on RESETZ. See Table 22 for the recommended external capacitance on the VOUT_3V3 pin.

10.1.3 VBUS 3.3-V LDO

The 3.3-V LDO from VBUS steps down voltage from VBUS to LDO_3V3 which allows the SN1804044ZBHR device to be powered from VBUS when VIN_3V3 is unavailable. This LDO steps down any recommended voltage on the VBUS pin. When VBUS is 20 V, as is allowable by USB PD, the internal circuitry of the SN1804044ZBHR device operates without triggering thermal shutdown; however, a significant external load on the LDO_3V3 pin can increase the temperature enough to trigger a thermal shutdown. The VBUS 3.3-V LDO blocks reverse current from LDO_3V3 back to VBUS allowing VBUS to be unpowered when LDO_3V3 is driven from another source. See Table 22 for the recommended external capacitance on the VBUS and LDO_3V3 pins.

10.2 1.8-V Core Power

The internal circuitry is powered from 1.8 V. Two LDOs step the voltage down from LDO_3V3 to 1.8 V. One LDO powers the internal digital circuits. The other LDO powers the internal low-voltage analog circuits.

10.2.1 1.8-V Digital LDO

The 1.8-V digital LDO provides power to all internal low-voltage digital circuits which includes the digital core, memory, and other digital circuits. See Table 22 for the recommended external capacitance on the LDO_1V8D pin.

10.2.2 1.8-V Analog LDO

The 1.8-V analog LDO provides power to all internal low-voltage analog circuits. See Table 22 for the recommended external capacitance on the LDO_1V8A pin.

10.3 VDDIO

The VDDIO pin provides a secondary input allowing some I/Os to be powered by a source other than LDO_3V3. The default state is power from LDO_3V3. The memory stored in the flash configures the I/Os to use LDO_3V3 or VDDIO as a source. The application code automatically scales the input and output voltage thresholds of the I/O buffer accordingly. See the *I/O Buffers* section for more information on the I/O buffer circuitry. See Table 22 for the recommended external capacitance on the VDDIO pin.

10.3.1 Recommended Supply Load Capacitance

Table 22 lists the recommended board capacitances for the various supplies. The typical capacitance is the nominally rated capacitance that must be placed on the board as close to the pin as possible. The maximum capacitance must not be exceeded on pins for which it is specified. The minimum capacitance is minimum capacitance allowing for tolerances and voltage derating ensuring proper operation.

VDDIO (continued)

Table 22. Recommended Supply Load Capacitance

PARAMETER	DESCRIPTION	VOLTAGE RATING	CAPACITANCE		
			MIN (ABS MIN)	TYP (TYP PLACED)	MAX (ABS MAX)
CVIN_3V3	Capacitance on VIN_3V3	6.3 V	5 µF	10 µF	
CLDO_3V3	Capacitance on LDO_3V3	6.3 V	5 µF	10 µF	25 µF
CVOUT_3V3	Capacitance on VOUT_3V3	6.3 V	0.1 µF	1 µF	2.5 µF
CLDO_1V8D	Capacitance on LDO_1V8D	4 V	500 nF	2.2 µF	12 µF
CLDO_1V8A	Capacitance on LDO_1V8A	4 V	500 nF	2.2 µF	12 µF
CLDO_BMC	Capacitance on LDO_BMC	4 V	1 µF	2.2 µF	4 µF
CVDDIO	Capacitance on VDDIO. When shorted to LDO_3V3, the CLDO_3V3 capacitance may be shared.	6.3 V	0.1 µF	1 µF	
CVBUS	Capacitance on VBUS 1	25 V	0.5 µF	1 µF	12 µF
CPP_5V0	Capacitance on PP_5V0	10 V	2.5 µF	4.7 µF	
CPP_CABLE	Capacitance on PP_CABLE. When shorted to PP_5V0, the CPP_5V0 capacitance may be shared.	10 V	2.5 µF	4.7 µF	
CPP_EXT	Capacitance on external high voltage source to VBUS	25 V	2.5 µF	4.7 µF	
	Capacitance on external high voltage sink from VBUS	25 V		47 µF	120 µF
CSS	Capacitance on soft start pin	6.3 V		220 nF	

10.3.2 Schottky for Current-Surge Protection

To prevent the possibility of large ground currents into the SN1804044ZBHR device during sudden disconnects because of inductive effects in a cable, TI recommends that a Schottky be placed from VBUS to GND as shown in Figure 87. The NSR20F30NXT5G diode is recommended.

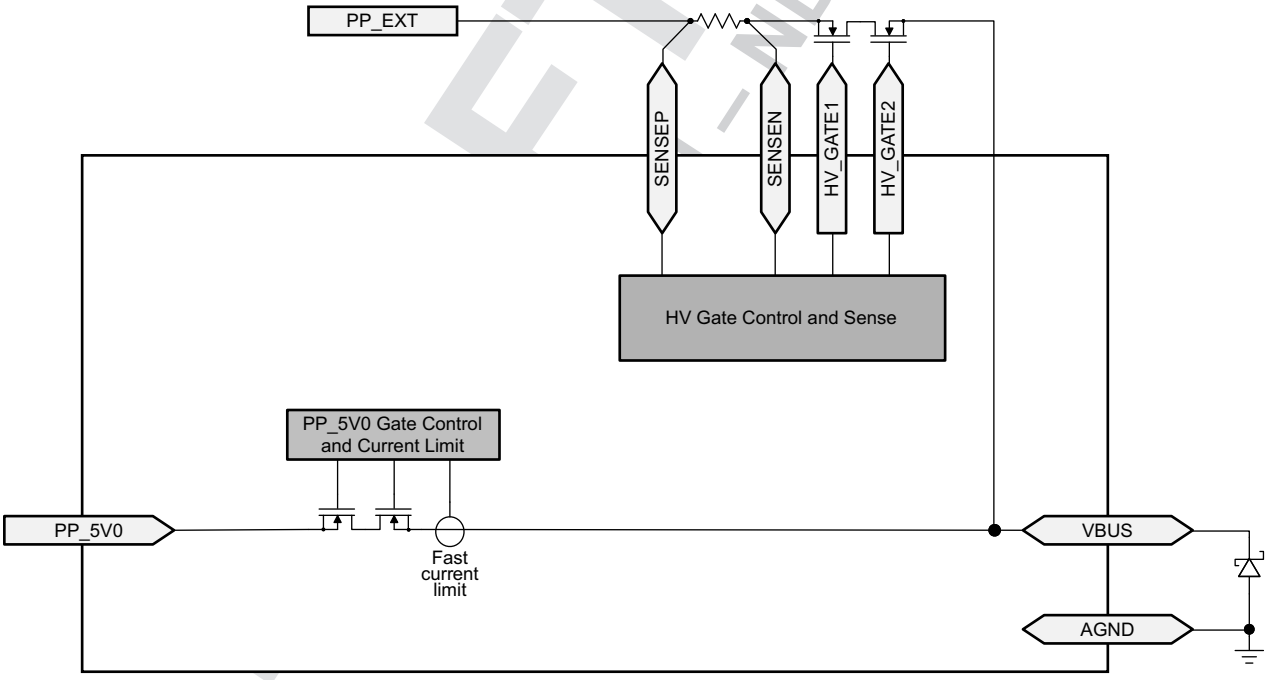


Figure 87. Schottky on VBUS for Current-Surge Protection

11 Layout

11.1 Layout Guidelines

Proper routing and placement will maintain signal integrity for high-speed signals and improve the thermal dissipation from the SN1804044ZBHR power path. The combination of power and high-speed data signals are easily routed if the following guidelines are followed. Consulting with a printed circuit board (PCB) manufacturer is a best practice to verify manufacturing capabilities.

11.1.1 SN1804044ZBHR Recommended Footprints

11.1.1.1 Standard SN1804044ZBHR Footprint (Circular Pads)

Figure 88 shows the SN1804044ZBHR footprint using a 0.25mm pad diameter. This footprint is applicable to boards that use an HDI PCB process that uses smaller vias to fan-out into the inner layers of the PCB. This footprint requires via fill and tenting and is recommended for size-constrained applications. The circular footprint allows for easy fan-out into other layers of the PCB and better thermal dissipation into the GND planes. Figure 89 shows the recommended via sizing for use under the balls. The size is 5-mil hole and 10-mil diameter. This via size allows for approximately 1.5-A current rating at 3 mΩ of DC resistance with 1.6 nH of inductance. TI recommends verifying these numbers with board manufacturing processes used in fabrication of the PCB.

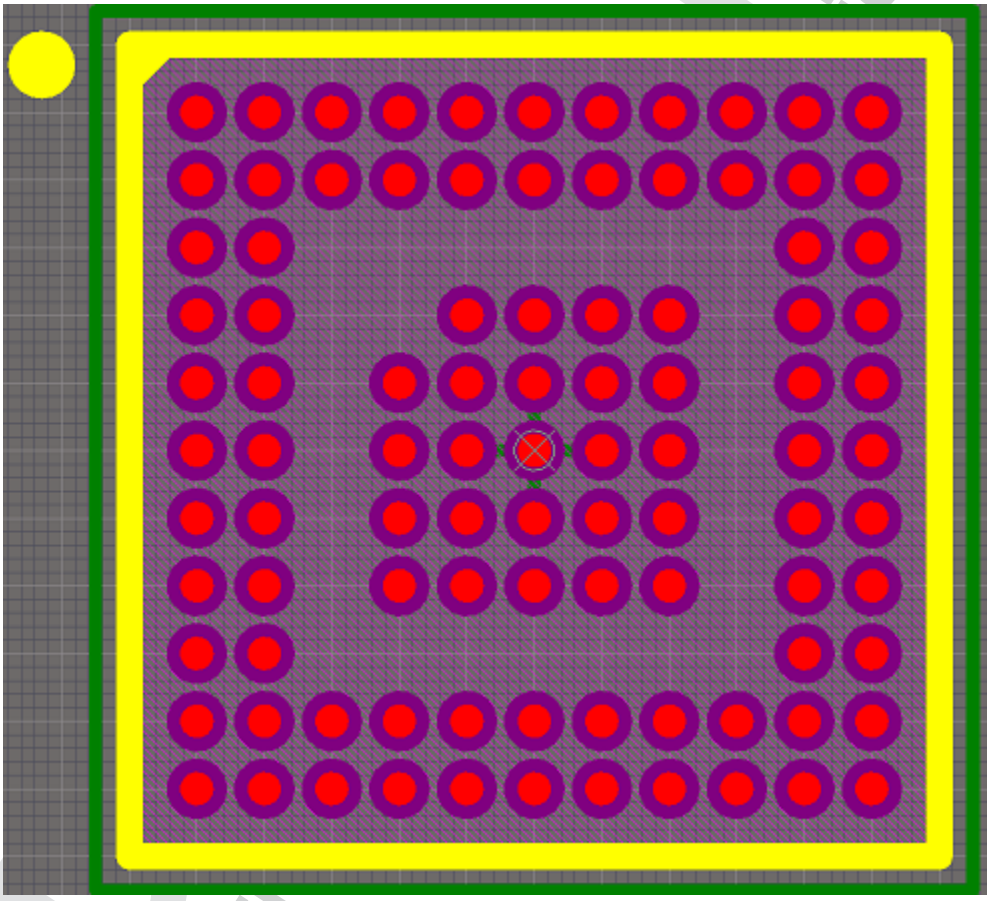


Figure 88. Top-View Standard SN1804044ZBHR Footprint (Circular Pads)

Layout Guidelines (continued)

Figure 89. Under Ball Recommended Via Size

11.1.2 Alternate SN1804044ZBHR Footprint (Oval Pads)

Figure 90 shows the SN1804044ZBHR footprint using oval-shaped pads in specific locations which allows the PCB designer to route the inner perimeter balls through the top layer. The balls around the perimeter have pads in an oval shape with the exception of the corner balls. Figure 91 shows the sizing for the oval pads, 0.25 mm × 0.17 mm. All of the other non-oval shaped pads have a 0.25-mm diameter. This footprint is recommended for MDI (medium density) PCB designs that are generally less expensive to build. The void under the SN1804044ZBHR device allows for vias to route the inner signals and connect to the GND and power planes. Figure 92 shows the recommended minimum via size (8mil hole and 16-mil diameter). The recommended 8mil vias will be rated for approximately 1.8 A of DC current and 1.5 mΩ of resistance with 1.3 nH of inductance. Some board manufactures may offer 6-mil hole and 12-mil diameter vias with a mechanical drill..

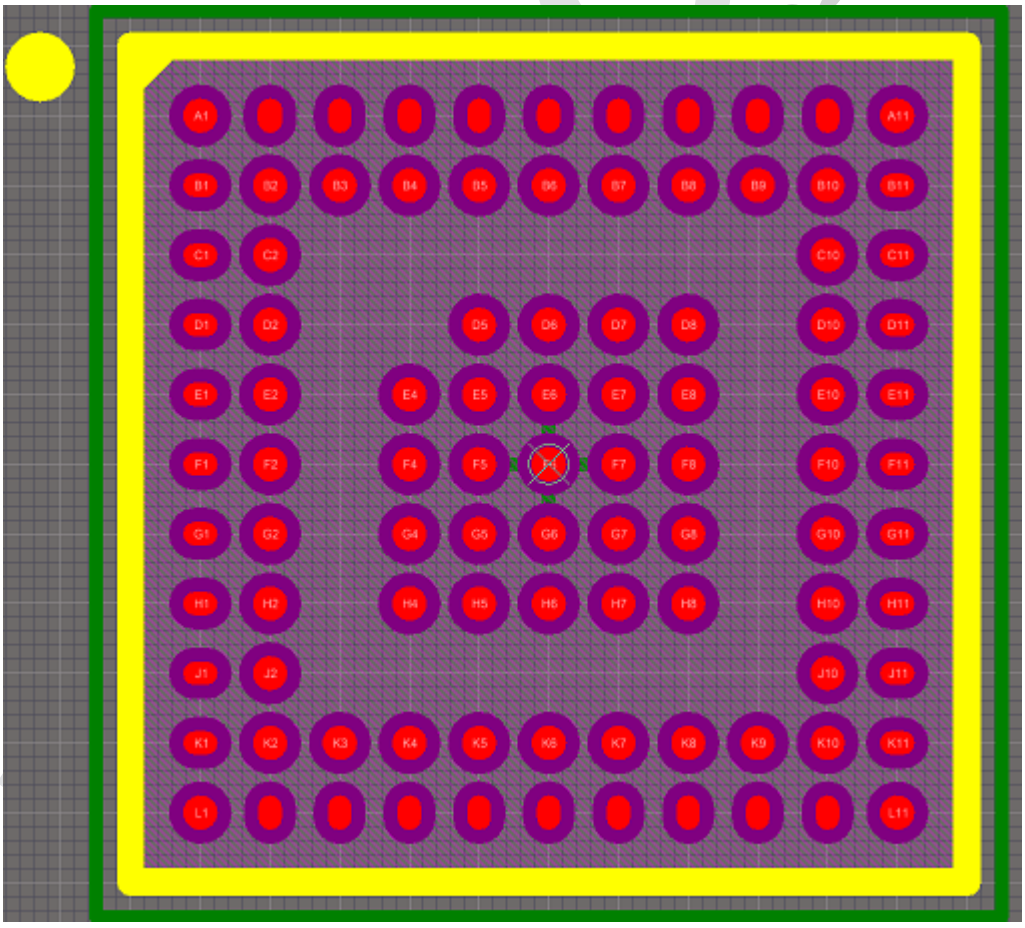


Figure 90. Top-View Alternate SN1804044ZBHR Footprint (Oval Pads)

Layout Guidelines (continued)

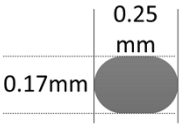


Figure 91. Oval Pad Sizing

Figure 92. Recommended Minimum Via Sizing

11.1.3 Top SN1804044ZBHR Placement and Bottom Component Placement and Layout

When the SN1804044ZBHR device is placed on top and the components on bottom the solution size are at the smallest. For systems that do not use the optional, external FET path, the solution size averages less than 64 mm^2 (8 mm × 8 mm). Systems that implement the optional external FET path average a solution size of less than 100 mm^2 (10 mm × 10 mm). These averages vary with component selection (NFETs, passives, and others). Selection of the oval pad SN1804044ZBHR footprint or standard SN1804044ZBHR footprint allows for similar results.

11.1.4 Oval Pad Footprint Layout and Placement

The oval pad footprint layout is generally more difficult to route than the standard footprint because of the top layer fan-out and void via placement required; however, when the footprint with oval pads is used, *Via on Pads*, laser-drilled vias, and HDI board processes are not required. Therefore, a footprint with oval pads is ideal for cost-optimized applications and is used for the following the layout example. This layout example follows the charger application example (see the *Fully-Featured USB Type-C and PD Charger Application* section) and includes all required passive components needed for this application. This design uses both the internal and optional external FET paths for sourcing and sinking power respectively. Follow the differential impedances for high-speed signals defined by the specifications (DisplayPort - AUXN/P and USB2.0). All I/Os are fanned out to provide an example for routing out all pins, not all designs will use all of the I/O on the SN1804044ZBHR device.

11.1.5 Component Placement

Placement of components on the top and bottom layers is used for this example to minimize solution size. The SN1804044ZBHR device is placed on the top layer of the board and the majority of the components are placed on the bottom layer. When placing the components on the bottom layer, TI recommends that they are placed directly under the SN1804044ZBHR device in a manner where the pads of the components are not directly under the void on the top layer. Figure 93 and Figure 94 show the placement in 2-D. Figure 95 and Figure 96 show the placement in 3-D.

11.1.6 Designs Rules and Guidance

When starting to route nets, starting with 4 mil clearance spacing is best. The designer may have to adjust the 4-mil clearance to 3.5 mil when fanning out the top layer routes. With the routing of the top layer having a tight clearance, TI recommends having the layout grid snapped to 1 mil. For certain routes on the layout done in this guide, the grid snap was set to 0.1 mil. For component spacing this design used a 20-mil clearance between components. The silk screen around certain passive components can be deleted to allow for closer placement of components.

Layout Guidelines (continued)

11.1.7 Routing PP_EXT, PP_5V0, and VBUS

On the top layer, create pours for PP_EXT, PP_5V0 and VBUS to extend area to place an 8-mil hole and 16-mil diameter vias to connect to the bottom layer. A minimum of 4 vias must be connected between the top and bottom layer. For the bottom layer, place pours that connect the PP_EXT, PP_5V0, and VBUS capacitors to the respective vias. The external FETS must also be connected through pours and place vias for the external FET gates. For 5-A systems, special consideration must be taken for ensuring enough copper is used to handle the higher current. For 0.5-oz copper top or bottom pours with 0.5-oz plating requires approximately a 120-mil pour width for 5-A support. When routing the 5 A through a 0.5-oz internal layer, more than 200 mil will be required to carry the current. Figure 97 and Figure 98 show the pours used in this example.

11.1.8 Routing Top and Bottom Passive Components

The next step is to route the connections to the passive components on the top and bottom layers. For the top layer only the CC1 and CC2 capacitors are placed on top. Routing the CC1 and CC2 lines with a 8-mil trace facilitates the required current for supporting powered Type-C cables through VCONN. For more information on VCONN, refer to the Type-C specification. Figure 99 shows how to route to the CC1 and CC2 lines to the respective capacitors. For the capacitor at the GND pin, use a 10-mil trace if possible. This particular system supports a dead-battery condition in which RPD_G1/2 is connected to CC1/2.

The top layer pads must be connected to the bottom placed component through vias (an 8-mil hole and a 16-mil diameter are recommended). For the VIN_3V3, VDDIO, LDO_3V3, LDO_1V8A, LDO1V8D, LDO_BMC, and VOUT_3V3, use 6-mil traces to route. For PP_CABLE, route using an 8-mil trace. For all other routes 4-mil traces can be used. To allow for additional space for routing, stagger the component vias to leave room for routing other signal nets. Figure 100 and Figure 101 show the top and bottom routing. Table 23 lists a summary of the trace widths.

Table 23. Routing Trace Widths

ROUTE	WIDTH (mil)
CC1, CC2, PP_CABLE	8
LDO_3V3, LDO_1V8A, LDO_1V8D, LDO_BMC, VIN_3V3, VOUT_3V3, VDDIO, HV_GATE1, HV_GATE2	6
Component GND	10

11.1.9 Void Via Placement

The void under the SN1804044ZBHR device is used to via out I/O and for thermal relief vias. A minimum of 6 vias must be used for thermal dissipation to the GND planes. The thermal relief vias must be placed on the right side of the device by the power path. Figure 102 shows the recommended placement of the vias. Note the areas under the void where vias are not placed which is done to allow the external FET gate drive and sense pins to route under the SN1804044ZBHR device through an inner layer. Figure 103 shows the top layer GND pour to connect the vias and GND balls together.

11.1.10 Top Layer Routing

When the components are routed, the rest of the area can be used to route all of the additional I/O. After all nets have been routed, place a polygonal pour underneath to connect the SN1804044ZBHR GND pins to the GND vias. Refer to Figure 104 for the final top routing and GND pour.

11.1.11 Inner Signal Layer Routing

The inner signal layer is used to route the I/O from the internal balls of the SN1804044ZBHR device and the external FET control and sensing. Figure 105 shows how to route the internal layer.

11.1.12 Bottom Layer Routing

The bottom layer has most of the components placed and routed already. Place a polygon pour to connect all of the GND nets and vias on the bottom layer (see Figure 106).

11.2 Layout Example

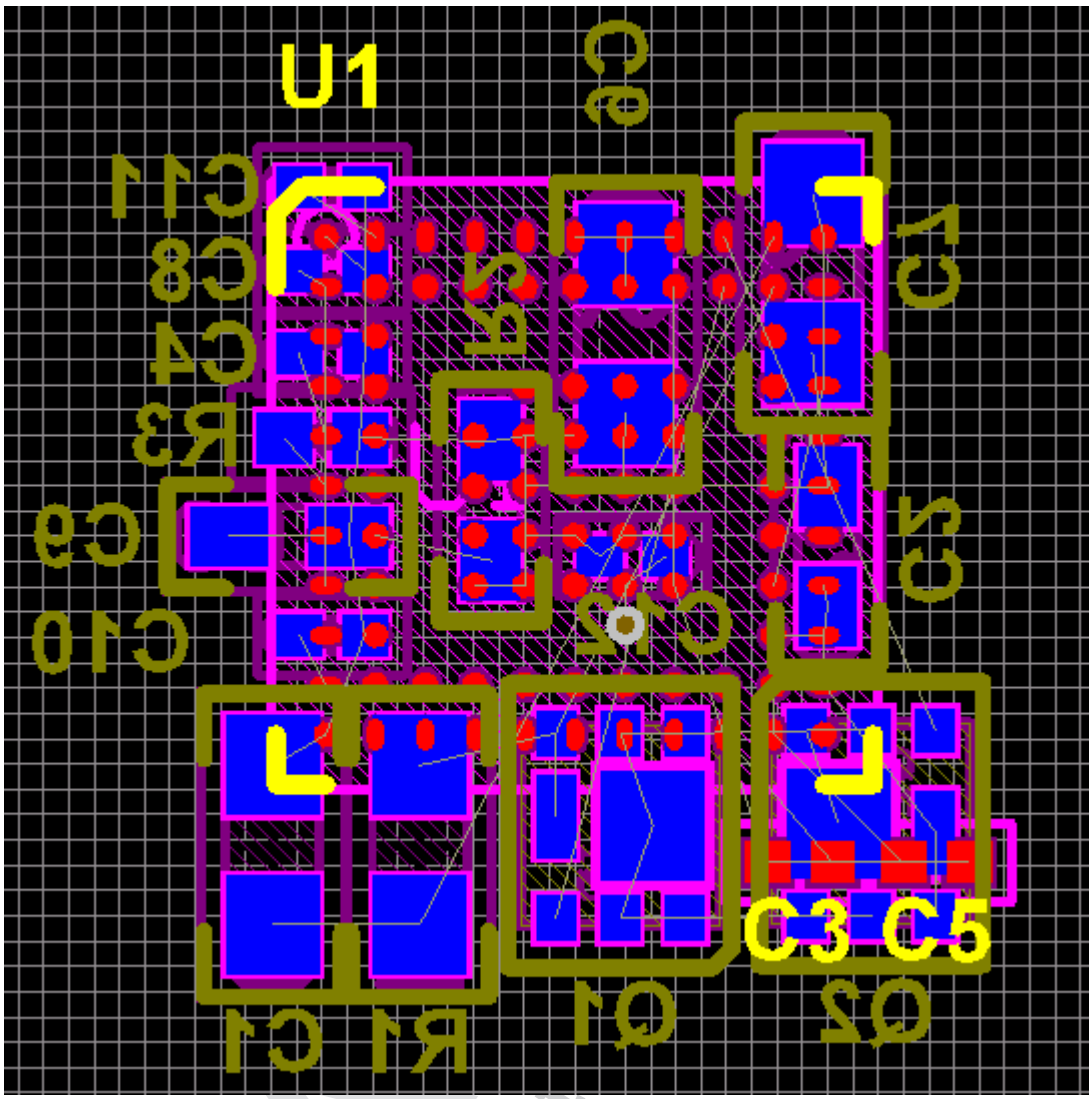


Figure 93. Example Layout (Top View in 2-D)

Layout Example (continued)

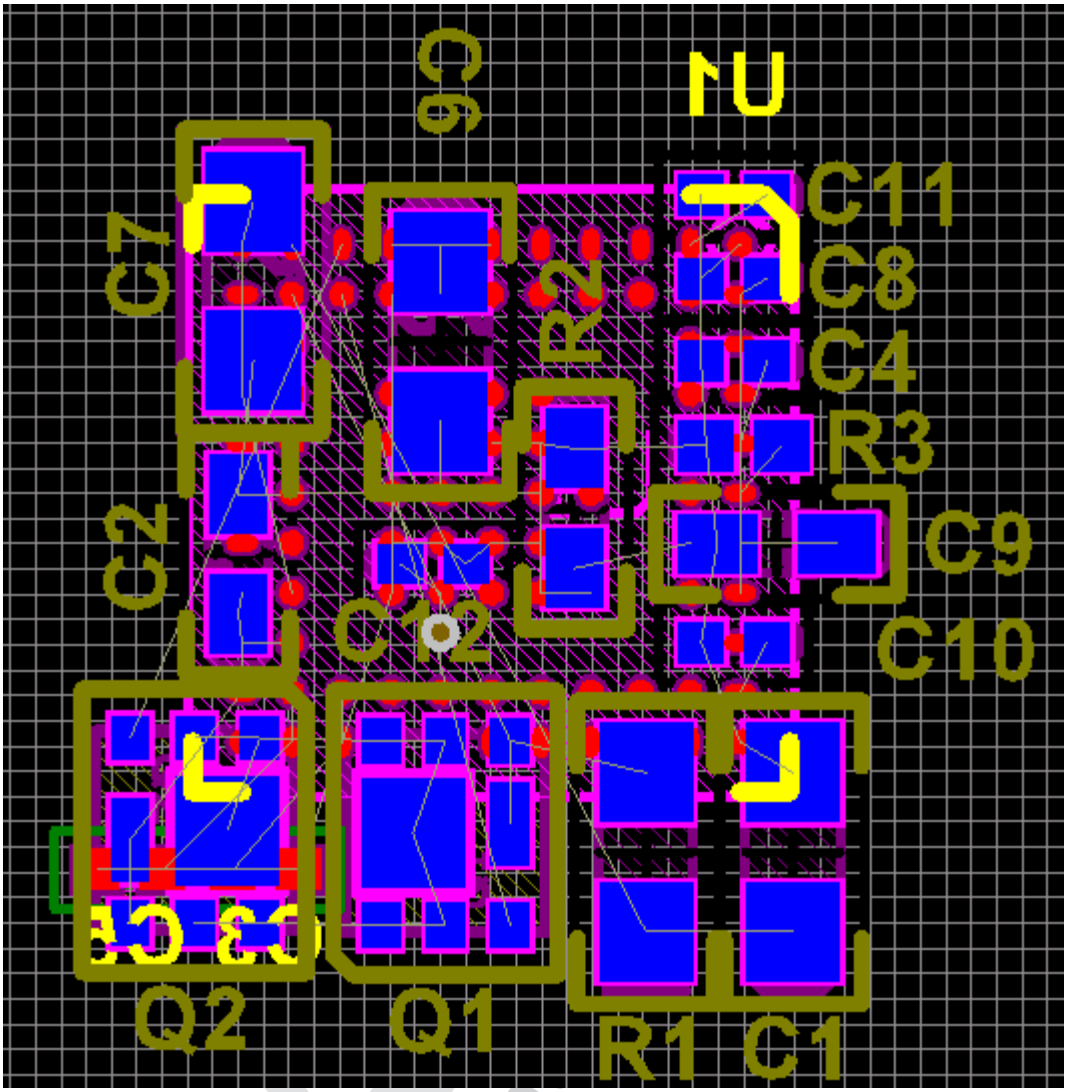


Figure 94. Example Layout (Bottom View in 2-D)

Layout Example (continued)

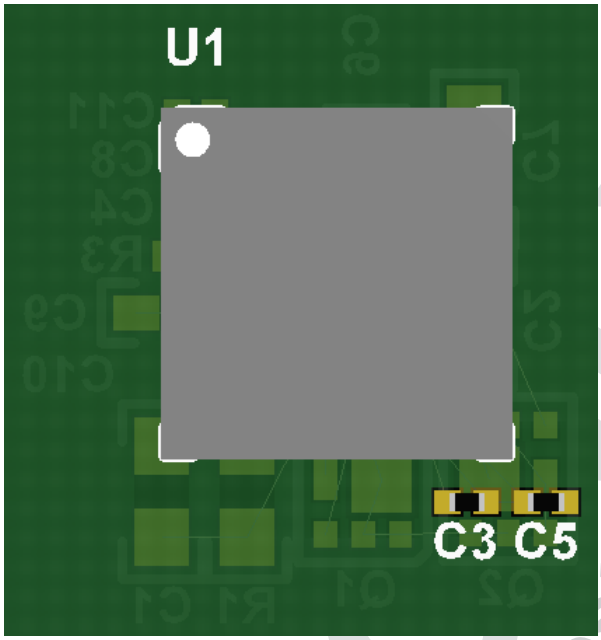


Figure 95. Example Layout (Top View in 3-D)

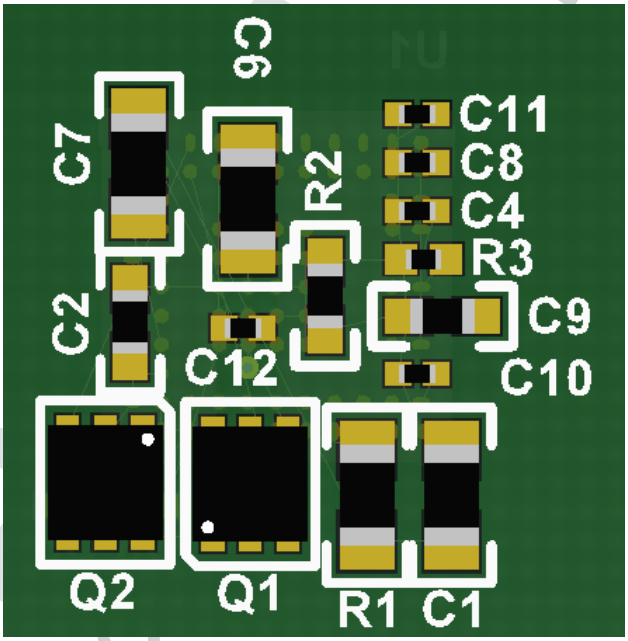


Figure 96. Example Layout (Bottom View in 3-D)

Layout Example (continued)

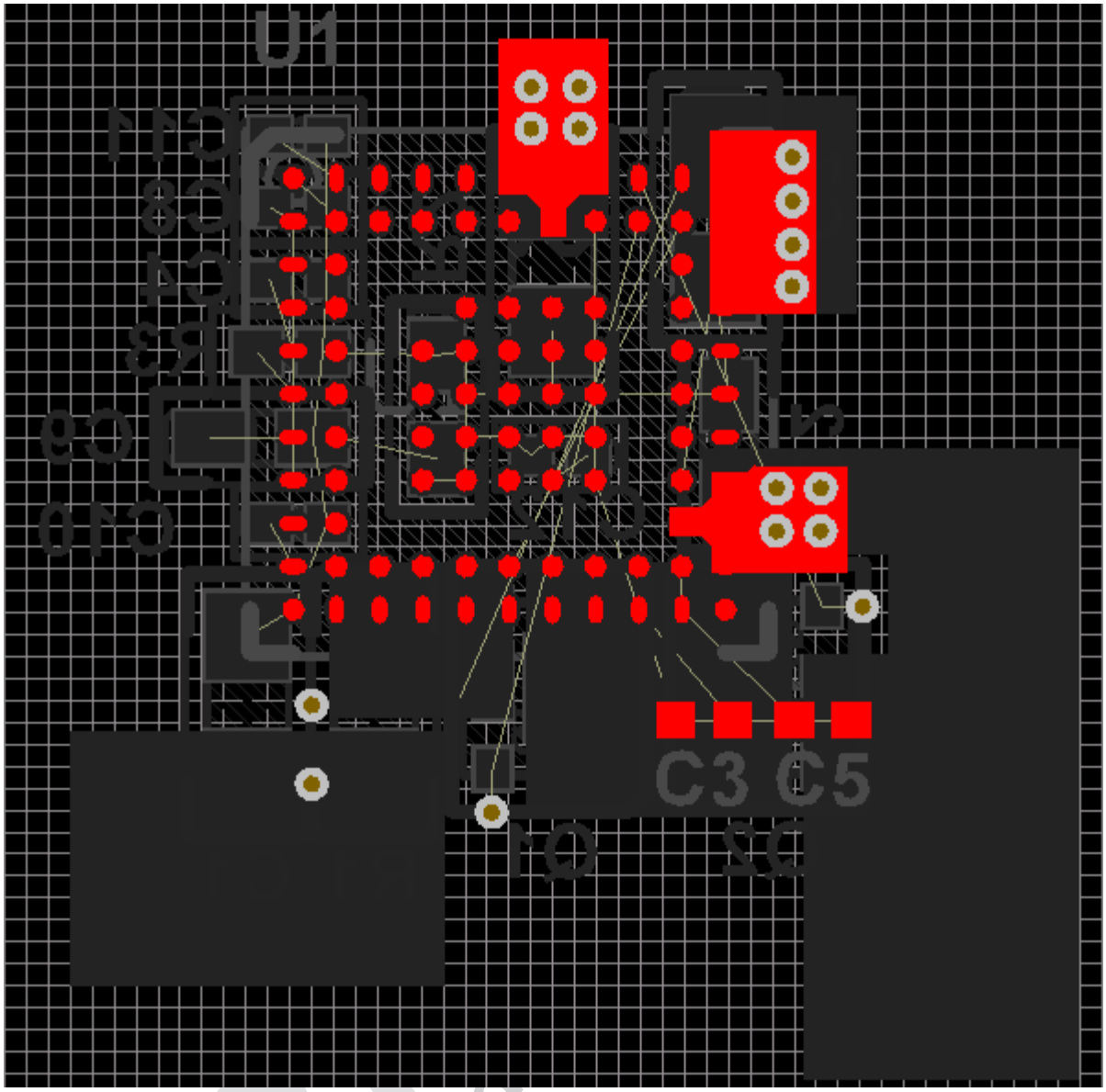


Figure 97. Top Polygonal Pours

Layout Example (continued)

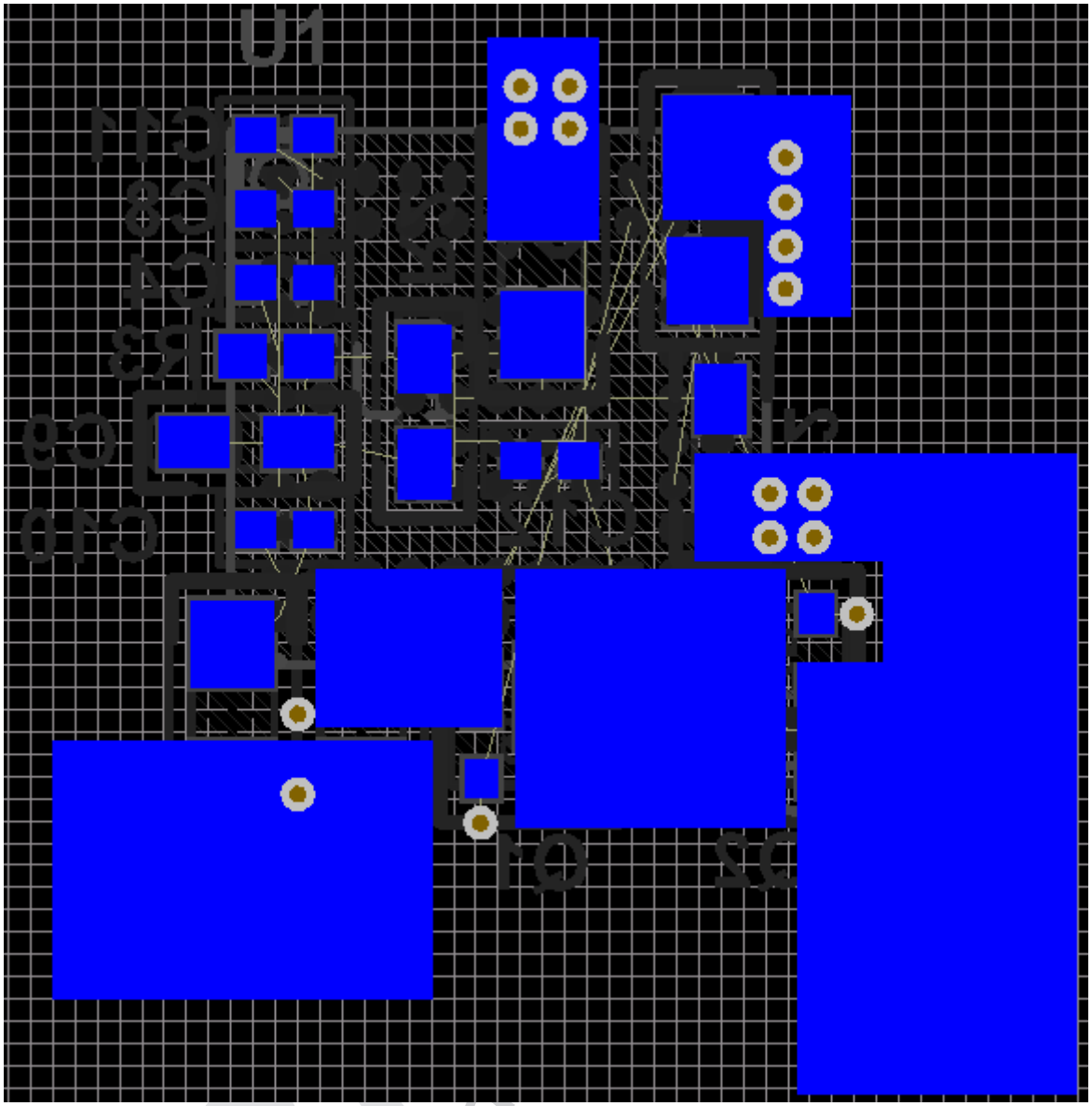


Figure 98. Bottom Polygonal Pours

Layout Example (continued)

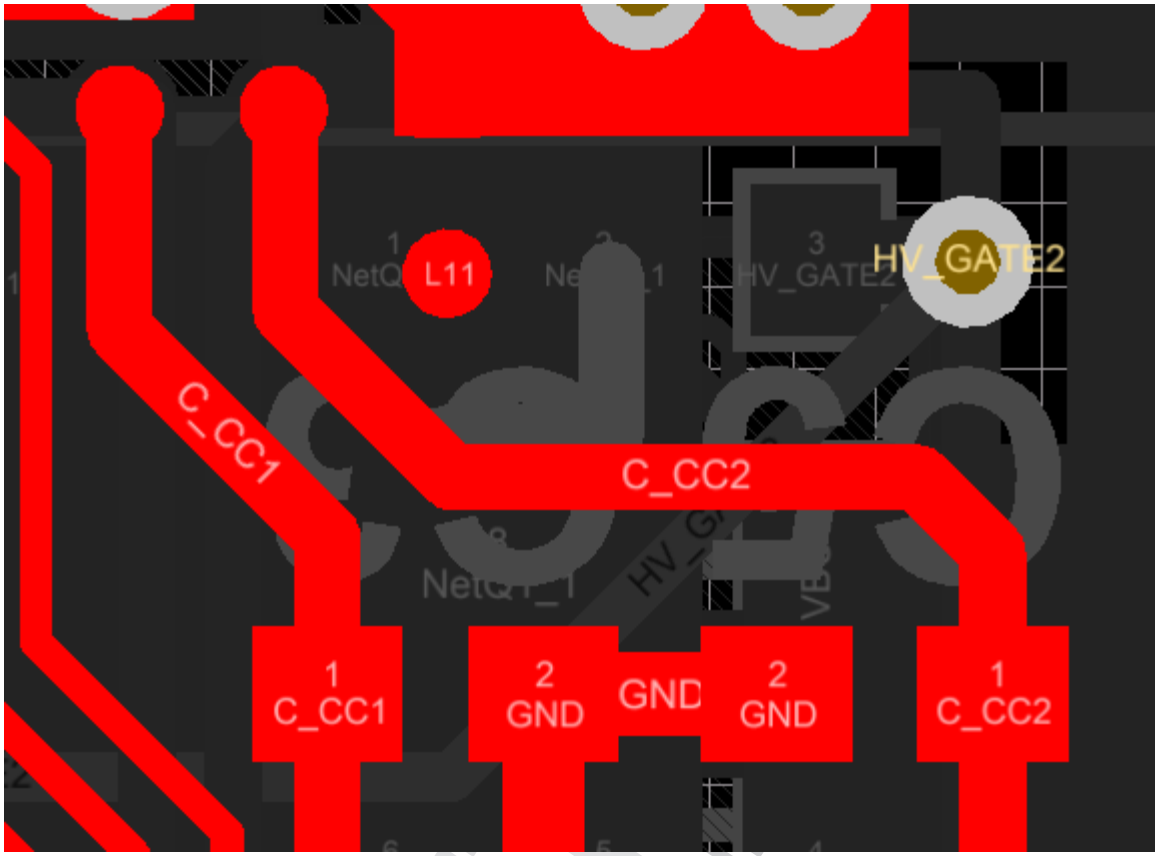


Figure 99. CC1 and CC2 Capacitor Routing

Layout Example (continued)

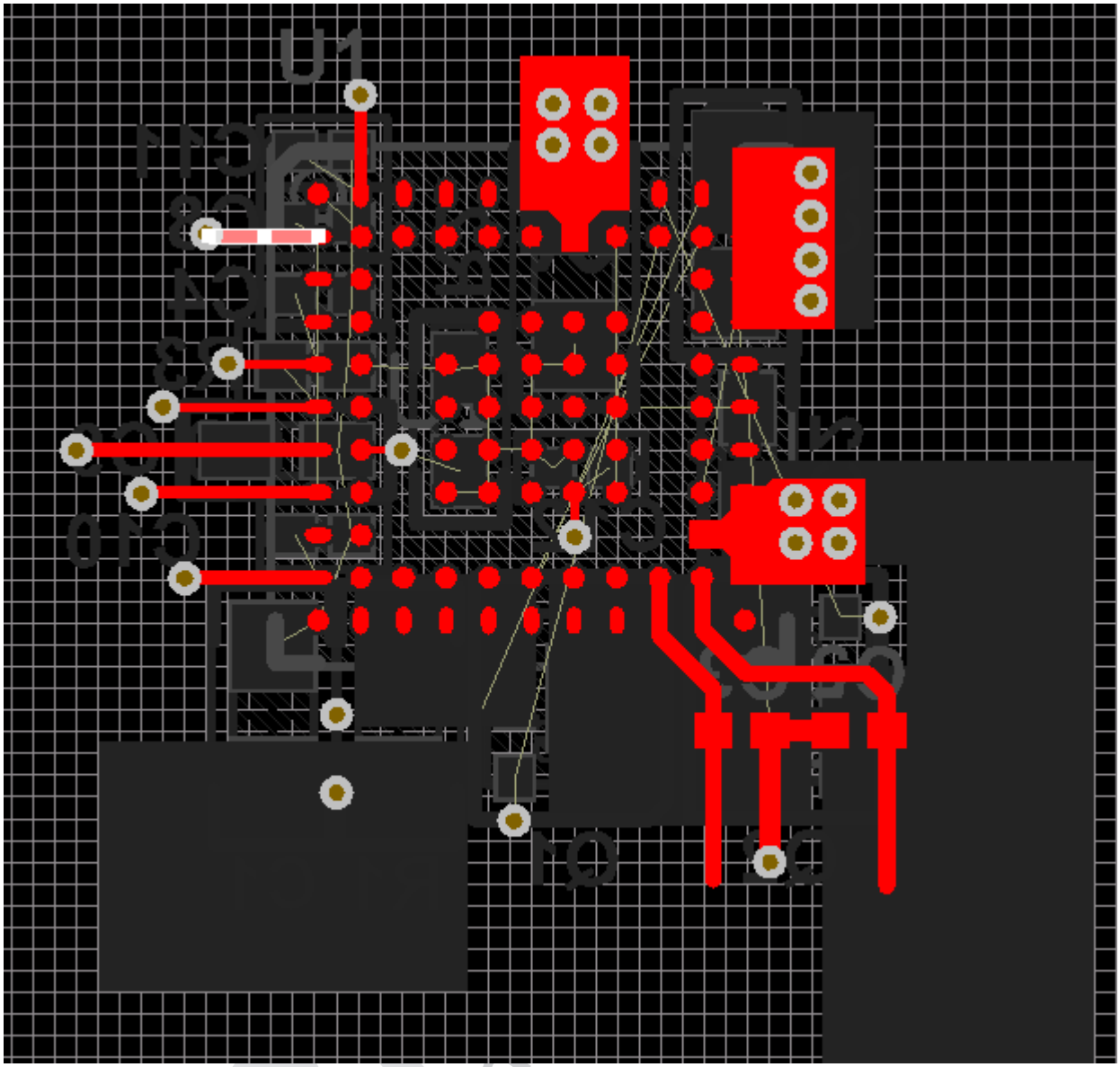


Figure 100. Top Layer Component Routing

Layout Example (continued)

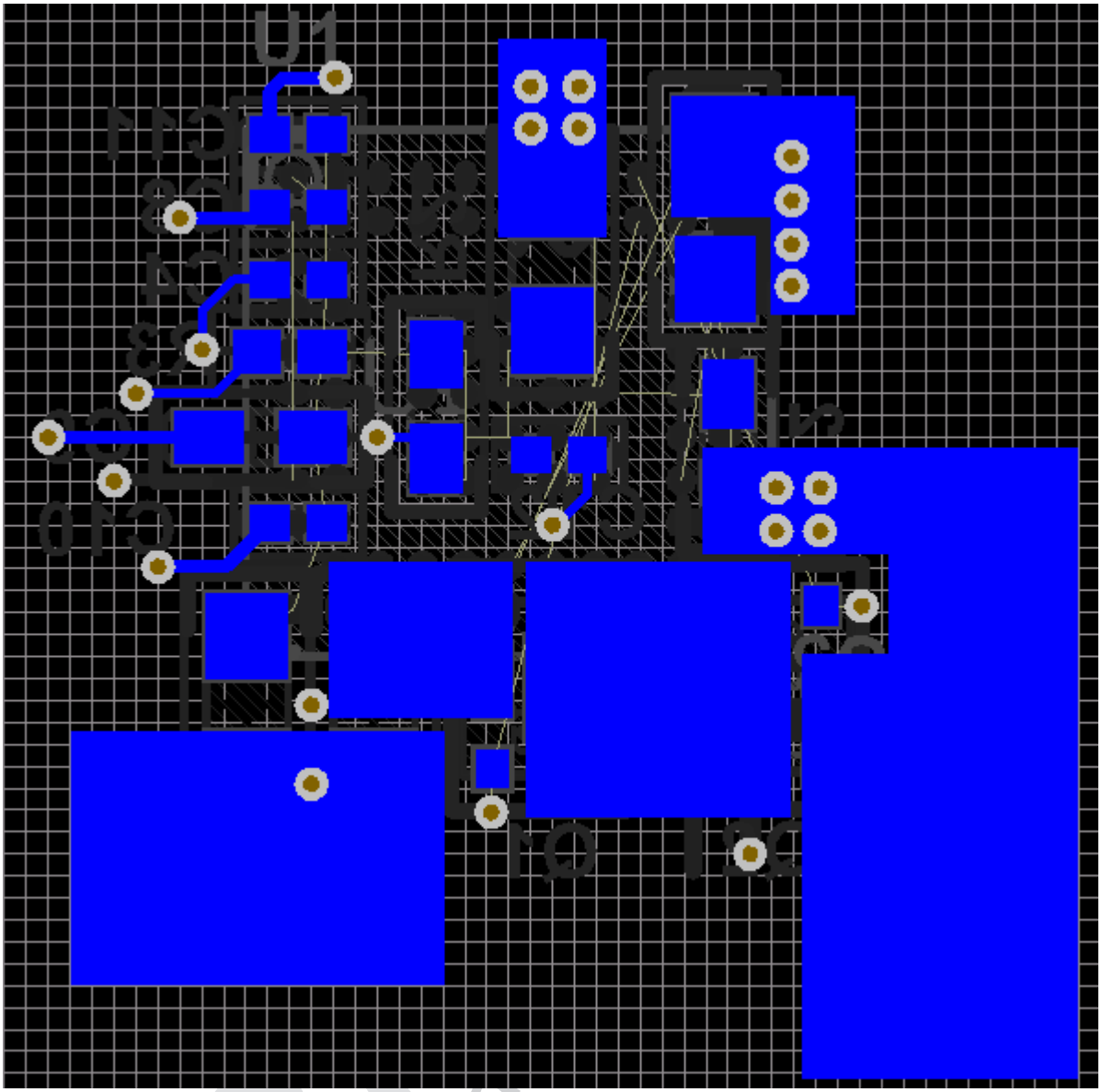


Figure 101. Bottom Layer Component Routing

Layout Example (continued)

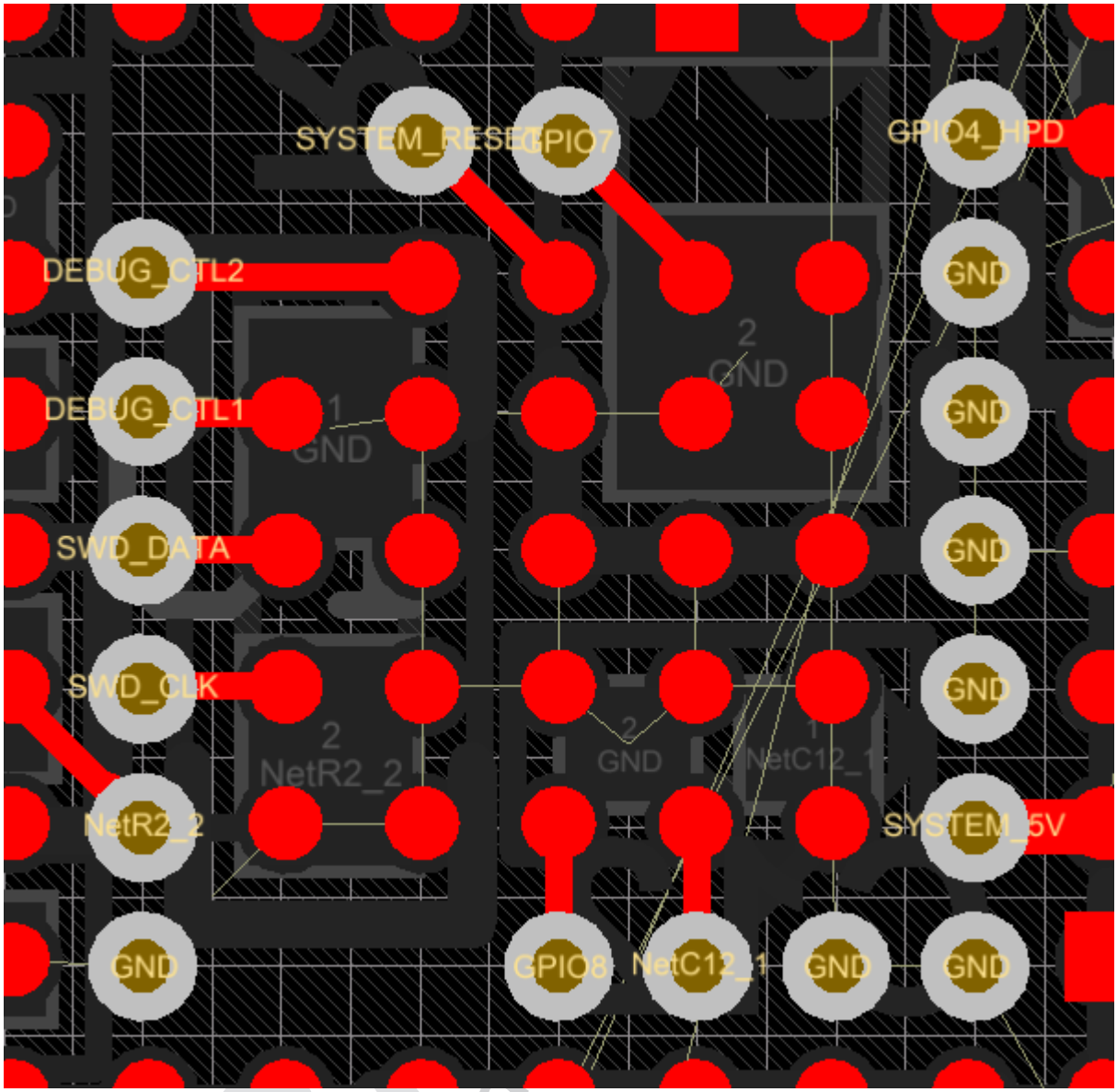


Figure 102. Void Via Placement

Layout Example (continued)

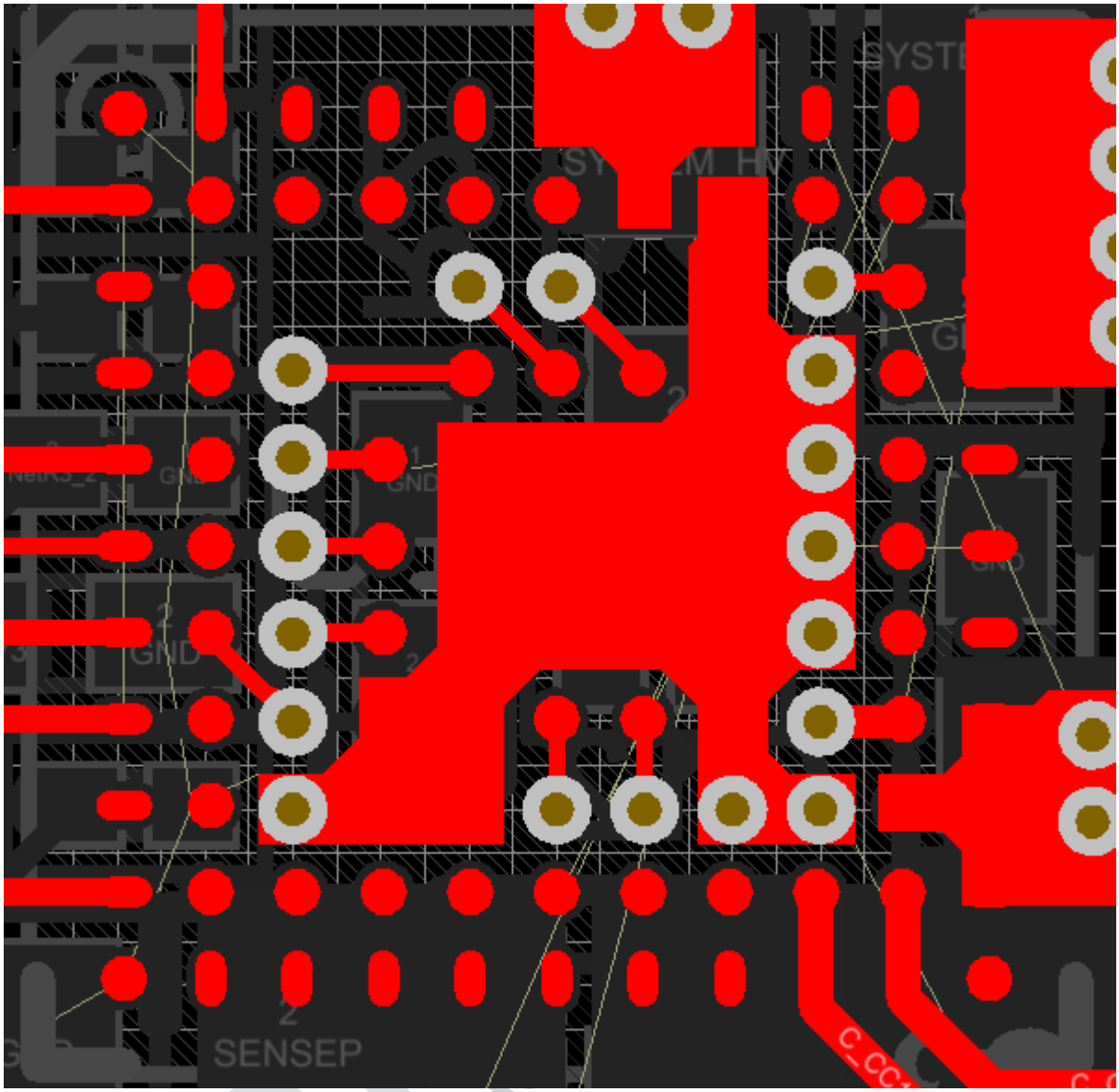


Figure 103. Top Layer GND Pour

Layout Example (continued)

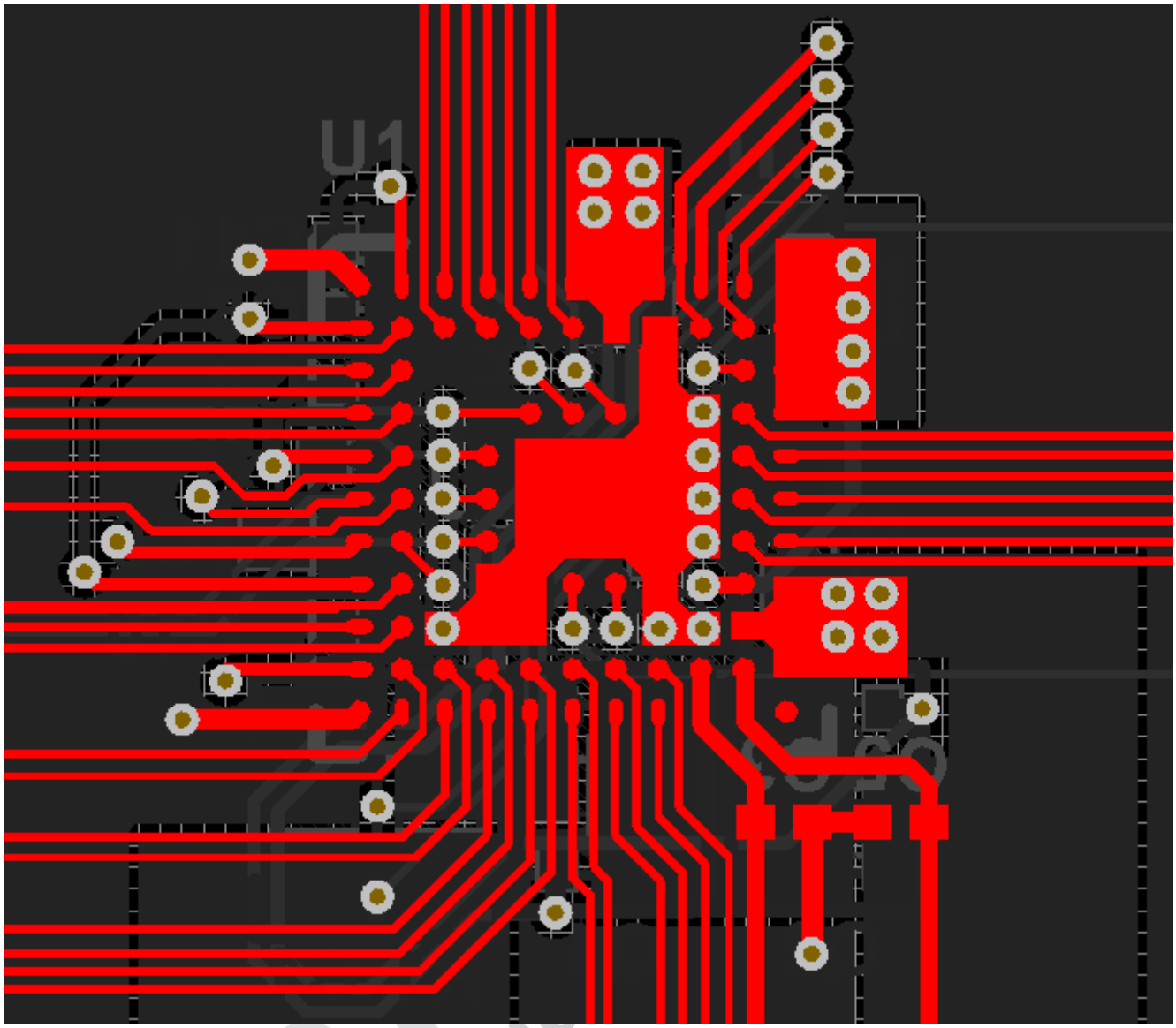


Figure 104. Final Routing and GND Pour (Top Layer)

Layout Example (continued)

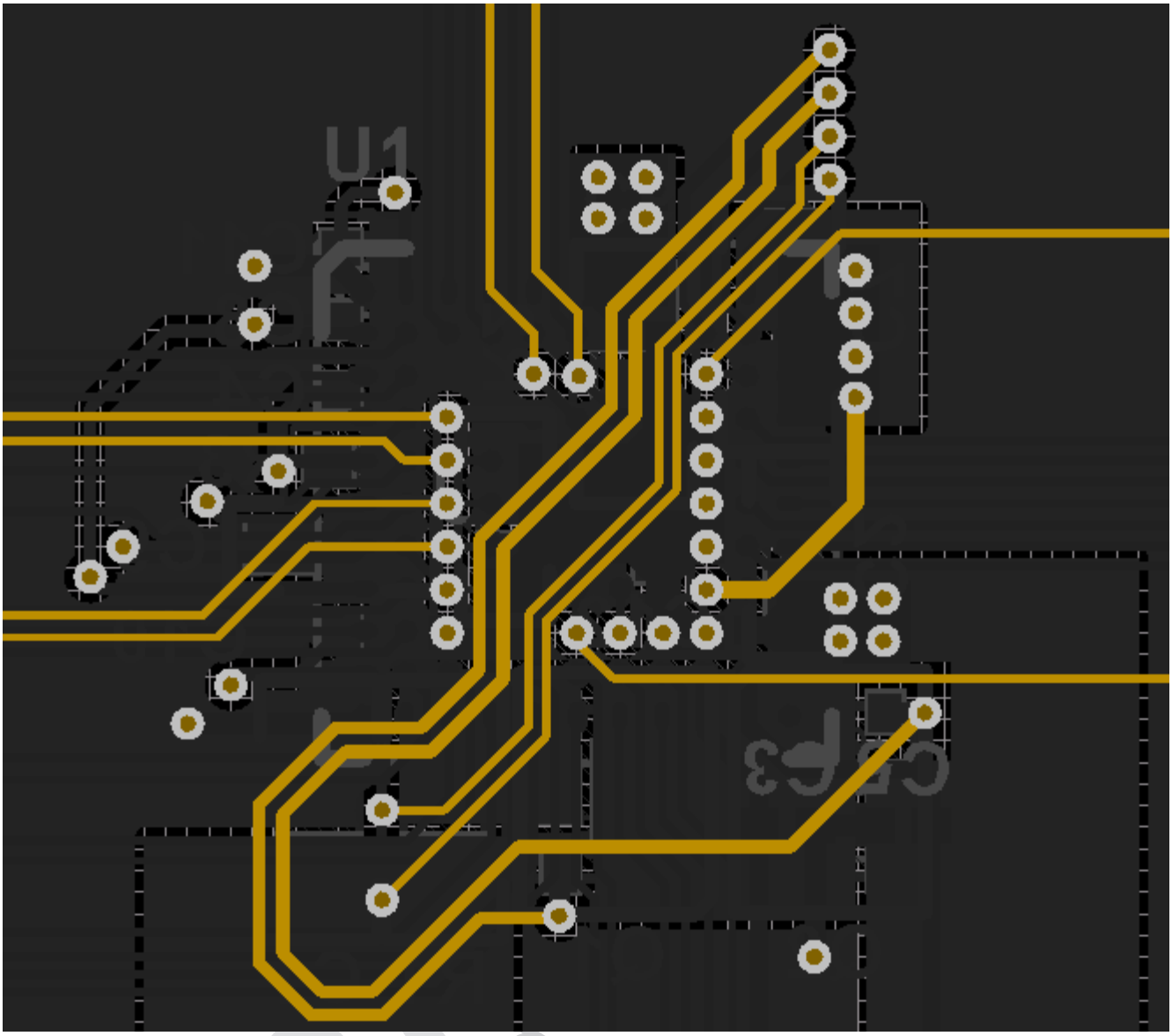


Figure 105. Final Routing (Inner Signal Layer)

Layout Example (continued)

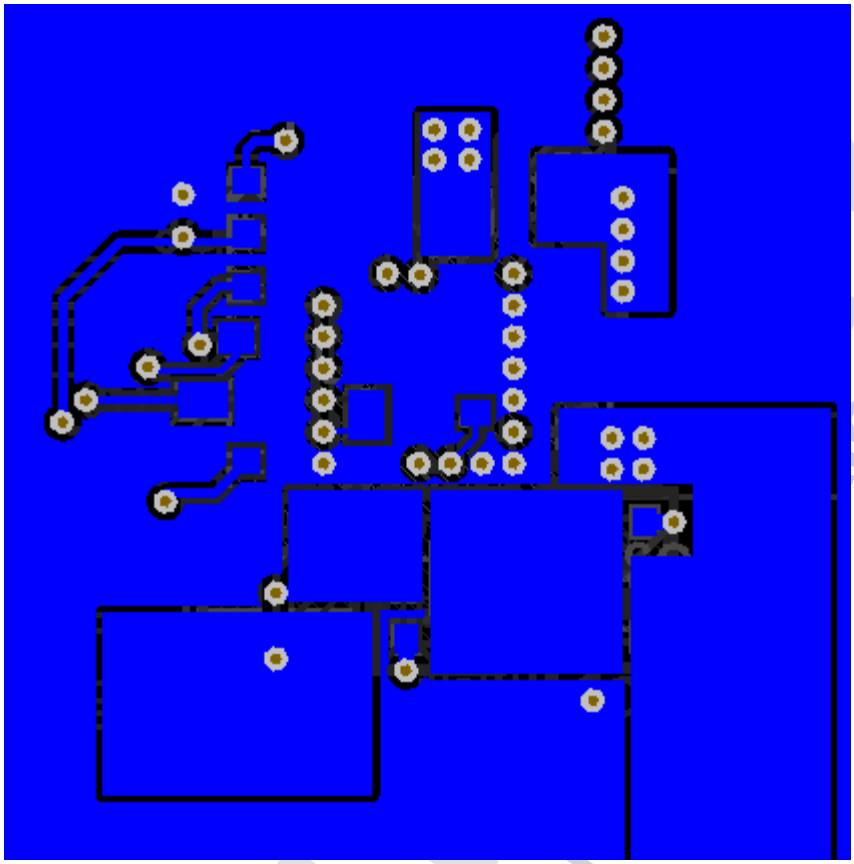


Figure 106. Final Routing (Bottom Layer)

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- NSR20F30NXT5G data sheet, *Schottky Barrier Diode*, http://www.onsemi.com/PowerSolutions/product.do?id=NSR20F30NX
- Texas Instruments, *Firmware User's Guide*
- Texas Instruments, *Host Interface Technical Reference Manual*
- USB Power Delivery Specification Revision 2.0, V1.1 (May 7th, 2015)
- USB Type-C Specification Release 1.1 (April 3rd, 2015)
- USB Battery Charging Specification Revision 1.2 (December 7th, 2010)
- W25X05CL data sheet, *2.5 / 3 / 3.3 V 512K-Bit Serial Flash Memory With 4KB Sectors and Dual I/O SPI*, www.winbond.com/hq/product/code-storage-flash-memory/serial-nor-flash/?__locale=en&partNo=W25X05CL

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
Thunderbolt is a trademark of Intel.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 Package Option Addendum

13.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking(4)(5)
SN1804044ZBHR	ACTIVE	NFBGA	ZBH	96	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-10 to 85	TPS65982 DD

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

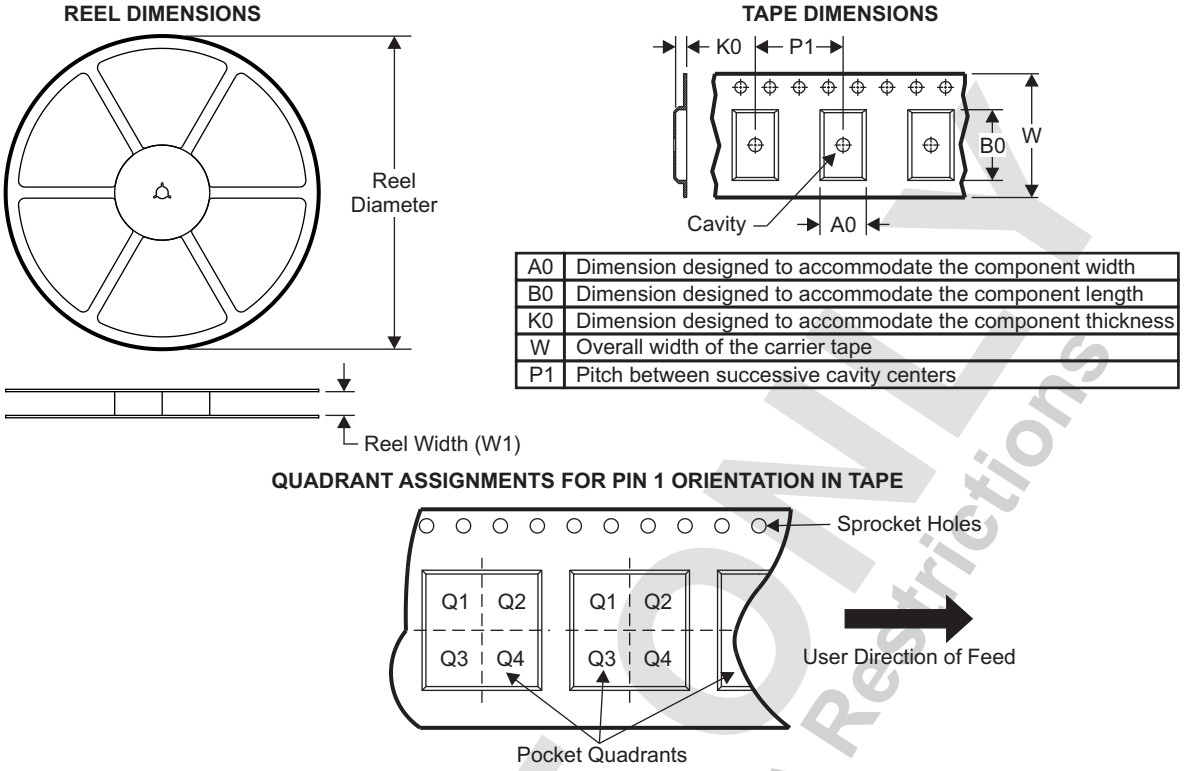
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

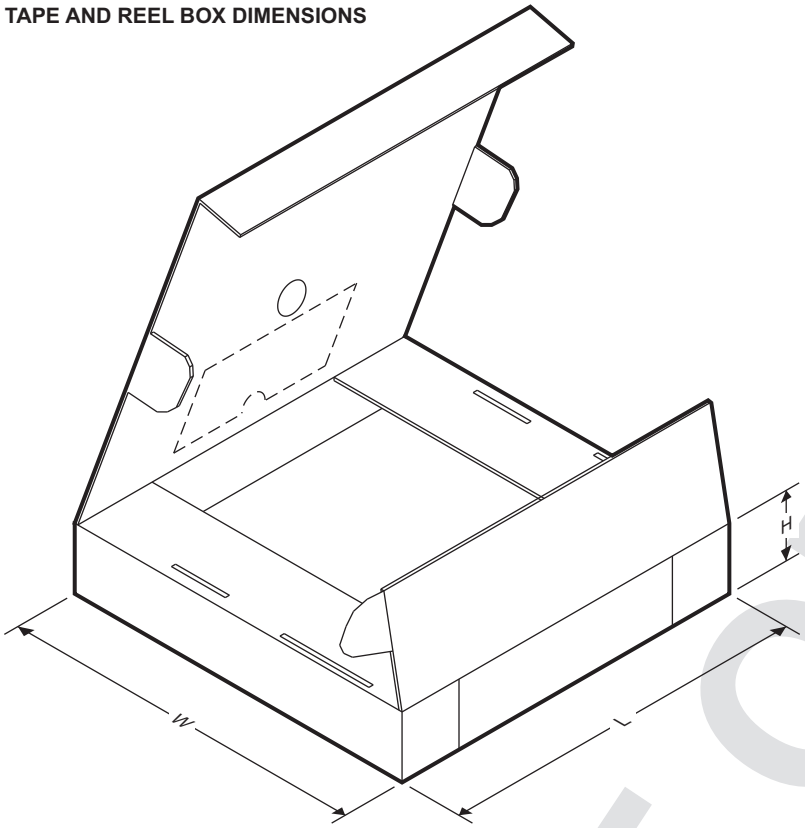
13.1.2 Tape and Reel Information



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN1804044ZBHR	NFBGA	ZBH	96	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



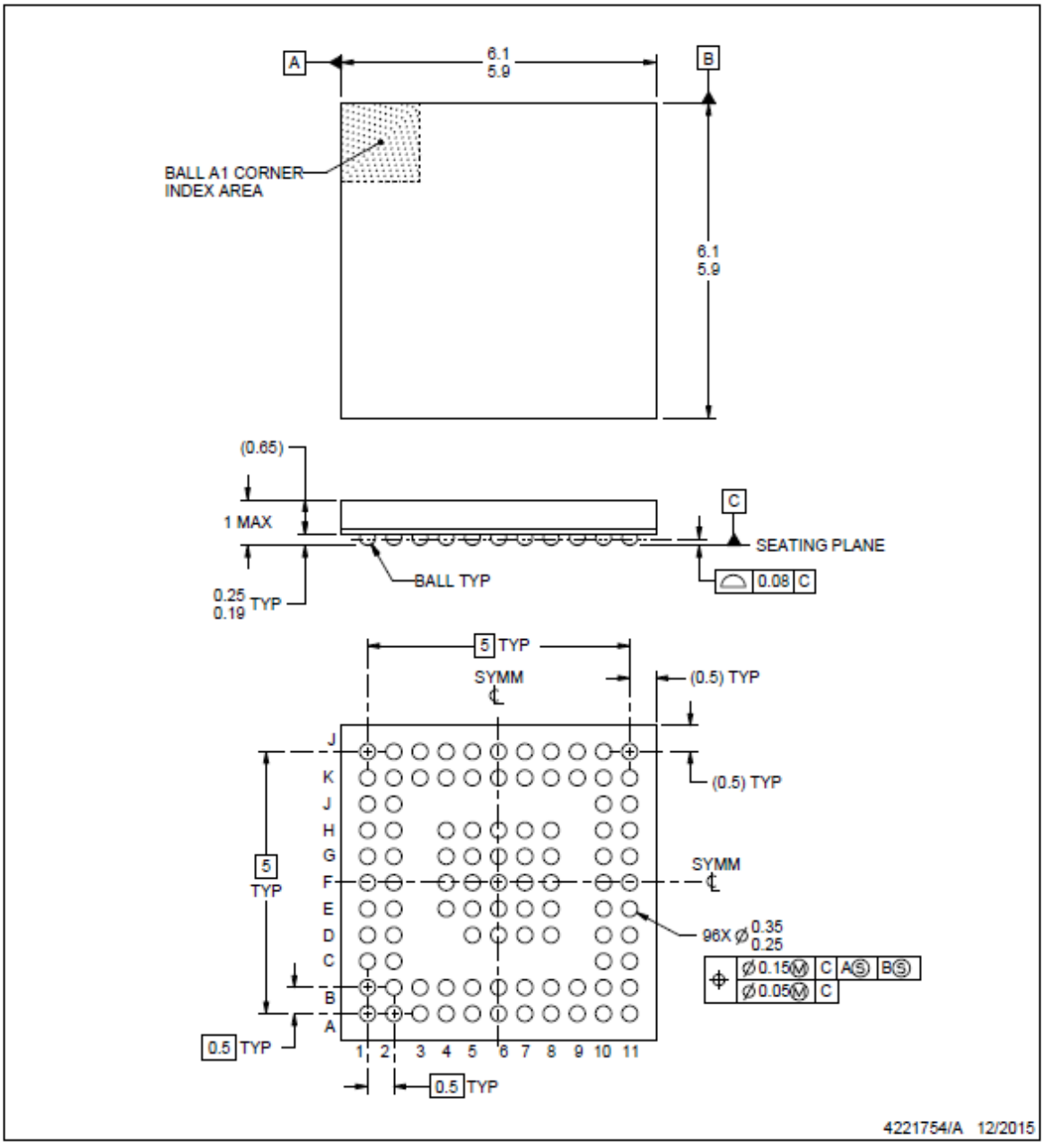
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN1804044ZBHR	NFBGA	ZBH	96	2500	336.6	336.6	31.8

PACKAGE OUTLINE

ZBH0096A

NFBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



NOTES:

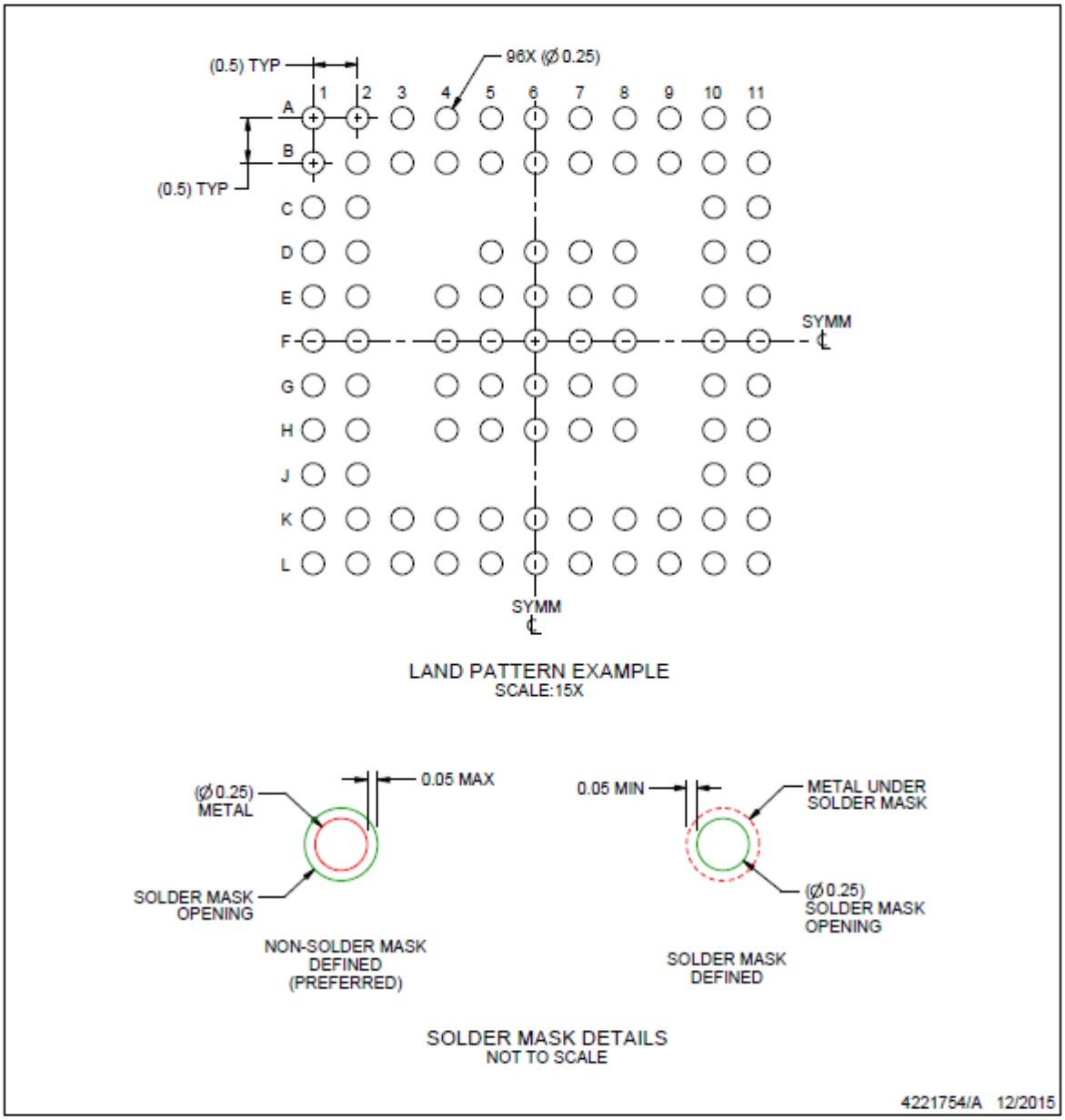
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

PRODUCT PREVIEW

EXAMPLE BOARD LAYOUT

ZBH0096A — **NFBGA - 1 mm max height**

PLASTIC BALL GRID ARRAY



NOTES: (continued)

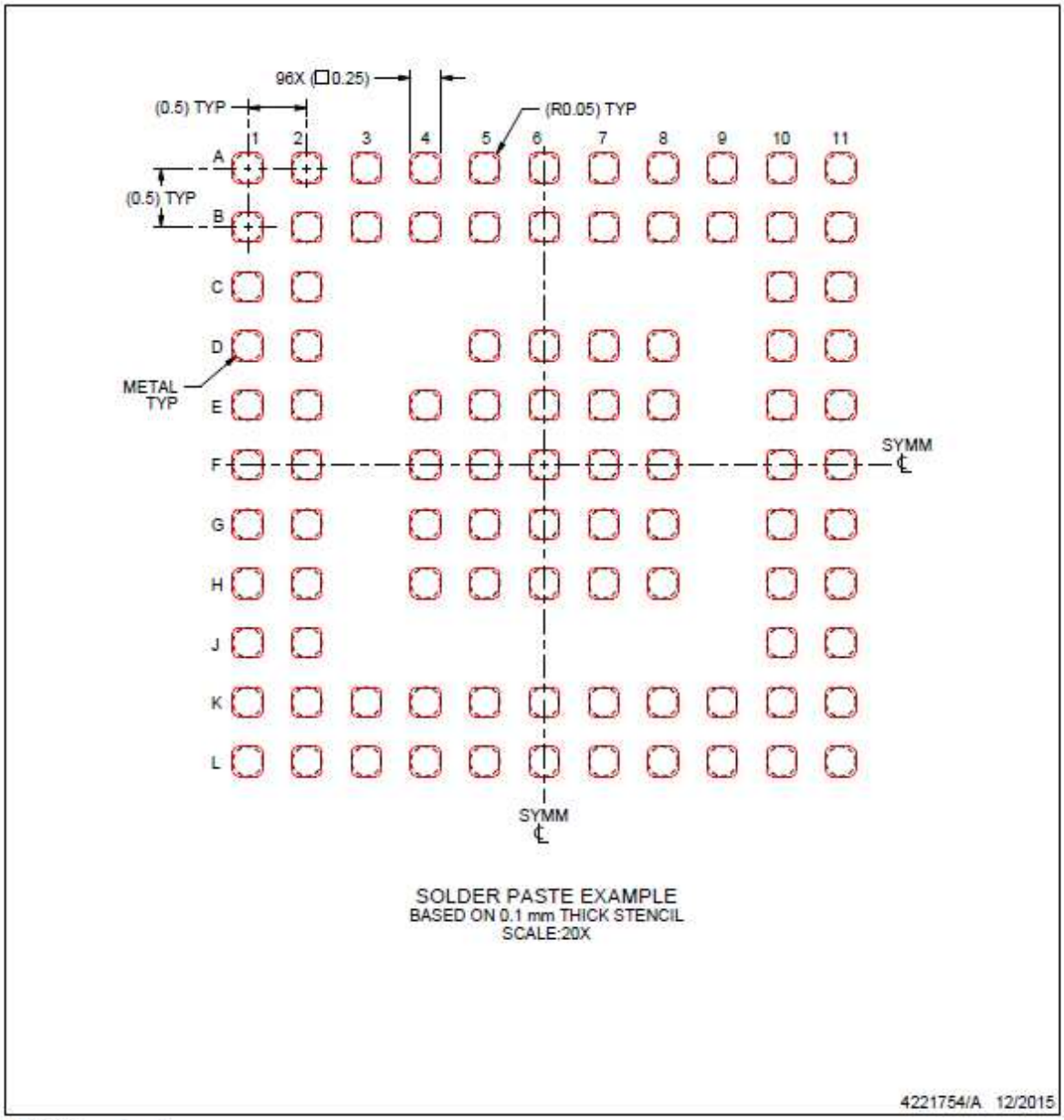
4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

EXAMPLE STENCIL DESIGN

ZBH0096A

NFBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:20X

4221754/A 12/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PRODUCT PREVIEW

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agrees that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their systems and products, and have full and exclusive responsibility to assure the safety of their products and compliance of their products (and of all TI products used in or for such Designers' products) with all applicable regulations, laws and other applicable requirements. Designers represent that, with respect to their applications, they have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designers agree that prior to using or distributing any systems that include TI products, they will thoroughly test such systems and the functionality of such TI products as used in such systems.

TI's provision of reference designs and any other technical, applications or design advice, quality characterization, reliability data or other information or services does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such reference designs or other items.

Designers are authorized to use, copy and modify any individual TI reference design only in connection with the development of end products that include the TI product(s) identified in that reference design. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of the reference design or other items described above may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS AND OTHER ITEMS DESCRIBED ABOVE ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNERS AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS AS DESCRIBED IN A TI REFERENCE DESIGN OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265