**Texas Instruments**

**Analog EVM Test Procedure**

**TFP401PZPEVM HDSDC010 Test Procedure**

**Rev. A**

1. **GENERAL**
   1. **PURPOSE**

* + 1. To provide detailed instructions for testing TFP401PZPEVM.
  1. **SCOPE**
     1. Covers complete instructions for testing TFP401PZPEVM. All of the control inputs are selectable via DIP Switch configuration. The devices should be tested using a programmable video signal generator, this guide was generated considering the model: *MSPG-925SM* . A external power through 3.3V DC IN is required.
  2. **REFERENCE DOCUMENTATION**
     1. HSDC010 \_Schematic.DSN
     2. HSDC010 \_PCB.pdf
     3. HSDC010 \_UserGuide.doc
  3. **MATERIALS**
     1. N/A

* 1. **DEFINITIONS**
     1. EVM – Evaluation Module / board
     2. DVI – Digital Visual Interface

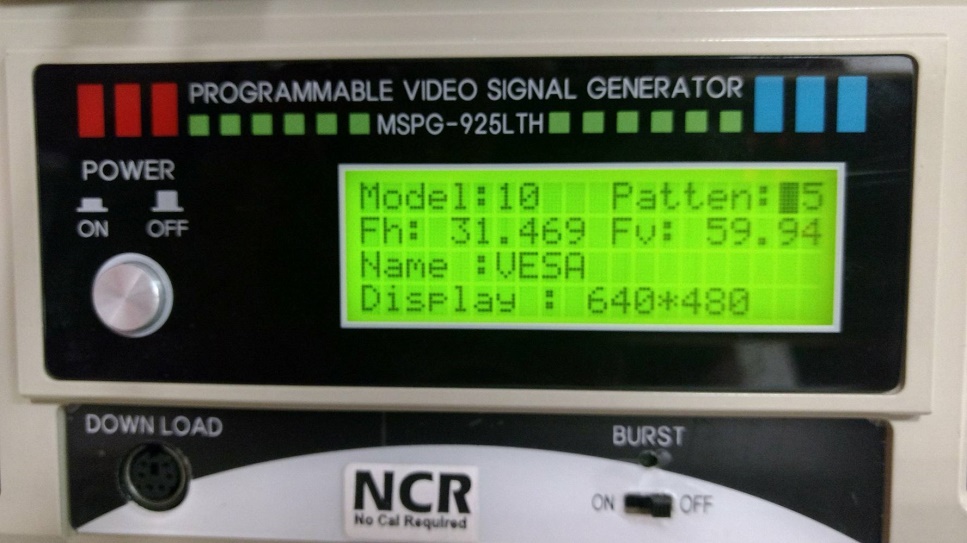
1. **SAFETY**
   1. This test must be performed by qualified personnel trained in electronics theory and understand the risks and hazards of the assembly to be tested.
   2. ESD precautions must be followed while handling electronic assemblies while performing this test.
   3. Precautions should be observed to avoid touching areas of the assembly that may get hot or present a shock hazard during testing.
2. **QUALITY**
   1. Test data or reports shall be made available upon request by Texas Instruments.
3. **APPAREL**
   1. Electrostatic smock
   2. Electrostatic Gloves or finger cots
   3. Safety Glasses
   4. Ground ESD wrist strap.
4. **EQUIPMENT**
   1. **Test Option # 1**
      1. TFP401PZPEVM.
      2. Programmable video signal generator Master MSPG-925SM.
      3. Oscilloscope.
      4. 3.3V Power Supply .
      5. Banana to Banana Cables.
      6. DVI Cable.
   2. **Test Option # 2**
      1. PC with a DVI video output.
      2. TFP401PZPEVM.
      3. Oscilloscope.
      4. 3.3V Power Supply.
      5. Banana to Banana Cables.
      6. DVI Cable.
      7. Monitor with DVI input (Max resolution 1080p).
5. **TFP401PZPEVM Jumper Configuration**

Configure all Jumpers to settings in the table below:

|  |  |  |
| --- | --- | --- |
| **Reference Designator** | **JMP Control** | **Configuration** |
| J8 | AVDD supply | SHUNT (SH-J8) |
| J9 | DVDD supply | SHUNT (SH-J9) |
| J10 | OVDD supply | SHUNT (SH-J10) |
| J11 | PVDD supply | SHUNT (SH-J11) |
| J6 | PDO# control | SHUNT on pin 1–2 (SH-J6) |

|  |  |  |
| --- | --- | --- |
| **SW2 Switch Section** | **Function** | **Configuration** |
| 1 | DFO | ON (LOW) |
| 2 | PD# | OFF (HIGH) |
| 3 | ST | ON (LOW) |
| 4 | PIXS | ON (LOW) |
| 5 | STAG# | OFF (HIGH) |
| 6 | PDO# | OFF (HIGH) |
| 7 | OCK\_INV | ON (LOW) |
| 8 | No used | NA |

1. **Check functionality:**
   1. **Option Test # 1**
2. Connect the video signal generator to the TFP401PZPEVM through the DVI cable.
3. Connect a 3.3V power supply to P1 and P2 to GND.
4. Configure the video signal generator:
   1. Model: 10
   2. Pattern: 15
   3. Fh: 31.469 Hz
   4. Fv: 60 Hz
   5. Resolution: 640X480



F igure 1. Video Signal Generator

1. Use the oscilloscope to measure the frequency of the following signals:

ODCK (J5.14), As we are using a resolution 640x480 for this example, the pixel rate must be 25 Mhz

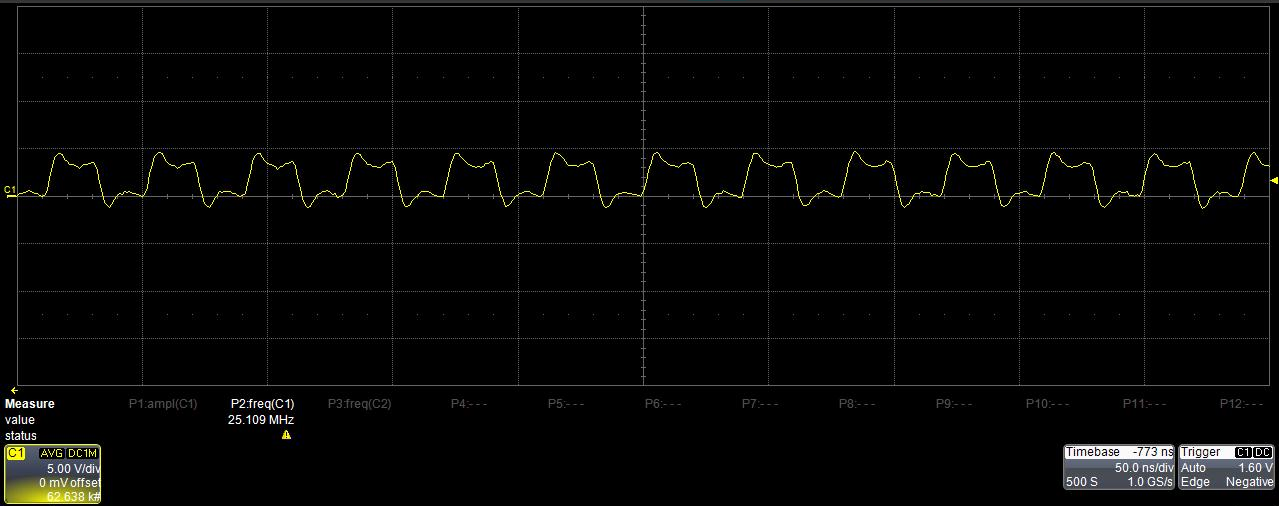


Figure 2. ODCK

Vsync (J5.10) for this example we’ll obtain a Vsync of 60 Hz

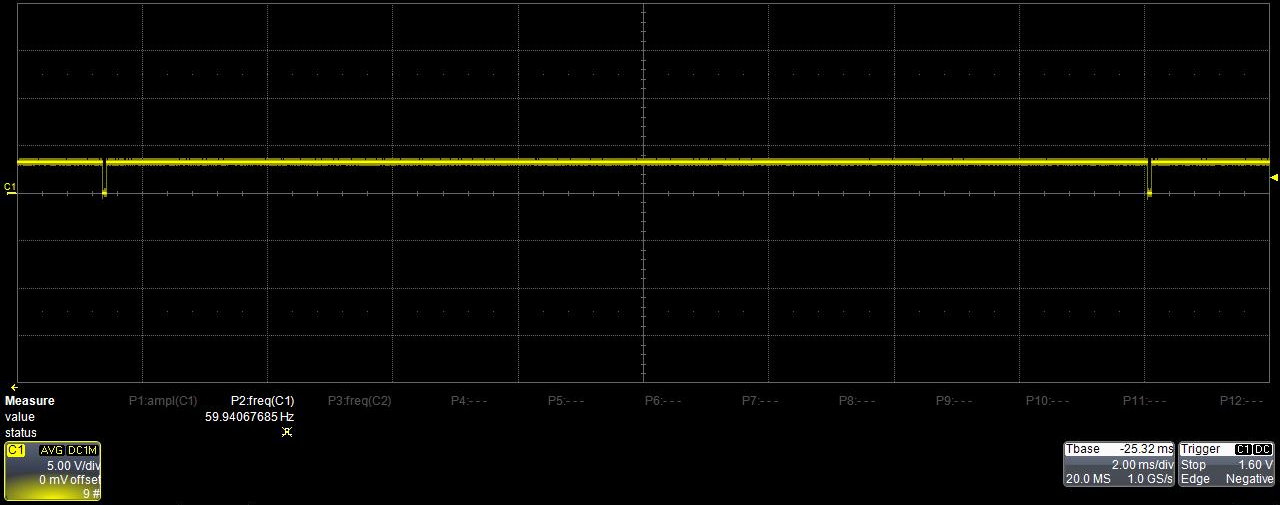


Figure 3. Vsync

Hsync(J5.12) for this example we’ll obtain a Hsync of 31.48 Hz

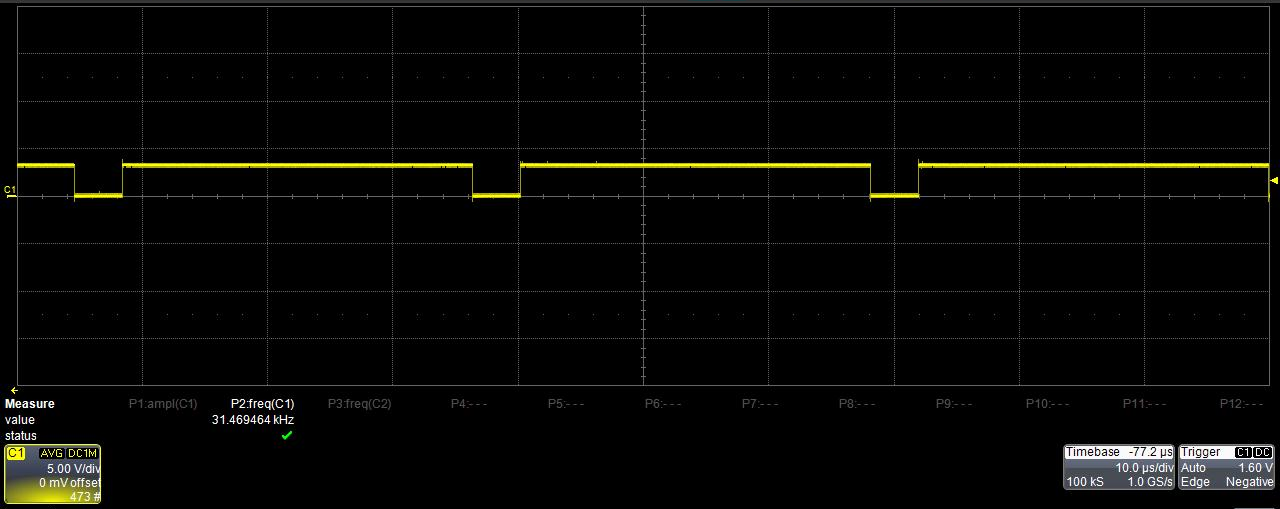


Figure 4. Hsync

DE(J5.8) for this example we’ll obtain a DE of 31.46 Hz

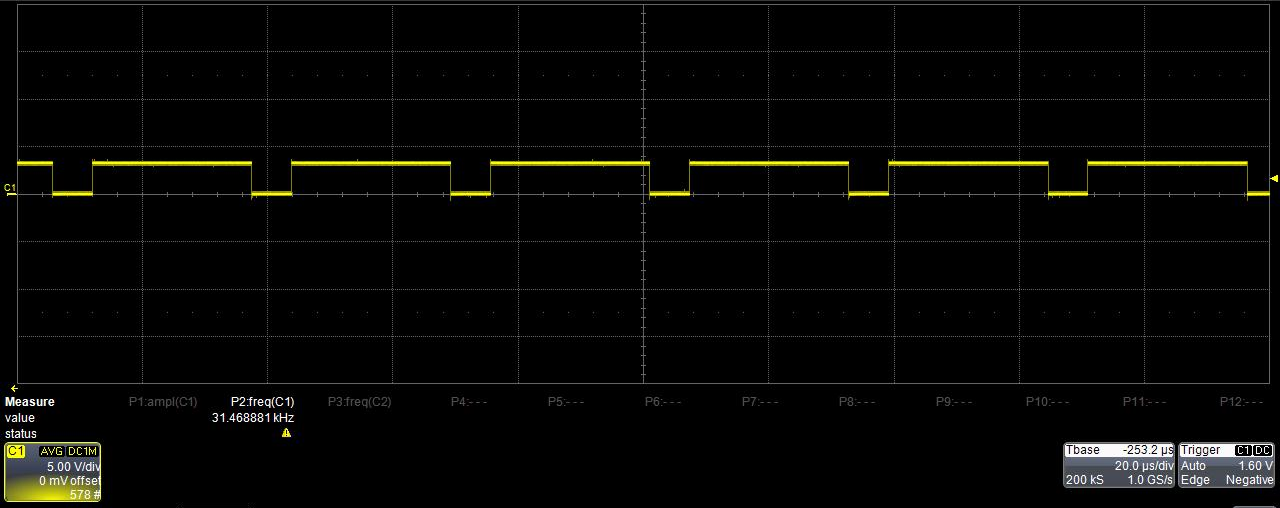


Figure 5. DE

1. Disable the Red pixels and monitor a low state in the following terminals.
2. J3: 9, 11, 13, 15, 18, 19, 21 and 23.
3. J14: 34, 36, 38, 40, 42, 44, 46 and 48.
4. Disable the Green pixels and monitor a low state in the following terminals.
5. J3: 25, 27, 29, 31, 33, 35, 37 and 39.
6. J14: 18, 20, 22, 24, 26, 28, 30 and 32.
7. Disable the Blue pixels and monitor a low state in the following terminals.
8. J3: 41, 43, 45, 47, 49, 51, 53 and 55.
9. J14: 2, 4, 6, 8, 10, 12, 14 and 16.
10. Disconnect the DVI cable and confirm that the J6.3 terminal is low.
    1. **Option Test # 2**
11. Connect the DVI Monitor to the PC.
12. Connect a 3.3V power supply to P1 and P2 to GND of the TFP401PZPEVM
13. Turn on the PC and check that the Monitor is displaying correctly.
14. Disconnect the DVI cable from the monitor and connect it to the TFP401PZPEVM (J3). Do not disconnect the DVI cable from the PC.
15. Use the oscilloscope to measure the frequency of the following signals:

ODCK (J5.14). This frequency of this signal must match with the panel pixel rate. For example: 108MHz

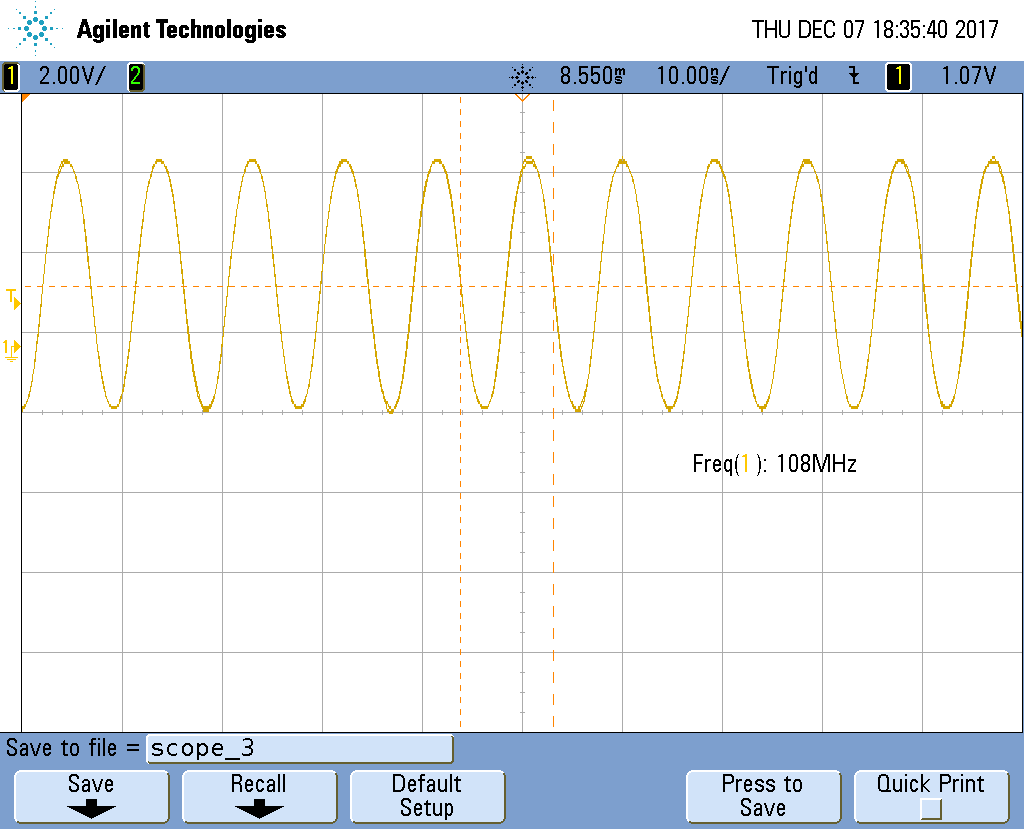


Figure 6. ODCLK

Vsync (J5.10) The frequency of this panel should be the refresh rate of the Monitor. For example: 60 Hz

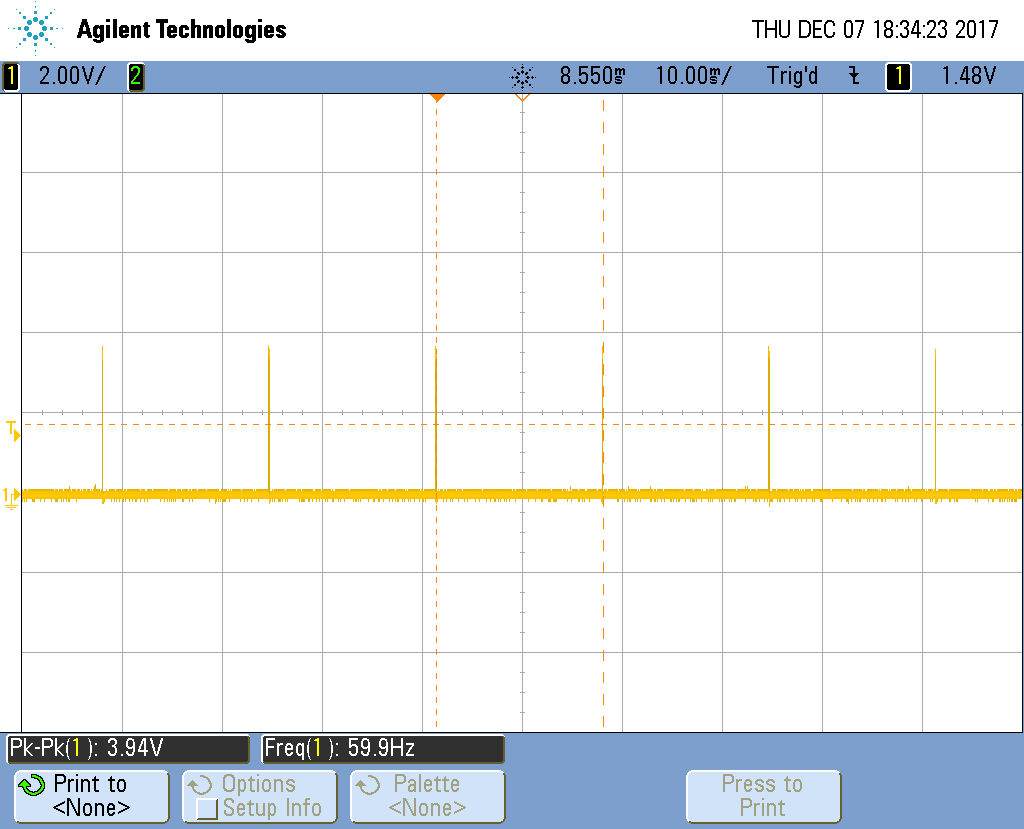


Figure 7. Vsync

1. **MATERIAL DISPOSITION & TRANSFER**

**8.1** CONFORMING MATERIAL

Units that have passed this test procedure shall be packaged into anti-static ESD approved bags, labeled with two labels according to the table below, and shipped per the P.O.

|  |  |
| --- | --- |
| **Label 1**  **Assembly Number+Dash Number if Applicable** | **Label 2**  **IC Number** |
| HSDC010 | TFP401PZP |
|  |  |

* 1. NON-CONFORMING MATERIAL

If yield loss is 2% or less, scrap non-conforming units and adjust P.O. to reflect total amount shipped. If yield loss approaches or exceeds 5%, contact EVM coordinator for assistance.