SMSC USB3320 vs TUSB1210

Ver1.2 28July 2010

TUSB1210 Overview :

- TUSB1210 is TI's first single-chip stand-alone USB2.0 HS transceiver chip with ULPI interface, and master/slave mode clock capability allowing it to be seamlessly connected with OMAP24xx and OMAP 34xx application processors or any other ULPI-interface USB2.0 HS controller device.
- TUSB1210 is available in a 32QFN package, and sampling soon !!
- TUSB1210 was designed to be pin-to-pin compatible with SMSC USB3320 device.
- However TUSB1210 is not a drop-in replacement for SMSC USB3320, some minor changes are required
- To allow a single application board to be capable of using both devices it is recommended to follow the guidelines in the following slides
- Both devices are compared for:
  - Block Diagram
  - Pinout
  - Application Diagram
    1. ULPI input clock mode
    2. ULPI output clock mode (REFCLK = 26MHz)
    3. ULPI output clock mode (REFCLK = 19.2MHz)
  - Package

SMSC3320 vs TUSB1210: Block Diagram

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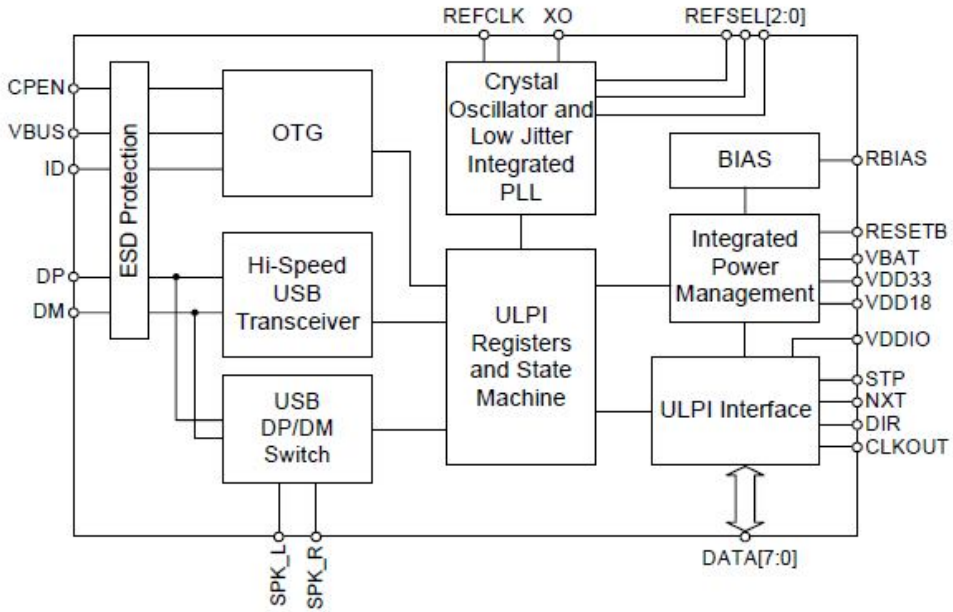
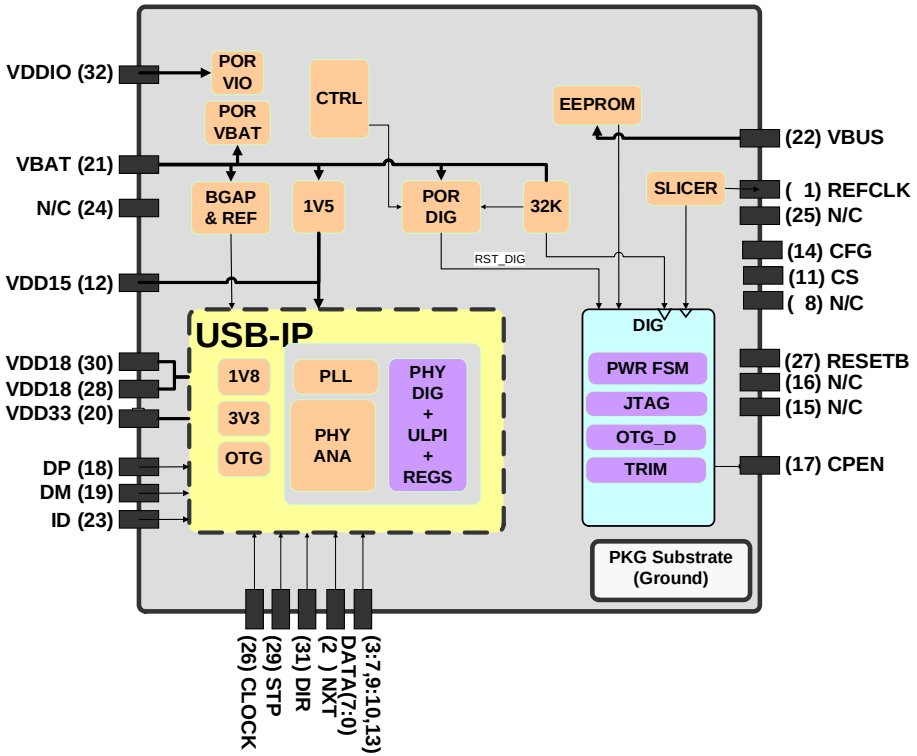
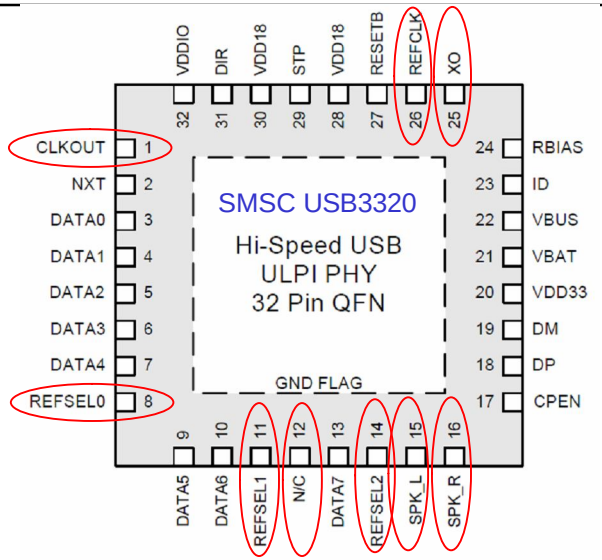
SMSC USB3320

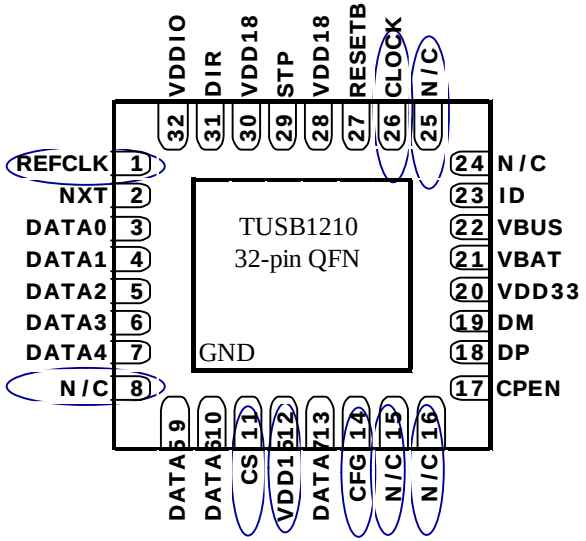


TUSB1210



SMSC3320 vs TUSB1210 : Pinout





PIN #	SMSC USB 3320	TUSB1210	COMMENT
1	CLKOUT	REFCLK	To match SMSC ULPI input mode. Tie to VDDIO in ULPI input clock mode
8	REFSEL0	N/C	Not bonded. Only 19.2M/26M input frequencies supported, via CFG pin #14..
11	REFSEL1	CS	Active-high chip select pin. When low the IC is in power down and ULPI bus is tri-stated. When high normal operation. Tie to VDDIO if unused.
12	N/C	VDD15	Bypass capacitor required on this pin for internal VDD15 LDO stability.
14	REFSEL2	CFG	REFCLK input frequency is 26M when this bit is '1' else 19.2MHz.
15	SPK_L	N/C	High-impedance (test pin). Audio switch feature not supported.
16	SPK_R	N/C	Not bonded. Audio switch feature not supported.
25	XO	N/C	XTAL Oscillator not supported
26	REFCLK	CLOCK	CLOCK pin placed at pin#26 to match SMSC ULPI input mode. Connect to 60MHz clock output pin of Link.

Suggested Application Diagram : TUSB1210

ULPI Input Clock Mode

1A

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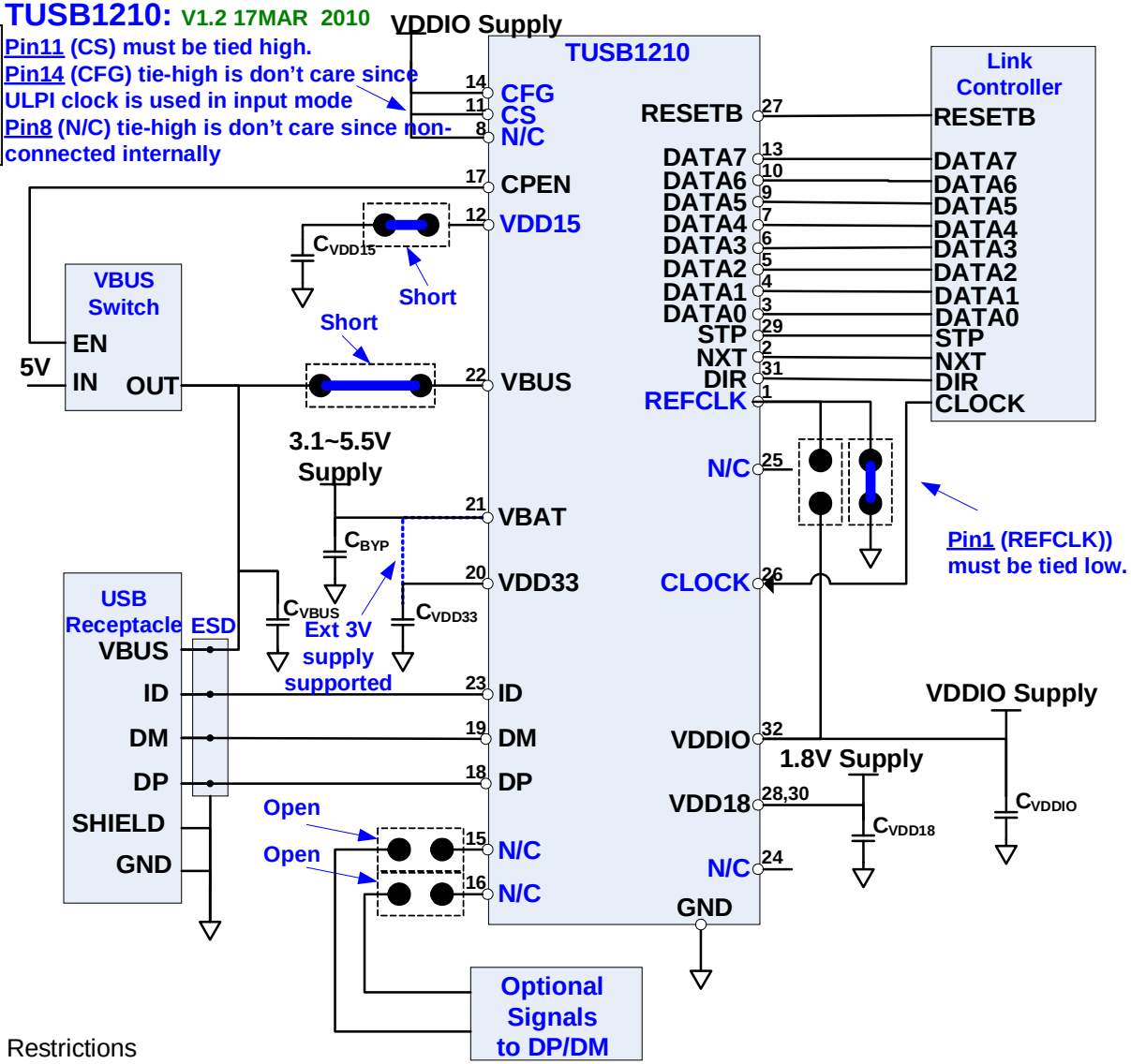
Suggested Application Diagram for compatibility with OMAP3 (Host or OTG, ULPI input-clock mode)

TUSB1210: V1.2 17MAR 2010

Pin11 (CS) must be tied high.

Pin14 (CFG) tie-high is don't care since ULPI clock is used in input mode

Pin8 (N/C) tie-high is don't care since non-connected internally



Suggested Application Diagram : SMSC USB3320

ULPI Input Clock Mode

1B

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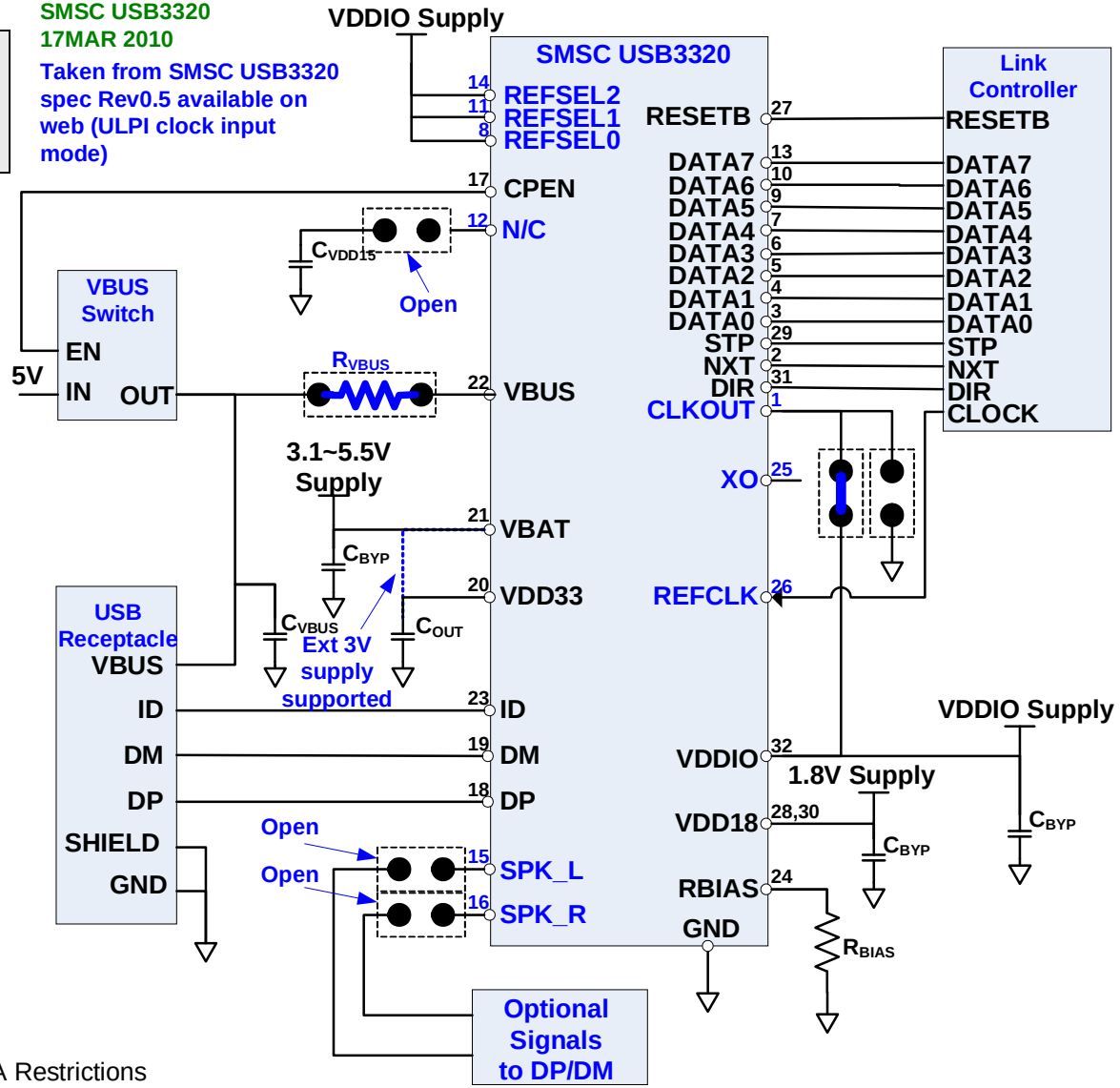
Suggested Application Diagram for compatibility with OMAP3 (Host or OTG, ULPI input-clock mode)

SMSC USB3320
17MAR 2010

Taken from SMSC USB3320 spec Rev0.5 available on web (ULPI clock input mode)



TUSB1210/SMSC USB3320 Connection rules

ULPI Input Clock Mode

1C

- TUSB1210
  - Clock connection:
    - Slave mode clock (ULPI clock input from LINK):
      - Pin1 (REFCLK) 0-ohm to GND
      - Pin26 (CLOCK) <- LINK ULPI CLKOUT
  - Pin12 (VDD15) 0-ohm to CVDD15 (2.2uF)
  - Pin22 (VBUS) 0-ohm series resistor
  - Pin24(NC) open

- SMSC USB3320
  - Note Pin numbers and physical package pin positions are same as TUSB1210 (but pin names differ)
  - Clock Connection:
    - Slave mode clock (ULPI clock output to LINK):
      - Pin1 (CLKOUT) 0-ohm to VDDIO
      - Pin26 (REFCLK) <- LINK ULPI CLKOUT
  - Pin12 (NC) open
  - Pin22 (VBUS) RVBUS 10kohm 5% for HOST device, 1kohm 5% resistor for OTG device
  - Pin24 (RBIAS) RBIAS 8.06kohm +/-1%

Suggested Application Diagram : TUSB1210

ULPI Output Clock Mode (REFCLK 26MHz)

2A

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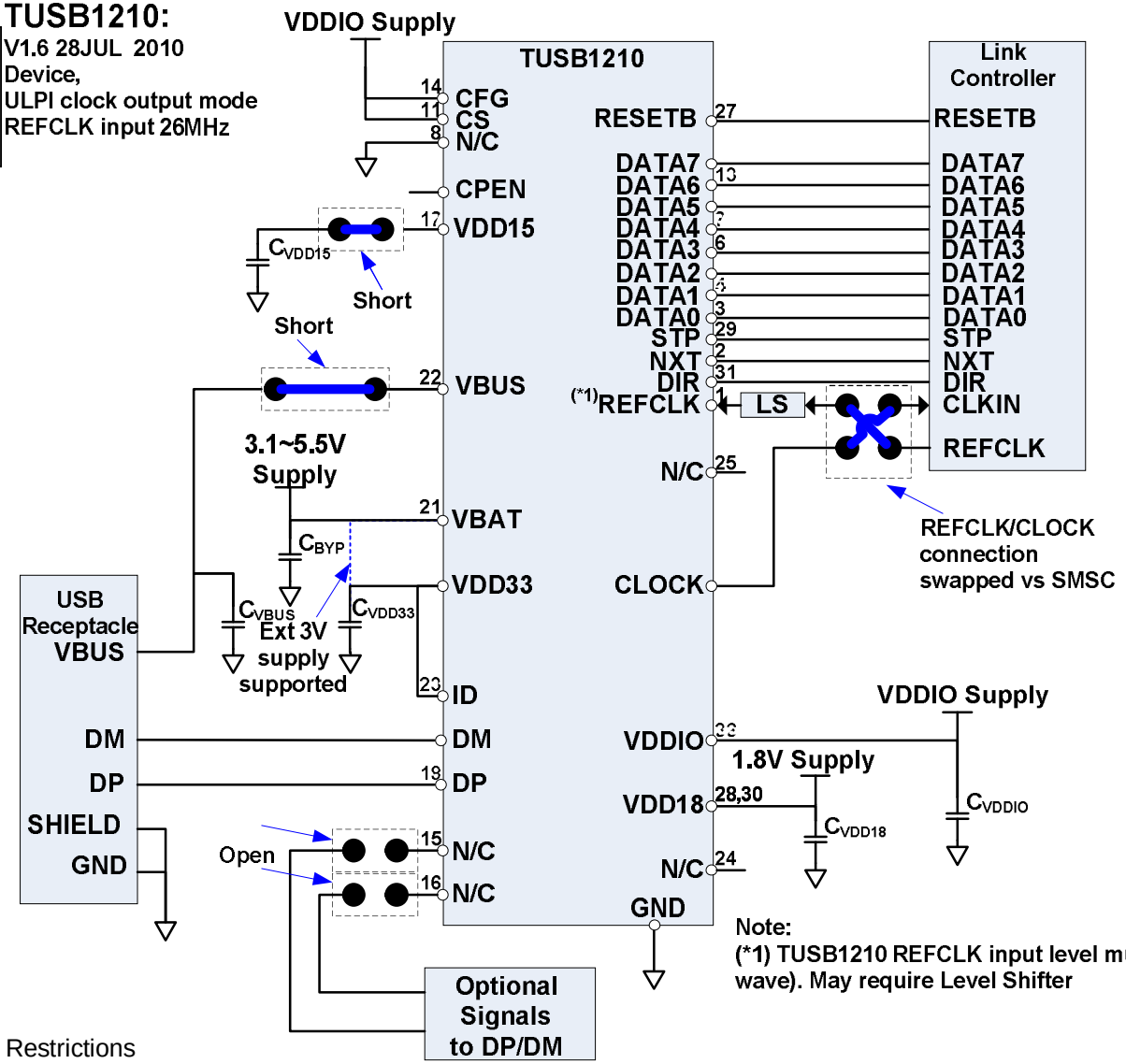
Suggested Application Diagram for compatibility with OMAP3 (Device, ULPI output-clock mode)

TUSB1210:
V1.6 28JUL 2010
Device,
ULPI clock output mode
REFCLK input 26MHz



Note:
(*1) TUSB1210 REFCLK input level must be 3.3V (square-wave). May require Level Shifter

Texas Instruments

Suggested Application Diagram : SMSC USB3320

ULPI Output Clock Mode (REFCLK 26MHz)

2B

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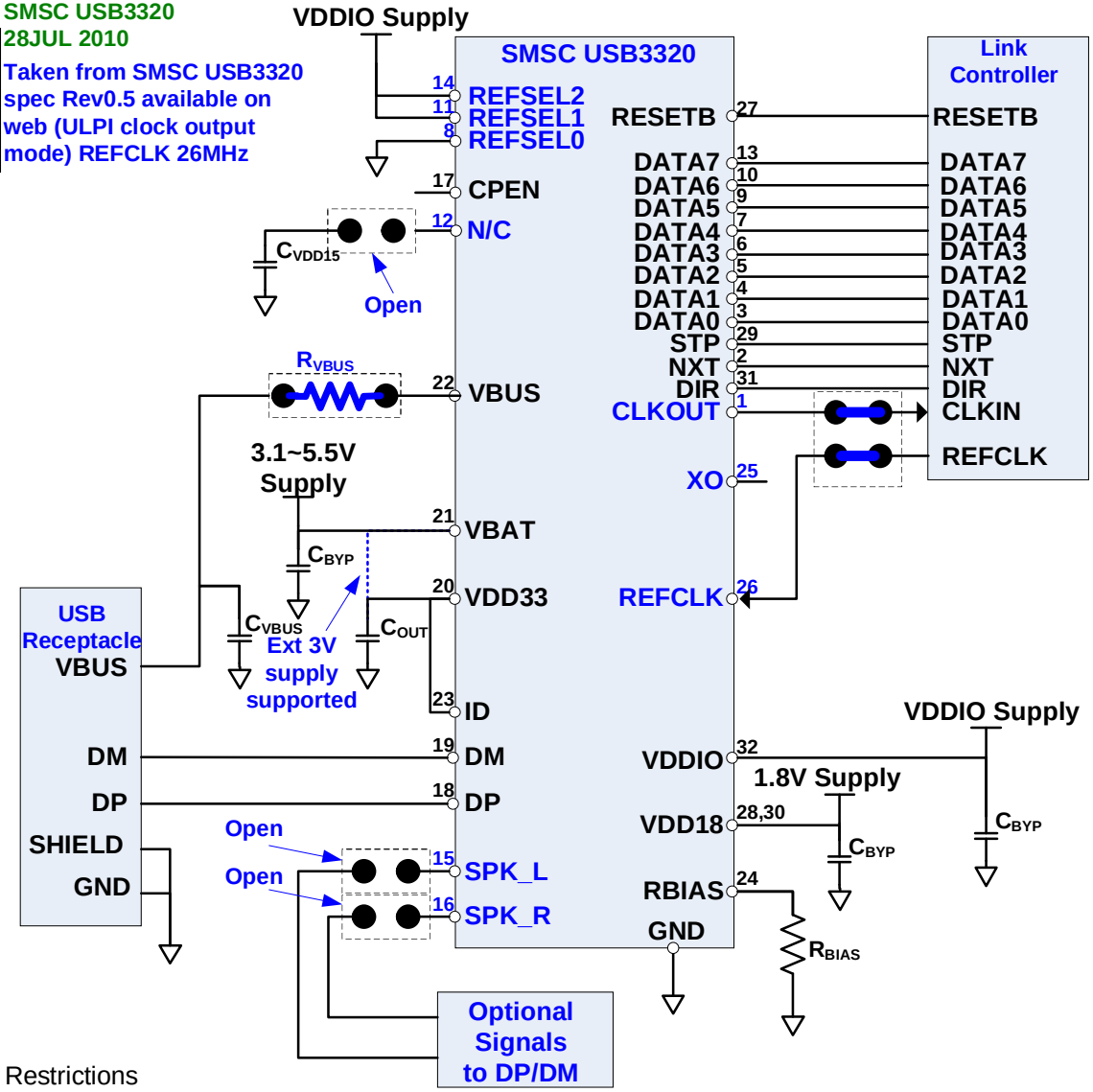
Suggested Application Diagram for compatibility with OMAP3 (Device, ULPI output-clock mode)

SMSC USB3320
28JUL 2010

Taken from SMSC USB3320 spec Rev0.5 available on web (ULPI clock output mode) REFCLK 26MHz



TUSB1210/SMSC USB3320 Connection rules

ULPI Output Clock Mode (REFCLK 26MHz)

2C

- TUSB1210
  - Clock connection:
    - Master mode clock (ULPI clock output to Link):
      - Note: TUSB1210 Pin1 (REFCLK) input level must be 3.3V (square-wave). May require Level Shifter
      - Pin1 (REFCLK) <- LINK REFCLK
      - Pin26 (CLOCK) -> LINK ULPI CLKIN
  - Pin12 (VDD15) 0-ohm to CVDD15 (2.2uF)
  - Pin22 (VBUS) 0-ohm series resistor
  - Pin24(NC) open

- SMSC USB3320
  - Note Pin numbers and physical package pin positions are same as TUSB1210 (but pin names differ)
  - Clock Connection:
    - Master mode clock: (ULPI clock output to LINK):
      - Pin1 (CLKOUT) -> LINK ULPI CLKIN
      - Pin26 (REFCLK) <- LINK REFCLK
  - Pin12 (NC) open
  - Pin22 (VBUS) RVBUS 10kohm 5% for HOST device, 1kohm 5% resistor for OTG device
  - Pin24 (RBIAS) RBIAS 8.06kohm +/-1%

Suggested Application Diagram : TUSB1210

ULPI Output Clock Mode (REFCLK 19.2MHz)

3A

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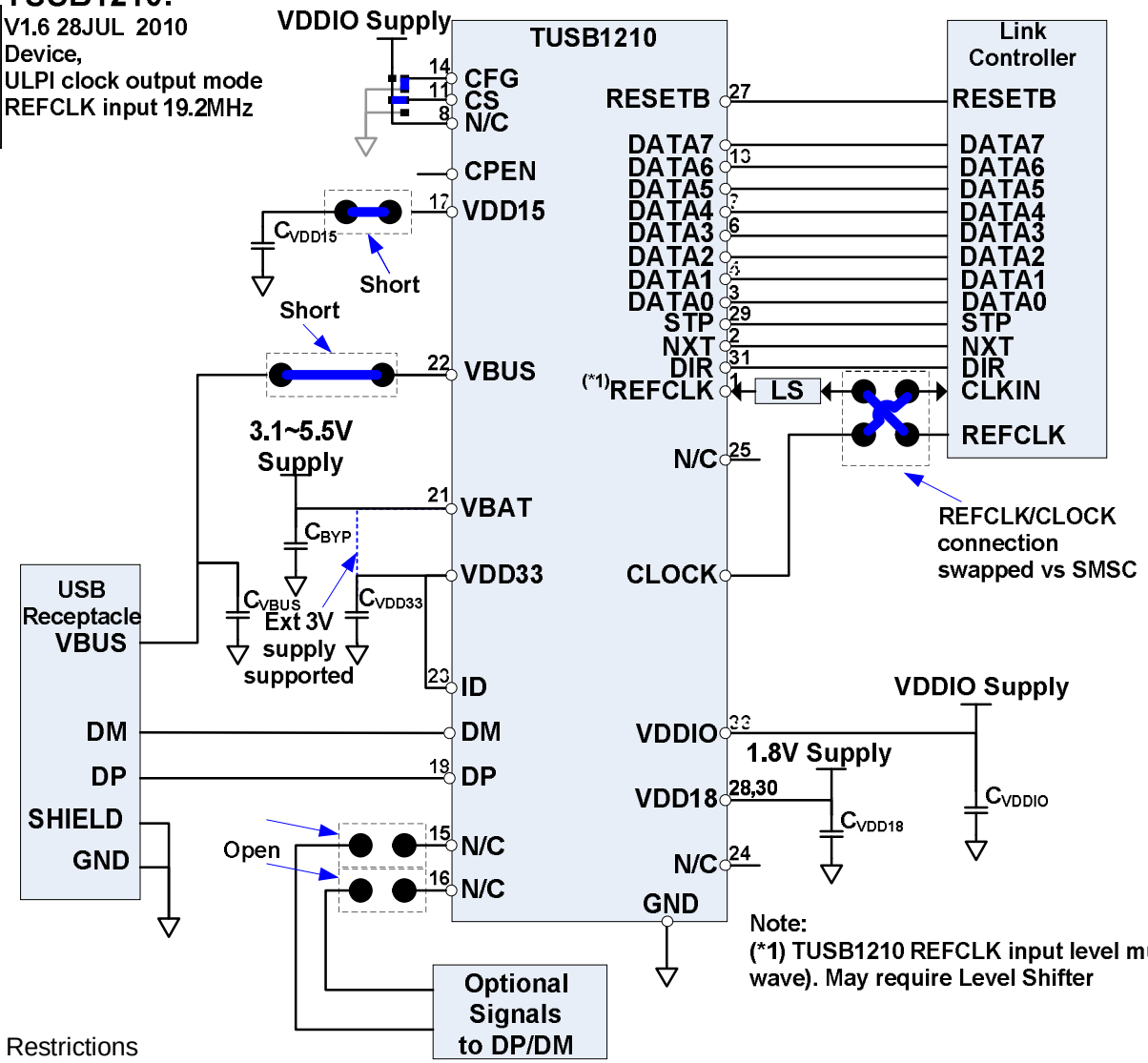
Suggested Application Diagram for compatibility with OMAP3 (Device, ULPI output-clock mode)

TUSB1210:
V1.6 28JUL 2010
Device,
ULPI clock output mode
REFCLK input 19.2MHz



Note:
(*1) TUSB1210 REFCLK input level must be 3.3V (square-wave). May require Level Shifter

Suggested Application Diagram : SMSC USB3320

ULPI Output Clock Mode (REFCLK 19.2MHz)

3B

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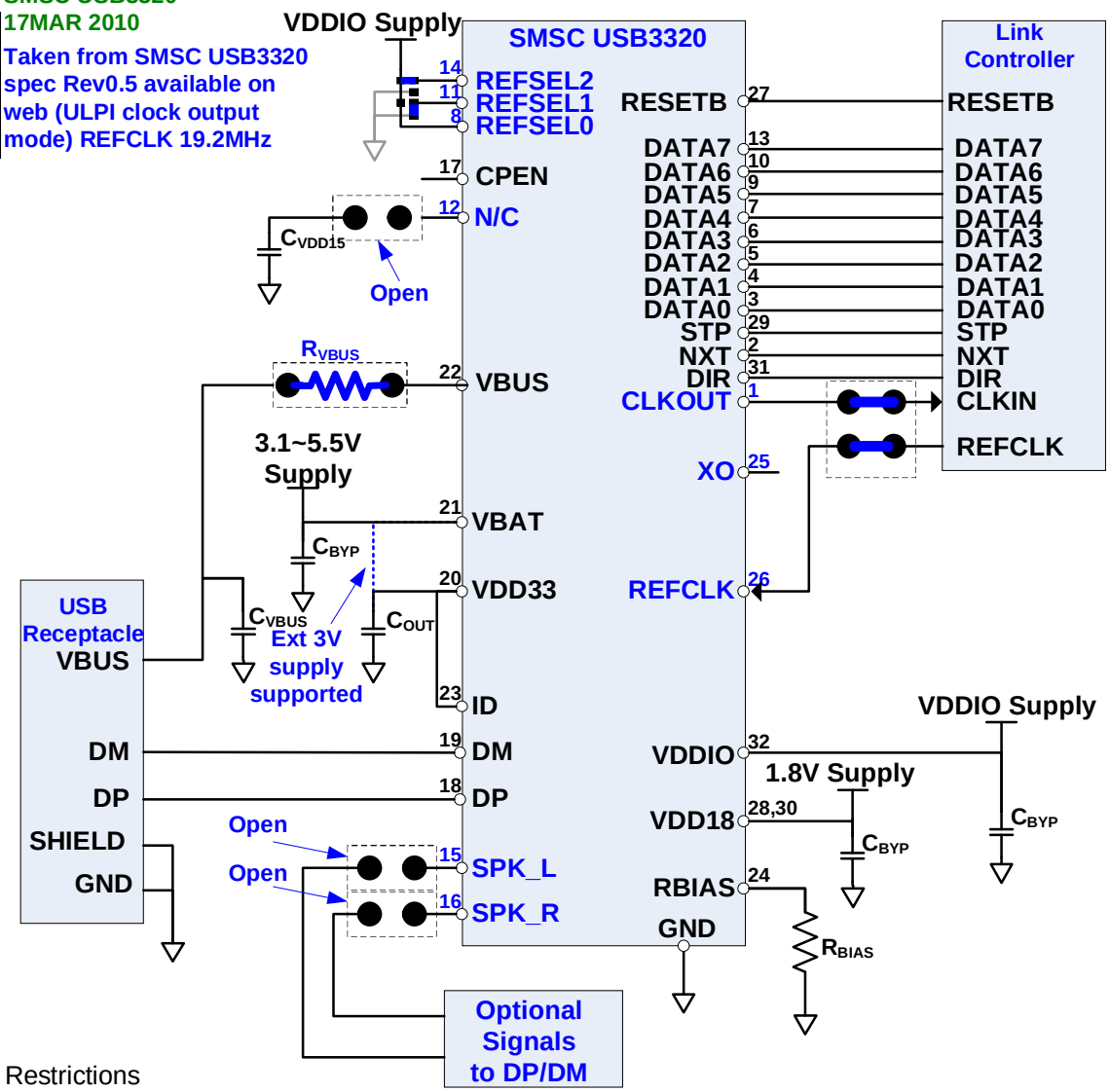
Suggested Application Diagram for compatibility with OMAP3 (Device, ULPI output-clock mode)

SMSC USB3320
17MAR 2010

Taken from SMSC USB3320 spec Rev0.5 available on web (ULPI clock output mode) REFCLK 19.2MHz



TUSB1210/SMSC USB3320 Connection rules

ULPI Output Clock Mode (REFCLK 19.2MHz)

3C

- TUSB1210
  - Clock connection:
    - Master mode clock (ULPI clock output to Link):
      - Note: TUSB1210 Pin1 (REFCLK) input level must be 3.3V (square-wave). May require Level Shifter
      - Pin1 (REFCLK) <- LINK REFCLK
      - Pin26 (CLOCK) -> LINK ULPI CLKIN
  - Pin11(CS) 0-ohm to VDDIO
  - Pin14(CFG) 0-ohm to GND
  - Pin12 (VDD15) 0-ohm to CVDD15 (2.2uF)
  - Pin22 (VBUS) 0-ohm series resistor
  - Pin24(NC) open

- SMSC USB3320
  - Note Pin numbers and physical package pin positions are same as TUSB1210 (but pin names differ)
  - Clock Connection:
    - Master mode clock: (ULPI clock output to LINK):
      - Pin1 (CLKOUT) -> LINK ULPI CLKIN
      - Pin26 (REFCLK) <- LINK REFCLK
  - Pin11(REFSEL1) 0-ohm to GND
  - Pin14(REFSEL2) 0-ohm to VDDIO
  - Pin12 (NC) open
  - Pin22 (VBUS) RVBUS 10kohm 5% for HOST device, 1kohm 5% resistor for OTG device
  - Pin24 (RBIAS) RBIAS 8.06kohm +/-1%

TUSB1210 External Components Summary

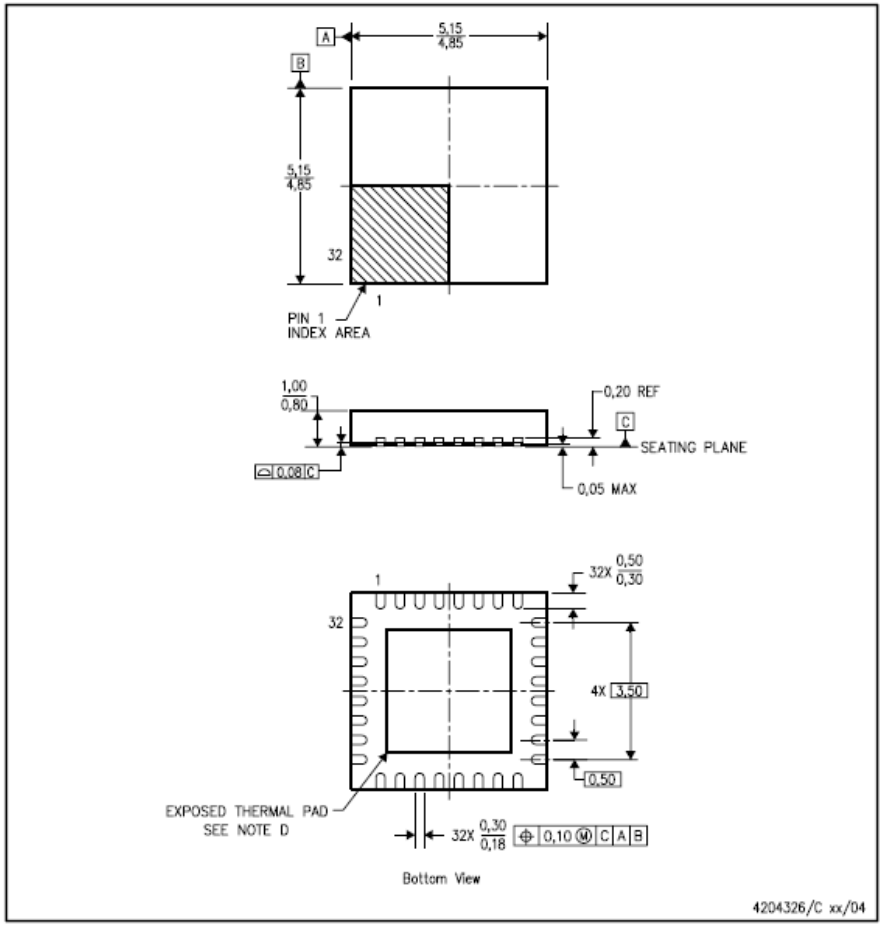
- Excerpt from TUSB1210 Datasheet (*)

  (*) This is intended for reference only, the TUSB1210 datasheet is the official information source

Table 7-1. TUSB1210 External Components

FUNCTION	COMPONENT	REFERENCE	VALUE	NOTE	LINK
V_{DDIO}	Capacitor	CVDDIO	100 nF	Suggested value, application dependent	Figure 9-1
V_{DD33}	Capacitor	CVDD33	2.2 µF	Range: [0.45 µF : 6.5 µF] , ESR = [0 : 600 mΩ] for f> 10 kHz	Figure 9-1
V_{DD15}	Capacitor	CVDD15	2.2 µF	Range: [0.45 µF : 6.5 µF] , ESR = [0 : 600 mΩ] for f> 10 kHz	Figure 9-1
V_{DD18}	Capacitor	Int 1.8V LDO CVDD18	2.2 µF	Range: [0.45 µF : 6.5 µF] , ESR = [0 : 600 mΩ] for f> 10 kHz	Figure 9-1
	Capacitor	Ext 1.8V supply CVDD18	100 nF	Suggested value, application dependent	Figure 9-1
V_{BAT}	Capacitor	CBYP	2.2 µF	Range: [0.45 µF : 6.5 µF] , ESR = [0 : 600 mΩ] for f> 10 kHz	Figure 9-1
V_{BUS}	Capacitor	CVBUS	See table 1.2	Place close to USB connector	Figure 9-1

Package : TUSB1210



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) Package configuration.
D The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO-220.

- Package:
  - QFN 32-pin
  - 5 x 5
  - 0.5mm pitch

Package : SMSC USB3320

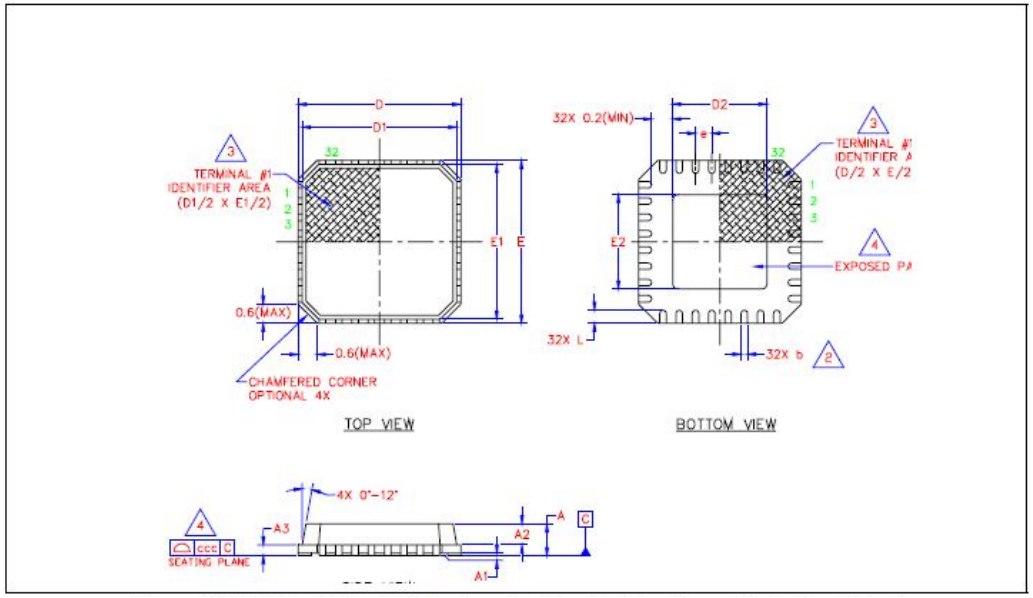


Figure 6 USB3320 32 Pin QFN Package Outline, 5 x 5 x 0.9 mm Body (Lead-Free)

Table 2 32 Terminal QFN Package Parameters

	MIN	NOMINAL	MAX	REMARKS
A	0.70	~	1.00	Overall Package Height
A1	0	0.02	0.05	Standoff
A2	~	~	0.90	Mold Thickness
A3		0.20 REF		Copper Lead-frame Substrate
D	4.85	5.0	5.15	X Overall Size
D1	4.55	~	4.95	X Mold Cap Size
D2	3.15	3.3	3.45	X exposed Pad Size
E	4.85	5.0	5.15	Y Overall Size
E1	4.55	~	4.95	Y Mold Cap Size
E2	3.15	3.3	3.45	Y exposed Pad Size
L	0.30	~	0.50	Terminal Length
e		0.50 BSC		Terminal Pitch
b	0.18	0.25	0.30	Terminal Width
ccc	~	~	0.08	Coplanarity

Notes:

1. Controlling Unit: millimeter.
2. Dimension b applies to plated terminals and is measured between 0.15mm and 0.30mm from the terminal tip. Tolerance on the true position of the leads is ± 0.05 mm at maximum material conditions (MMC).
3. Details of terminal #1 identifier are optional but must be located within the zone indicated.
4. Coplanarity zone applies to exposed pad and terminals.