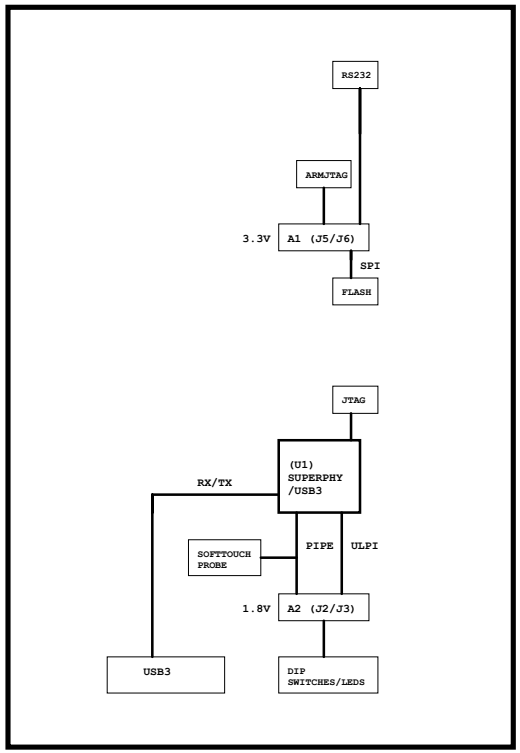
DESIGN NOTES:
- ESTIMATE THE NUMBER OF LAYERS TO BE 6 OR 8 LAYERS.
- ALL SINGLE-ENDED NETS ARE 50-OHMS IMPEDANCE UNLESS OTHERWISE SPECIFICED.
- ALL DIFFERENTIAL NETS ARE 100-OHMS DIFFERENTIAL IMPEDANCE UNLESS OTHERWISE SPECIFIED.



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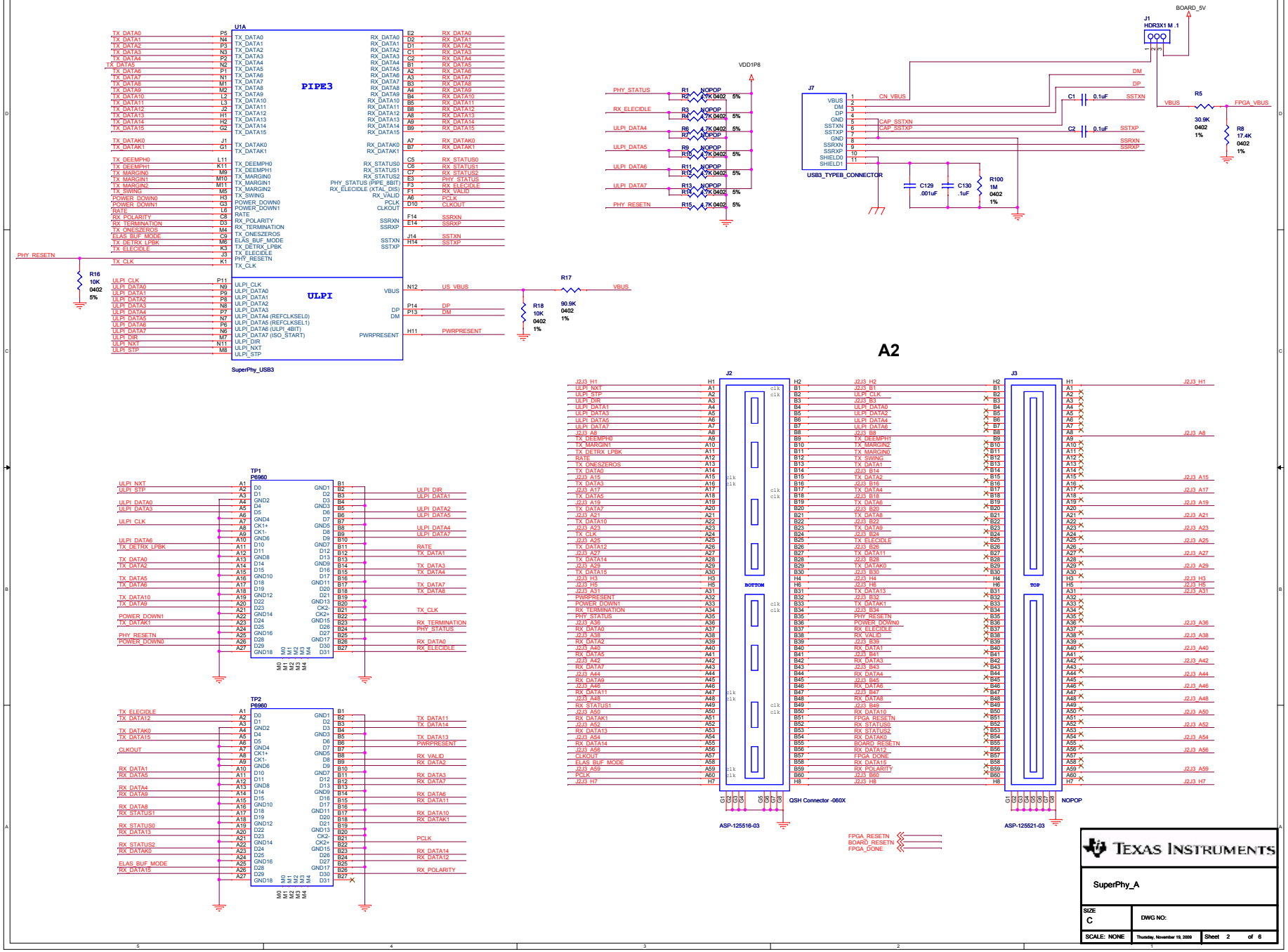
U1A
PIPE3
ULPI
SuperPhy_USB3
VDD1P8
R1 NOPOP
R2 47K 0402 5%
R3 NOPOP
R4 47K 0402 5%
R6 47K 0402 5%
R7 NOPOP
R9 NOPOP
R10 47K 0402 5%
R11 NOPOP
R12 47K 0402 5%
R13 NOPOP
R14 47K 0402 5%
R15 47K 0402 5%
R16 10K 0402 5%
R17 90.9K 0402 1%
R18 10K 0402 1%
J7
USB3_TYPEB_CONNECTOR
C1 0.1uF
C2 0.1uF
C129 .001uF
C130 .1uF
R100 1M 0402 1%
R5 30.9K 0402 1%
R8 17.4K 0402 1%
J1 HDR3X1 M_1
BOARD_5V
A2
J2
J3
TP1
P6960
TP2
P6960
QSH Connector -060X
ASP-125516-03
ASP-125521-03
NOPOP
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SuperPhy_A
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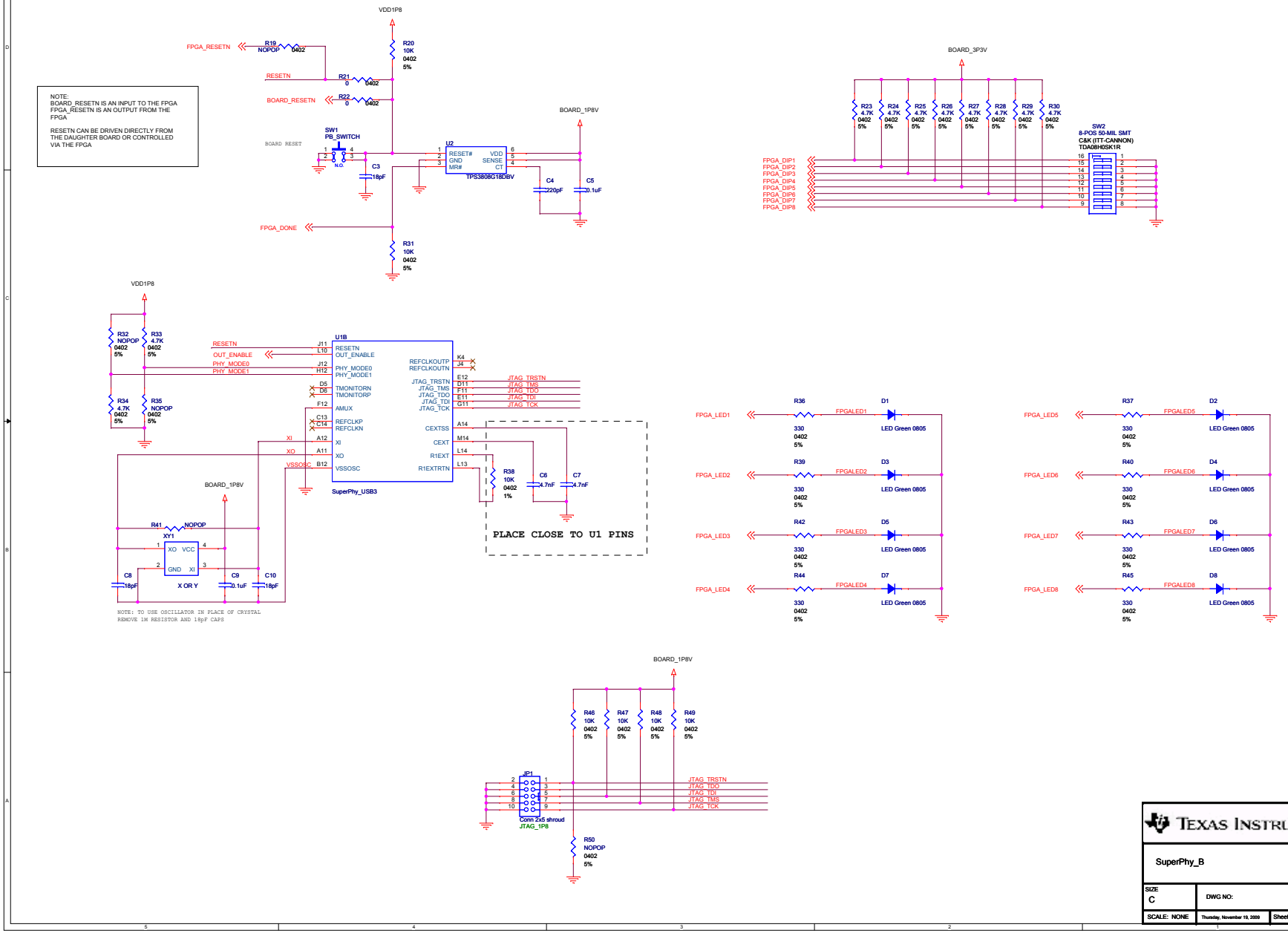
NOTE:
BOARD_RESETN IS AN INPUT TO THE FPGA
FPGA_RESETN IS AN OUTPUT FROM THE FPGA.
RESETN CAN BE DRIVEN DIRECTLY FROM THE DAUGHTER BOARD OR CONTROLLED VIA THE FPGA
VDD1P8
FPGA_RESETN
R19 NOPOP 0402
R20 10K 0402 5%
RESETN
R21 0 0402
BOARD_RESETN
R22 0 0402
BOARD_1P8V
SW1 PB_SWITCH
BOARD RESET
N.O.
C3 18pF
U2
RESET# VDD
GND SENSE
MR# CT
TPS3808G18DBV
C4 220pF
C5 0.1uF
FPGA_DONE
R31 10K 0402 5%
BOARD_3P3V
R23 4.7K 0402 5%
R24 4.7K 0402 5%
R25 4.7K 0402 5%
R26 4.7K 0402 5%
R27 4.7K 0402 5%
R28 4.7K 0402 5%
R29 4.7K 0402 5%
R30 4.7K 0402 5%
SW2
8-POS 50-MIL SMT
C&K (ITT-CANNON)
TDA08H0SK1R
FPGA_DIP1
FPGA_DIP2
FPGA_DIP3
FPGA_DIP4
FPGA_DIP5
FPGA_DIP6
FPGA_DIP7
FPGA_DIP8
VDD1P8
R32 NOPOP 0402 5%
R33 4.7K 0402 5%
R34 4.7K 0402 5%
R35 NOPOP 0402 5%
U1B
RESETN
OUT_ENABLE
PHY_MODE0
PHY_MODE1
TMONITORN
TMONITORP
AMUX
REFCLKP
REFCLKN
XI
XO
VSSOSC
REFCLKOUTP
REFCLKOUTN
JTAG_TRSTN
JTAG_TMS
JTAG_TDO
JTAG_TDI
JTAG_TCK
CEXTSS
CEXT
R1EXT
R1EXTRTN
SuperPhy_USB3
R38 10K 0402 1%
C8 4.7nF
C7 4.7nF
PLACE CLOSE TO U1 PINS
BOARD_1P8V
R41 NOPOP
XY1
XO VCC
GND XI
X OR Y
C8 18pF
C9 0.1uF
C10 18pF
NOTE: TO USE OSCILLATOR IN PLACE OF CRYSTAL
REMOVE 1M RESISTOR AND 18pF CAPS
FPGA_LED1
FPGA_LED2
FPGA_LED3
FPGA_LED4
R36 330 0402 5%
R39 330 0402 5%
R42 330 0402 5%
R44 330 0402 5%
D1 LED Green 0805
D3 LED Green 0805
D5 LED Green 0805
D7 LED Green 0805
FPGALED1
FPGALED2
FPGALED3
FPGALED4
FPGA_LED5
FPGA_LED6
FPGA_LED7
FPGA_LED8
R37 330 0402 5%
R40 330 0402 5%
R43 330 0402 5%
R45 330 0402 5%
D2 LED Green 0805
D4 LED Green 0805
D6 LED Green 0805
D8 LED Green 0805
FPGALED5
FPGALED6
FPGALED7
FPGALED8
BOARD_1P8V
R46 10K 0402 5%
R47 10K 0402 5%
R48 10K 0402 5%
R49 10K 0402 5%
JP1
Conn 2x5 shroud
JTAG_1P8
JTAG_TRSTN
JTAG_TDO
JTAG_TDI
JTAG_TMS
JTAG_TCK
R50 NOPOP 0402 5%
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SuperPhy_B
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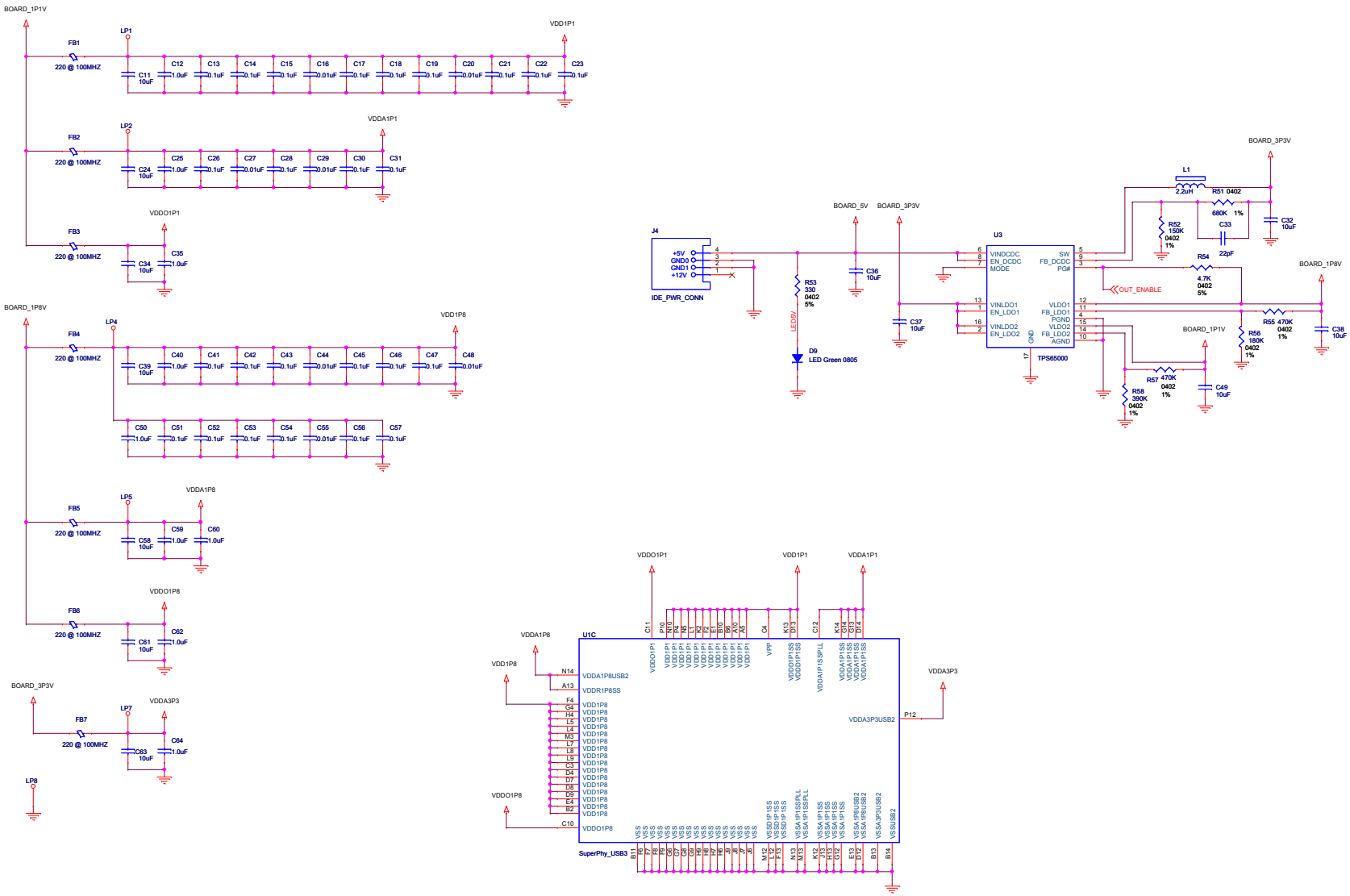

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SuperPhy_C

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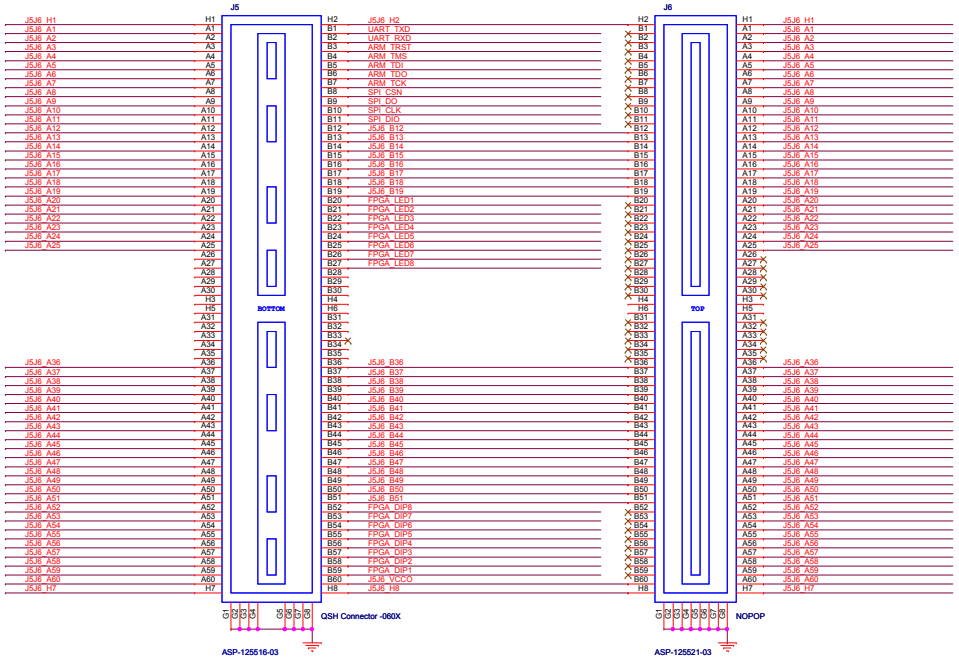
ALL 3.3V SIGNALS. MAKE SURE
BANK ON FPGA IS SET TO 3.3V

A1



UART_TXD
UART_RXD
ARM_TRST
ARM_TMS
ARM_TDI
ARM_TDO
ARM_TCK
SPI_CSN
SPI_DO
SPI_CLK
SPI_DIO

FPGA_DIP1
FPGA_DIP2
FPGA_DIP3
FPGA_DIP4
FPGA_DIP5
FPGA_DIP6
FPGA_DIP7
FPGA_DIP8
FPGA_LED1
FPGA_LED2
FPGA_LED3
FPGA_LED4
FPGA_LED5
FPGA_LED6
FPGA_LED7
FPGA_LED8

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HAPS_A1

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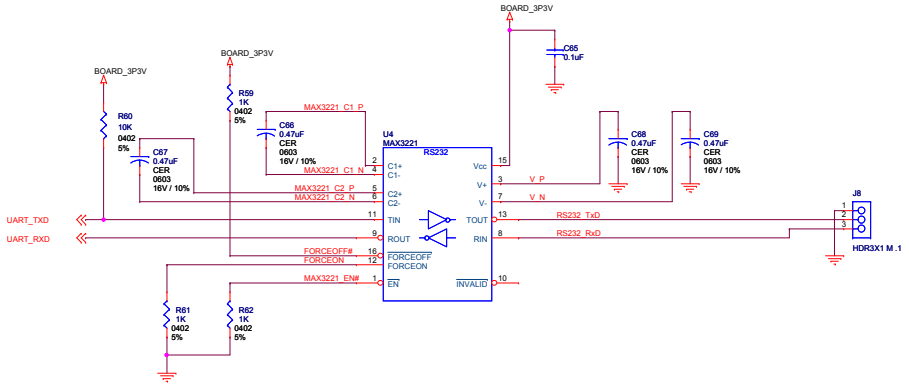
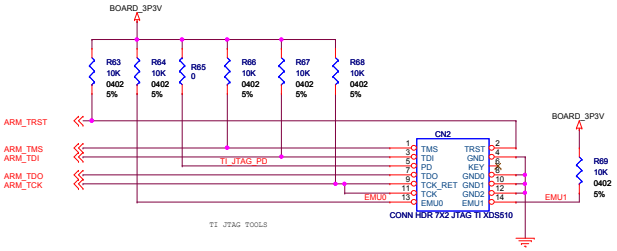
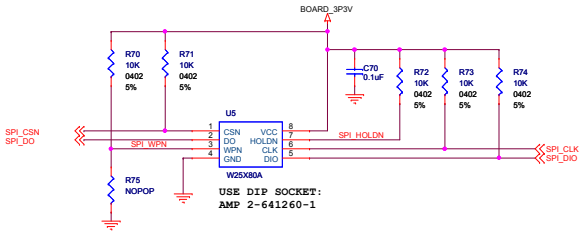
RS232 PORT



ARM JTAG XDS510 CONNECTOR



SPI EEPROM



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JTAG/SPI/TERM

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