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TI Designs
ONET SFP+ 10G LR Reference Design With ONET8551T, ONET1151P, and ONET1151L

TEXAS INSTRUMENTS

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Design Resources

MSP430FR5728	Product Folder
ONET8551T	Product Folder
ONET1151P	Product Folder
ONET1151L	Product Folder
TPS82693	Product Folder

Design Overview

The Texas Instruments 10.3125-Gbps SFP+ LR Reference Design evaluation board (EVM) was designed to demonstrate the optical performance of the ONET1151L laser driver, the ONET8551T high-gain transimpedance amplifier (TIA), and the ONET1151P limiting Amplifier. An MSP430™ microcontroller (MCU), the MSP430FR5728, is used to control the setup of the ONET1151L and ONET1151P in conjunction with a graphical user interface (GUI). The MSP430FR5728 device also stores the register settings in FRAM. The TPS82693 high-efficiency MicroSiP step-down converter is used to supply 2.85 V to the ICs to reduce the module power dissipation. This design is a functional SFP+ module used to demonstrate the performance of the transmitter and receiver. Digital diagnostics and temperature compensation of the laser-driver modulation current are not included.

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WebBench Calculator Tools
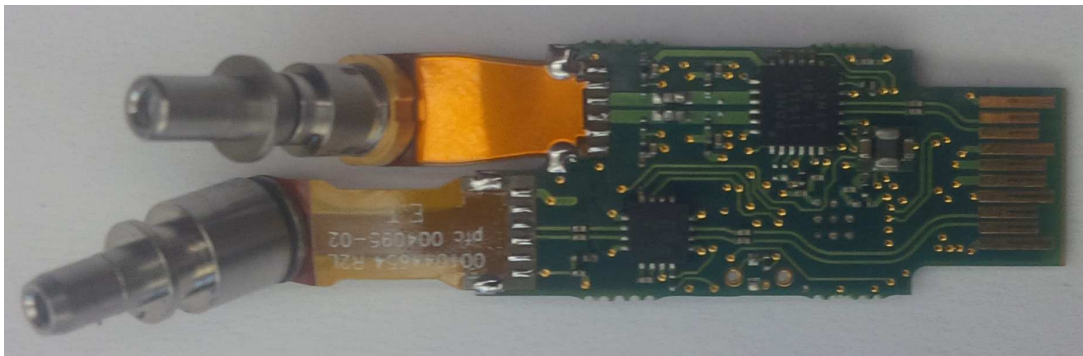
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1 Introduction

The 10.3125-Gbps SFP+ LR Reference Design evaluation board evaluates the optical performance of the ONET1151L device, the ONET8551T device and the ONET1151P device. The ONET1151L is used to drive a 1310-nm DFB laser in an LC transmit-optical sub-assembly (TOSA). The ONET1151P is used to amplify the signal from the PIN-TIA LC receive-optical sub-assembly (ROSA) which contains the ONET8551T TIA.
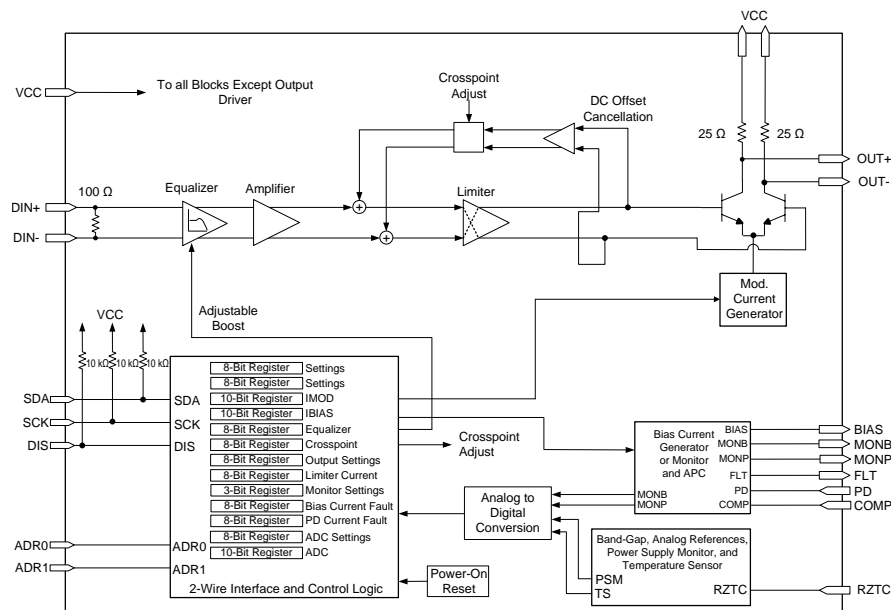
1.1 ONET1151L

Figure 1. ONET1151L — 11.3-Gbps Low-Power Laser-Diode Driver

1.1.1 Features

- Two-wire digital interface with integrated DACs and ADC for control and diagnostic management
- 150 to 1200-mVp-p input voltage
- Digitally programmable:
    - Input equalizer
    - Modulation current up to 85 mA
    - Bias current up to 100 mA
    - Cross point control
    - Rise and fall times
    - Output de-emphasis
    - Output termination resistance
- Output polarity select
- Photodiode current range
- Automatic power control (APC)
- Power-supply monitor and temperature sensor
- Fault detection

1.1.2 Applications

- 10-Gb ethernet optical transmitters
- SONET OC-192 optical transmitters

- XFP and SFP+ transceiver modules
- XENPAK, XPAK, X2, and 300-pin MSA transponder modules

1.1.3 Benefits

- 25-Ω passive back termination reduces sensitivity to laser mismatch
- Low power: 400 mW with IMOD = 30 mA and IBIAS = 30 mA
- Pin compatible to the ONET1101L
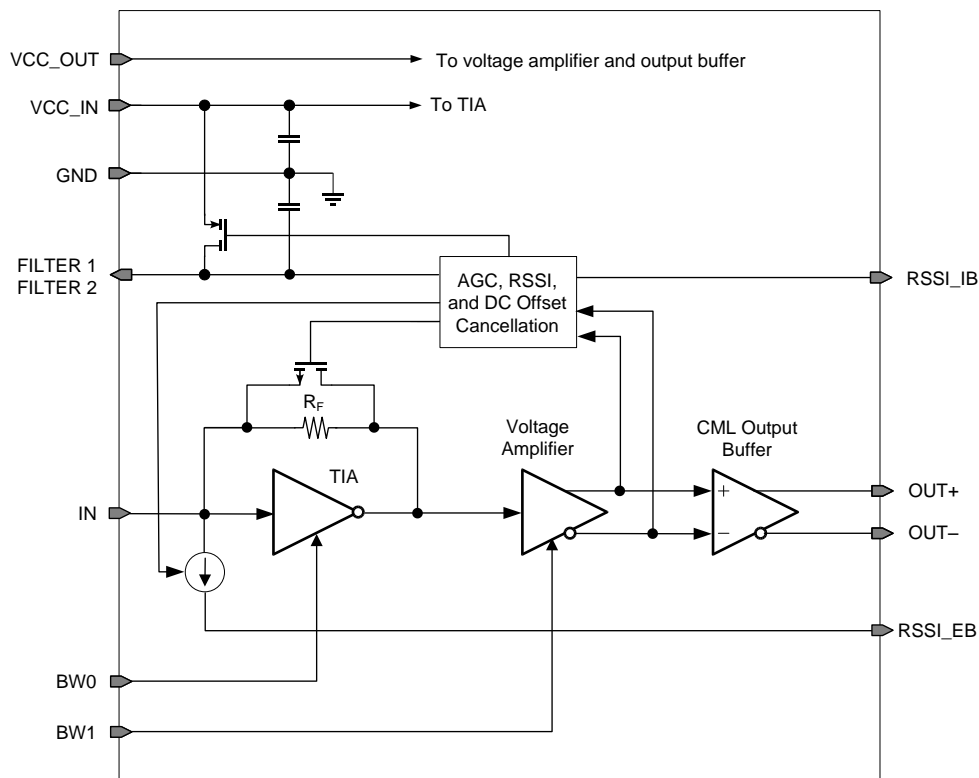- –40°C to 100°C ambient operation

1.2 ONET8551T

Figure 2. ONET8551T — 11.3-Gbps High-Gain Limiting-TIA With RSSI

1.2.1 Features

- 9-GHz bandwidth
- 10-kΩ differential transimpedance
- 0.9-μA_{RMS} input referred noise
- –20-dBm sensitivity
- 2.5-mApp input overload current
- Received signal-strength indicator
- 92-mW typical power dissipation
- Single 3.3-V supply
- –40°C to 100°C ambient operation
- On-chip supply filter capacitor
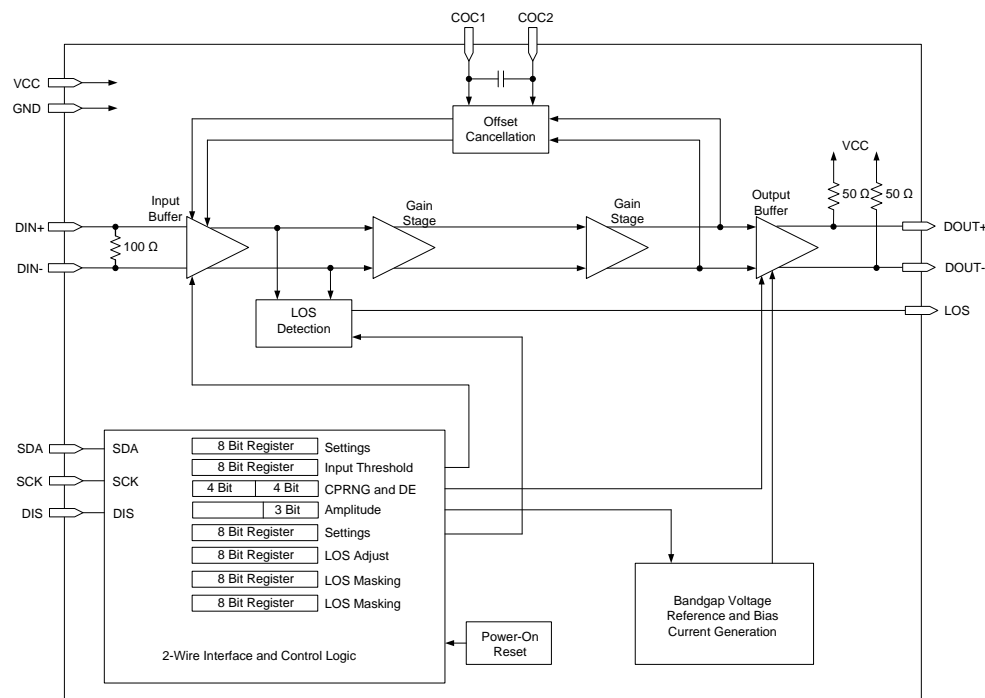- Die size less than 1000 μm × 900 μm

1.2.2 Applications

- 10-Gb ethernet optical receivers
- 8x and 10x fibre-channel optical receivers
- SONET OC-192 optical receivers
- 10G-PON
- 6G and 10G CPRI and OBSAI
- PIN and APD preamplifiers

1.2.3 Benefits

- One TIA for PIN and APD applications
- High gain for reduced crosstalk
- Low bandwidth and transimpedance variation over temperature
- Low power

1.3 ONET1151P

Figure 3. ONET1151P — 11.3-Gbps Limiting Amplifier

1.3.1 Features

- Digitally programmable:
  - LOS
  - Amplitude
  - Input threshold
  - De-emphasis
  - LOS masking time
- 6-mVpp input sensitivity
- Single 3.3-V supply
- –40°C to 100°C ambient operation

1.3.2 Applications

- 10-Gb ethernet optical receivers
- 8x and 10x fibre-channel optical receivers
- 6G and 10G CPRI and OBSAI
- 10G-PON
- SONET OC-192 optical receivers

1.3.3 Benefits

- Few external components
- Programmable masking time for LOS bounce
- Low power: 132 mW with 600-mVpp output
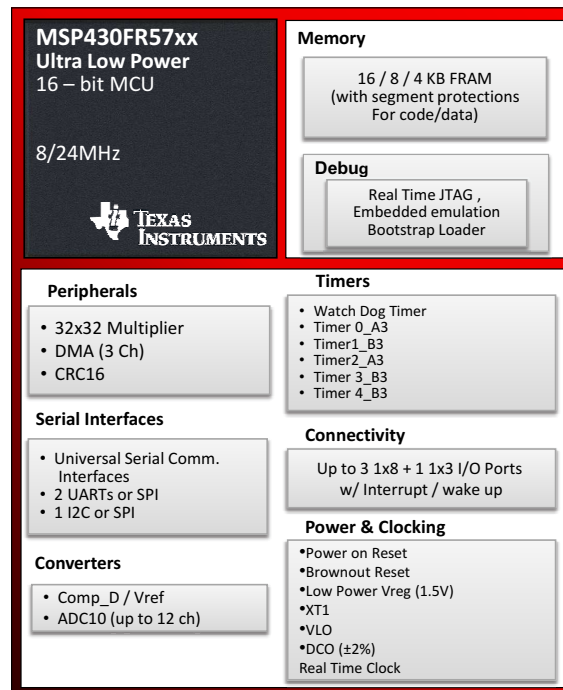- Pin compatible to the ONET8501PB

1.4 MSP430FR57xx

Figure 4. MSP430FR57xx — Ultra-Low Power 16-bit MCU

1.4.1 Performance

- 8-MHz and 24-MHz, 16-bit RISC CPU
  Power
  - Supply voltage range 2 V to 3.6 V
  - Power consumption (typical values at 25ºC)
  - Active mode: 100 µA/MHz
  - Standby mode (LPM3): 6.3 µA
  - RTC mode (LPM3.5): 1.5 µA
  - Shutdown mode (LPM4.5): 0.32 µA
  - Wake up from Standby Mode in 100µs
  - 16-KB, 8-KB, and 4-KB FRAM version with free program code and data-memory partitioning

– 1-KB static random-access memory (SRAM)

Package

– 24-pin and 40-pin QFN

– 38-Pin TSSOP

– Temp Range –40ºC to 85ºC

1.4.2   Benefits

• FRAM: Ultra-low power, universal memory
  – Nearly infinite (1015) write cycles
  – 160-times faster than Flash (greater than 2 MB/s)
  – 250-times less power in writes
  – Flexible as data or program memory
• High performance analog
  – ADC10: 200 ksps and 150-µA consumption
  – Versatile analog comparator with 15 external channels, voltage hysteresis, and reference generator
• Cost-efficient system implementation
  – Fast to program
  – Less inventory management
  – Flexible and secure memory partitioning

  For more information about the FRAM Series, go to www.ti.com/fram.

1.5   *TPS82690, TPS82695, TPS82693, and TPS82698*

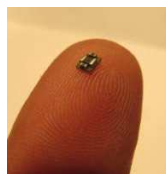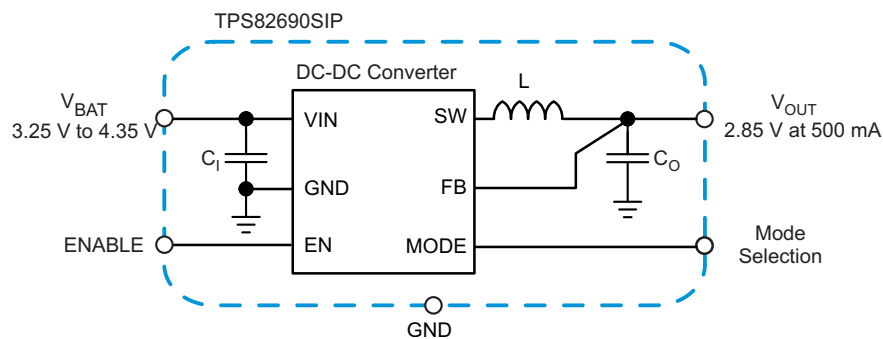**Figure 5. MSP430FR57xx — Ultra-Low Power 16-bit MCU**

Table 1. V_{OUT} and I_{OUT} Options

Device	V_{OUT}	I_{OUT}
TPS82695	2.5 V	500 mA
TPS82690[1]	2.85 V	500 mA
TPS82693	2.85 V	800 mA
TPS82697	2.8 V	800 mA
TPS82698	3 V	800 mA

[1]   Device is in preview.

1.5.1 Features

- Regulated switching frequency: 3 4MHz
- All required external components are integrated
- High PSRR and fast AC load regulation combined with low-ripple Power Save Mode
- Automatic Power Safe Mode transition or forced PWM Mode operation
- Input voltage: 2.3 V to 4.35 V
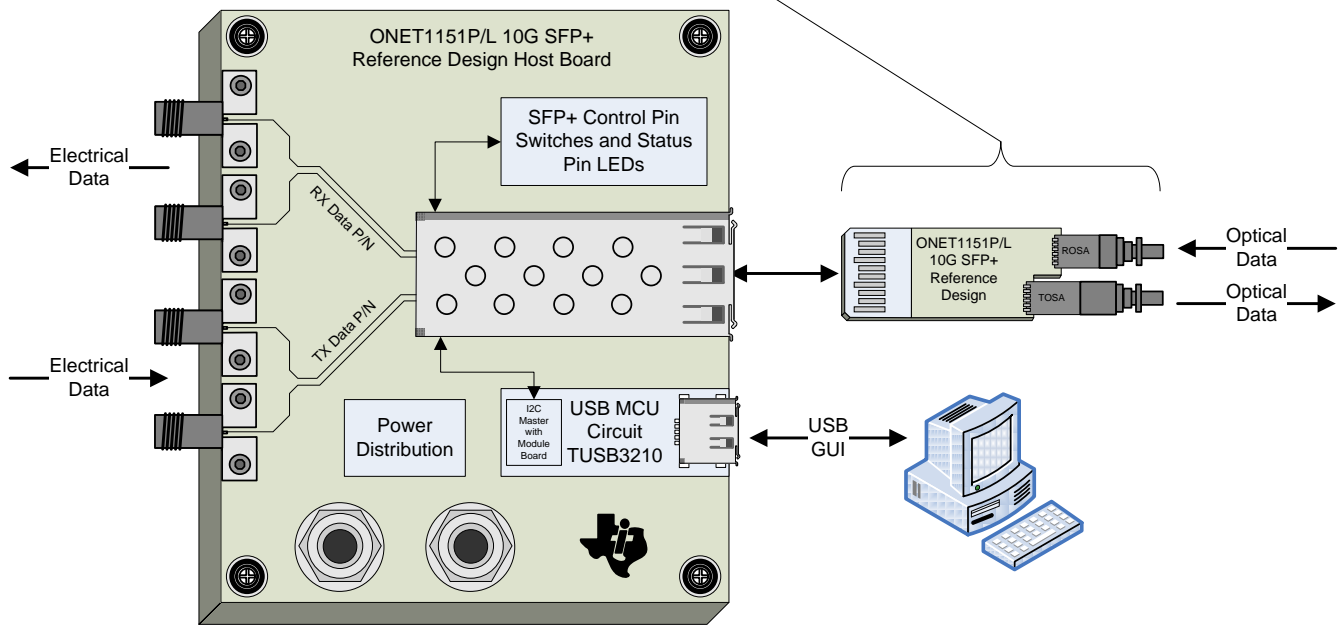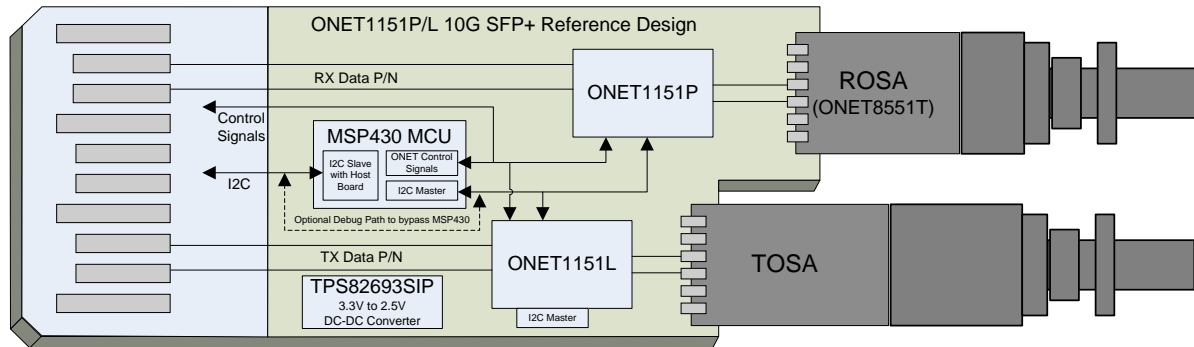- Active power-down sequencing (optional)

1.5.2 Applications

- Mid-end to high-end cell phones and smart phones
- Digital TV, WLAN, GPS, and *Bluetooth*®
- Flash memory
- Portable audio and video

1.5.3 Benefits

- Allows less than 7 mm^2 total solution size and therefore provides 75 mA/mm
- Reduces hardware-design workload with no more questionable designs
- Makes the device an alternative high efficient solution over linear regulators
- Allows to choose between high efficiency over entire load range (PSM) or regulated fixed frequency (PWM)
- Supports Li-Ion batteries with extended voltage range
- Allows time control for power sequencing and a clear and sharp start-up voltage

2   Modules and Schematics

SFP+ Module

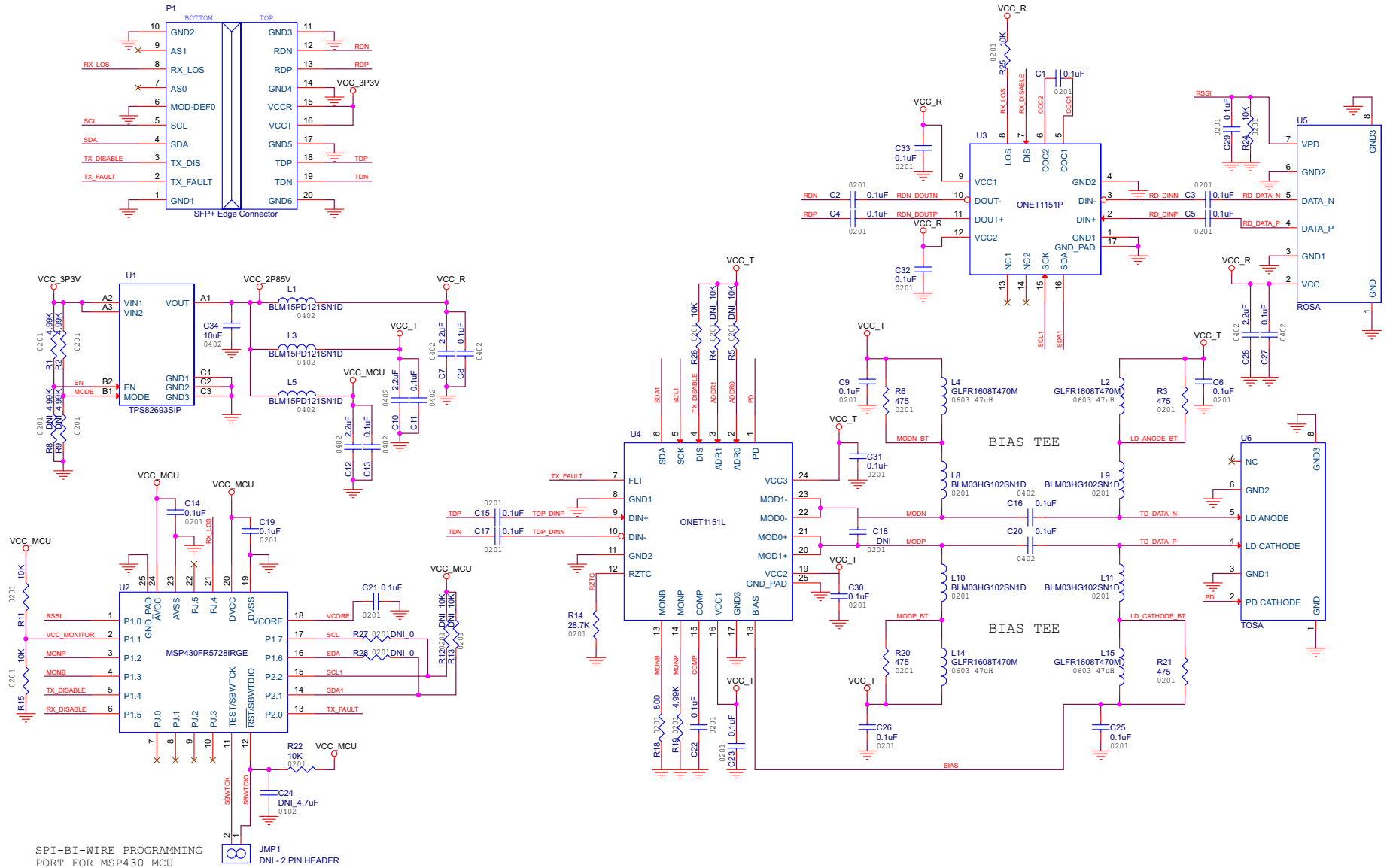
SFP+ Host Board

Figure 6. Module and Host Board

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Figure 7. SFP+ Module Schematic

ONET1151P   **ROSA with ONET8551T**

TPS82693   **ONET1151L**   **TOSA**
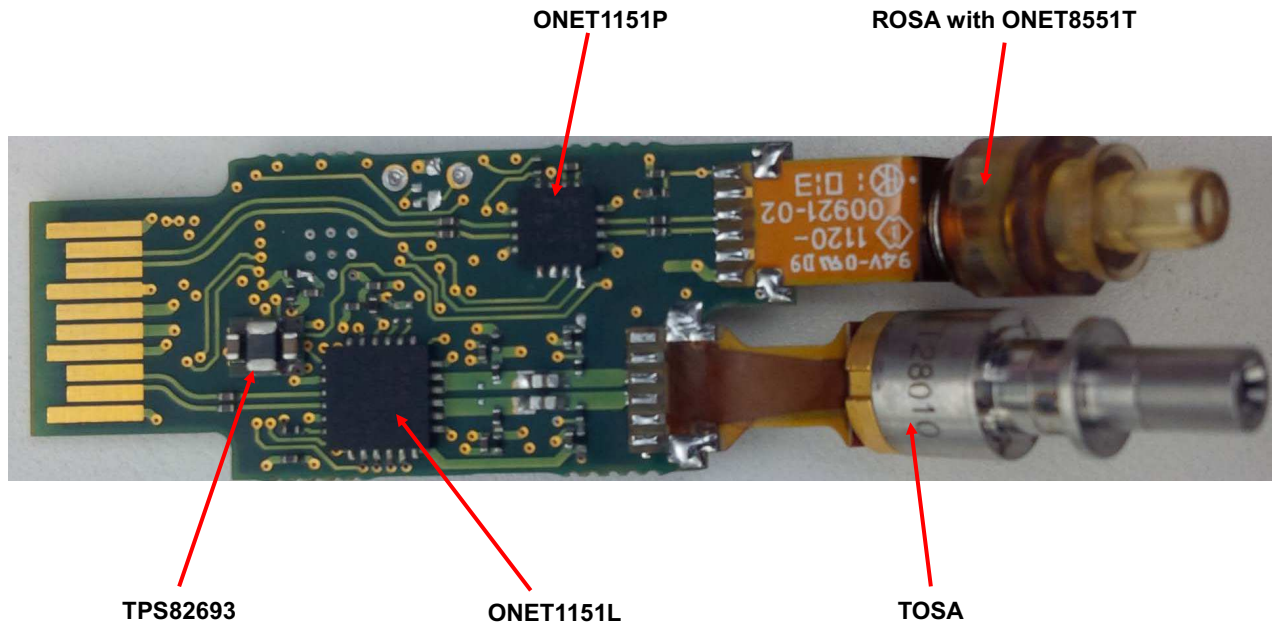
Figure 8. Module Top Side

MSP430FR5728
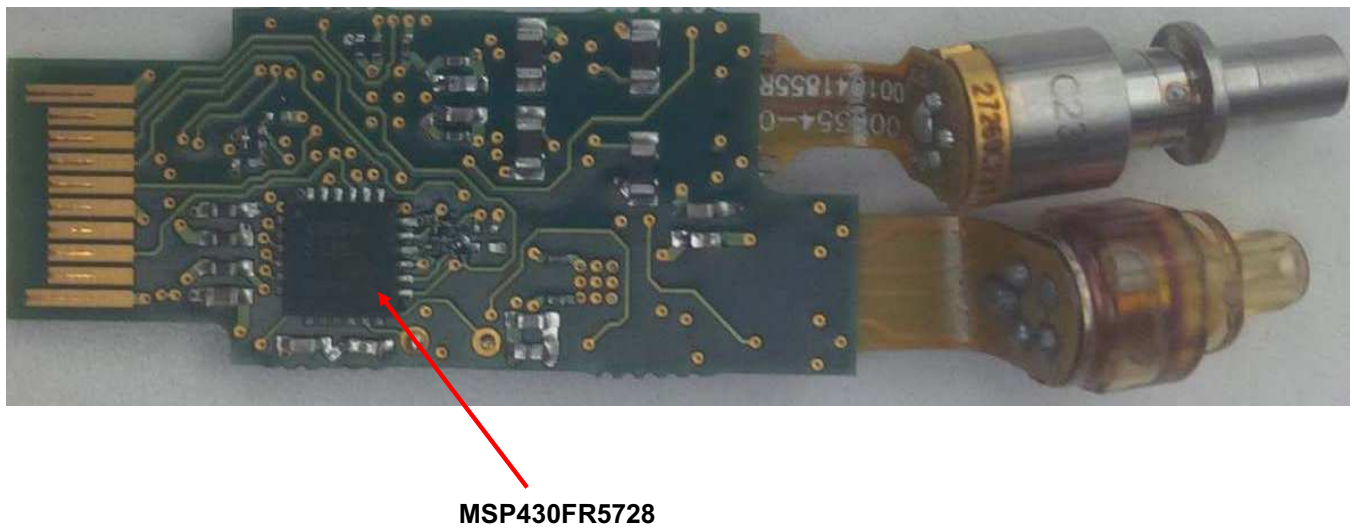
Figure 9. Module Bottom Side

Figure 10. Host Board
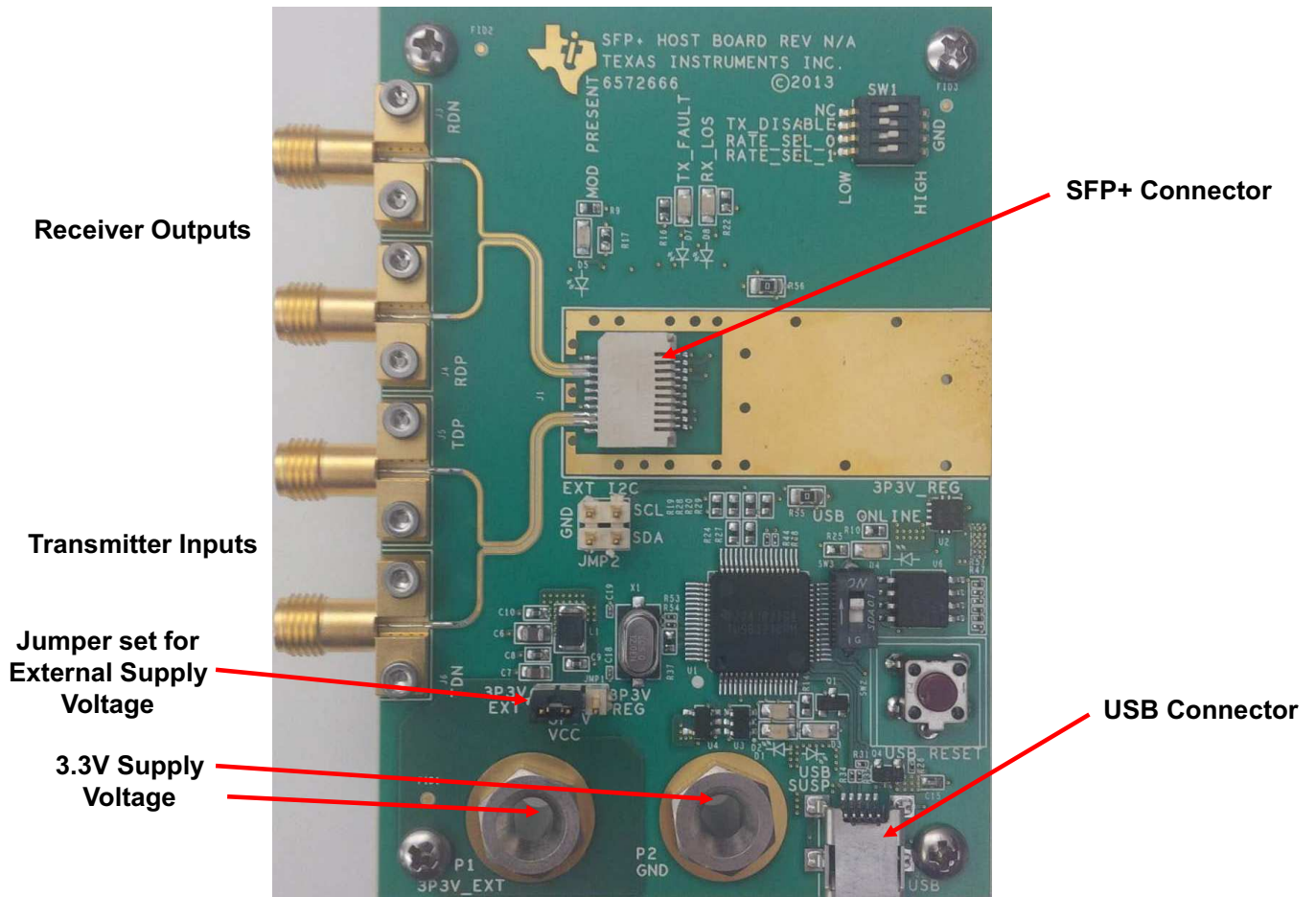
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3   Quick Set-Up Instructions

1. Run the GUI software executable file provided on the CD and follow the installation instructions.

2. Plug the SFP+ module into the SFP+ connector on the host board.

3. Connect a differential data-input signal source to the transmitter SMA connectors TDP/TDN. Set the data rate up to 11.3-Gbps and set the amplitude between 150-mVp-p differential and 1200-mVp-p differential.

4. Connect the receiver differential outputs RDP/RDN to the input of an oscilloscope.

5. Connect the TOSA output to the input of an oscilloscope.

6. Connect an optical source to the ROSA input.

7. Apply a 3.3-V supply to the 3.3-V banana jack and the supply ground to the GND banana jack (P1 and P2). The typical current consumption is about 122 mA.

8. Attach the interface cable from the USB port of the computer to the USB port on the host board. LEDs D1 and D4 light up green.

9. Set the TX_Disable switch (S1) to LOW.

10. Run the GUI by clicking on the desktop icon. Ensure that the EVM is powered on before the GUI is started.

11. Select *Device Configuration* for the ONET1151L or ONET1151P for high-level GUI control of each device. Alternatively, the *Low Level Register Interface* can be used to directly program the registers.

12. The ONET1151P powers up in default mode with all registers set to zero except for the the output amplitude register (Reg3) which is set to 0x02.

13. The ONET1151L powers up in a disabled state (Chip Enable = 0). To enable the device, click on *Chip Enable*.

14. For initial evaluation, open-loop operation is recommended. Select *Open Loop* and adjust the bias current to set the average optical power. Adjust the modulation current to set the extinction ratio.

15. The transmitter performance can be optimized by adjusting the de-emphasis, back termination resistance and the limiter stage bias currents.
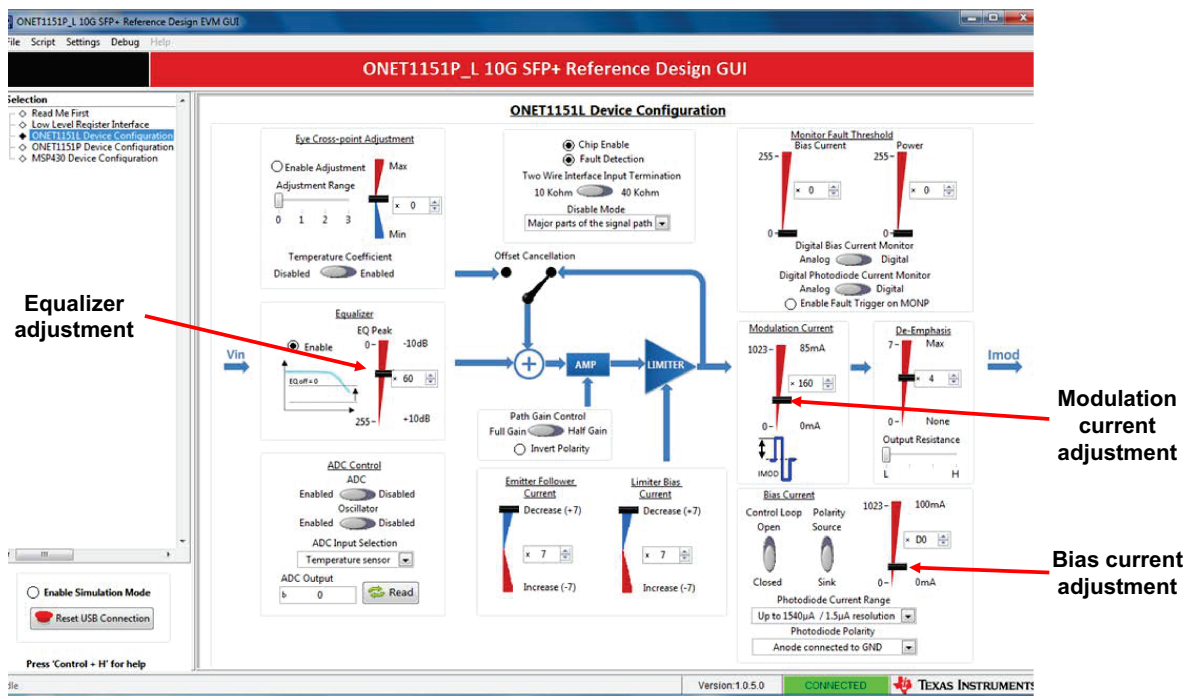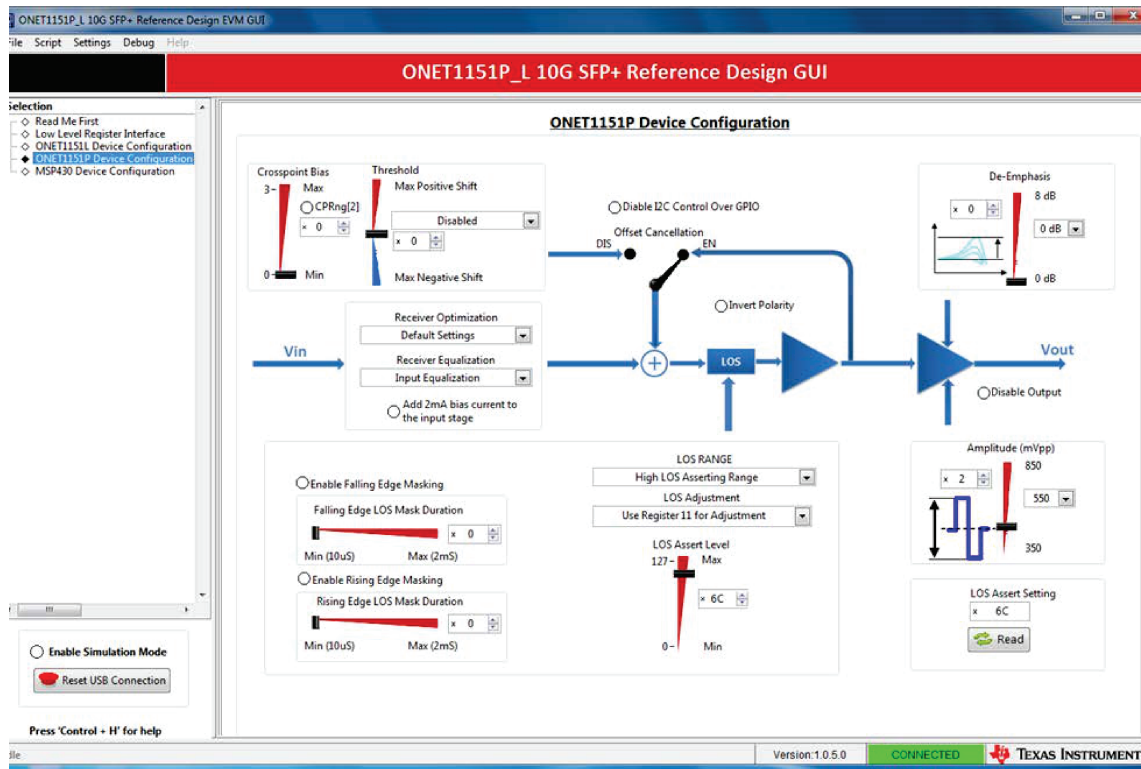

Figure 11. ONET1151L GUI

Figure 12. ONET1151P GUI

Register values can be modified directly with the *Low Level Register Interface* as shown in Figure 13.
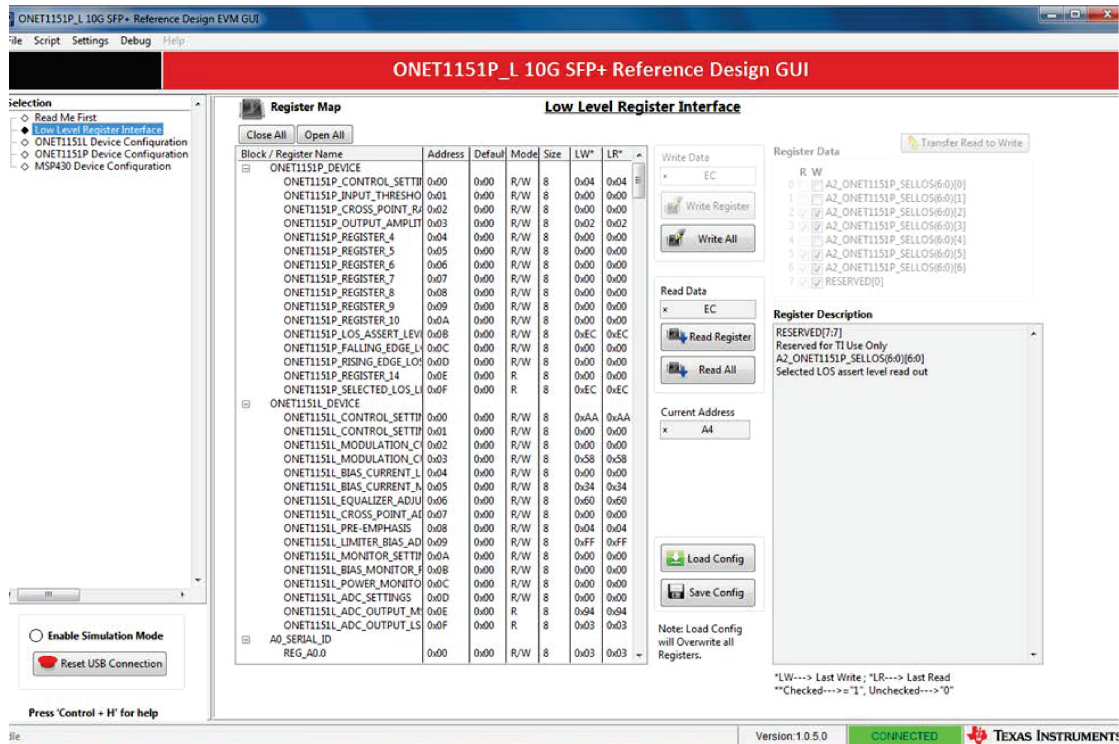

Figure 13. Low-Level Register Interface

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Once the module has been set-up, the register settings can first be transferred to A2 memory and then to FRAM for permanent storage and then recalled at power-up (see Figure 14).
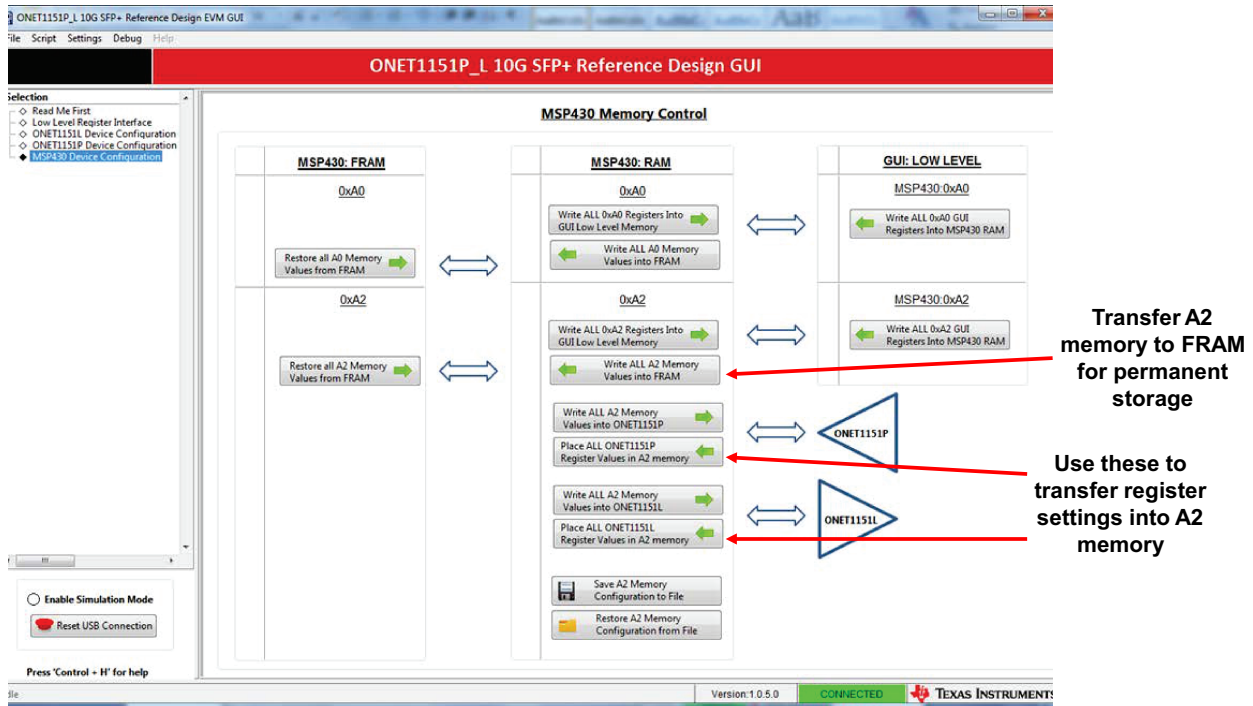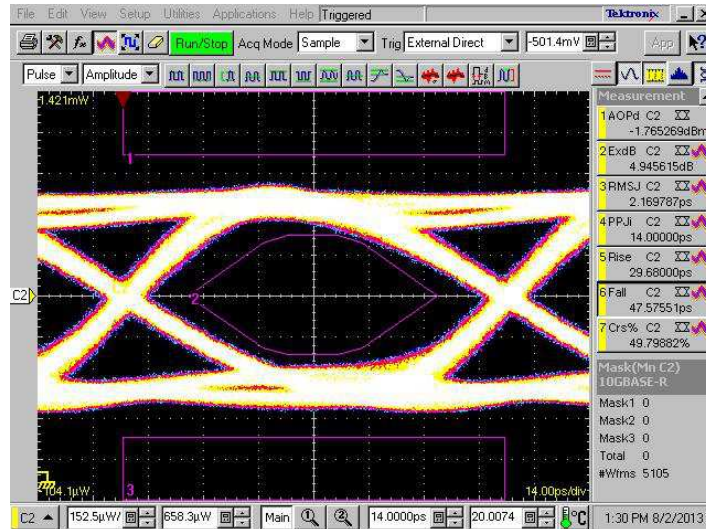

Figure 14. Register Storage in FRAM

4   Test Results

4.1   Module 1

Module 1 included the TX293k TOSA and TPS82693 step-down converter.

4.1.1   Module 1 Transmitter Optical Eye Diagrams

Reg0 = 0x82, Reg1 = 0x00, Reg2 = 0x00, Reg3 = 0x42 , Reg4 = 0x00, Reg5= 0x74 , Reg6 = 0x40, Reg7 = 0x00, Reg8 = 0x09, Reg9 = 0xFF, Reg10 = 0x00

**Figure 15. At –10°C Closed-Loop 10.3125-Gbps PRBS31-1 Pattern
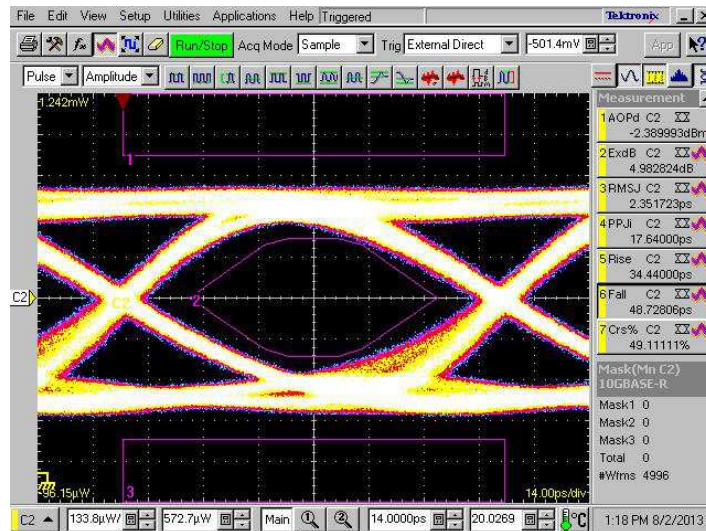VCC = 3.3 V, ICC = 179 mA, Power Dissipation = 591 mW, 31% Mask Margin**

NOTE: The module power dissipation is approximately 0.94 × 591 = 556 mW, assuming 94% efficiency in the regulator.
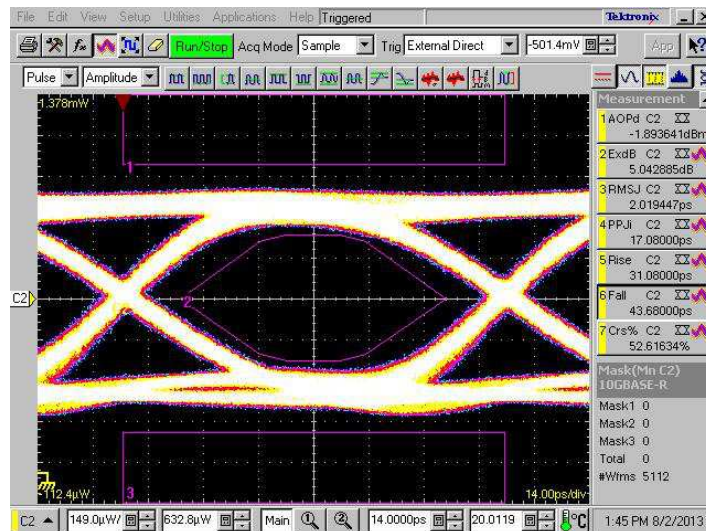
Reg0 = 0x82, Reg1 = 0x00, Reg2 = 0x00, Reg3 = 0x4C , Reg4 = 0x00, Reg5= 0x74 , Reg6 = 0x40, Reg7 = 0x00, Reg8 = 0x0B, Reg9 = 0xFF, Reg10 = 0x00

**Figure 16. At 25°C Closed-Loop 10.3125-Gbps PRBS31-1 Pattern
VCC = 3.3 V, ICC = 195 mA, Power Dissipation = 644 mW, 40% Mask Margin**

NOTE: The module power dissipation is approximately 0.94 × 644 = 605 mW, assuming 94% efficiency in the regulator.

Reg0 = 0x82, Reg1 = 0x00, Reg2 = 0x00, Reg3 = 0x68, Reg4 = 0x00, Reg5= 0x74 , Reg6 = 0x40, Reg7 = 0x00, Reg8 = 0x0B, Reg9 = 0xFF, Reg10 = 0x00

Figure 17. At 85°C Closed-Loop 10.3125-Gbps PRBS31-1 Pattern
VCC = 3.3 V, ICC = 244 mA, Power Dissipation = 805 mW, 30% Mask Margin

NOTE: The module power dissipation is approximately 0.94 × 805 = 757 mW, assuming 94% efficiency in the regulator.

4.1.2 Module 1 Receiver Eye Diagrams
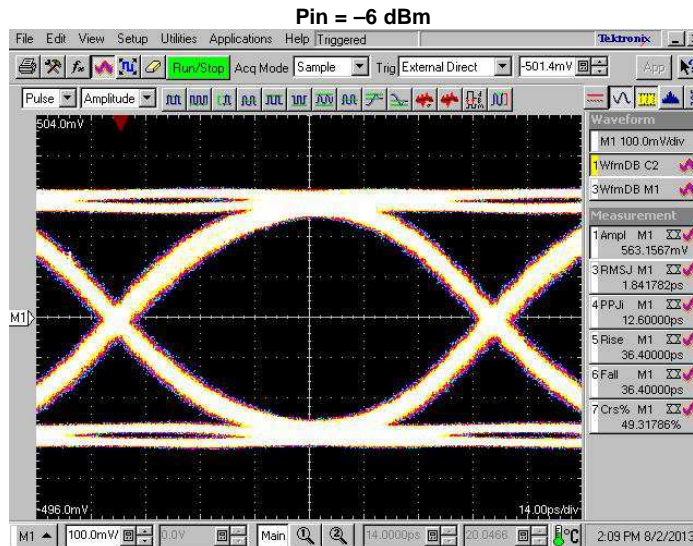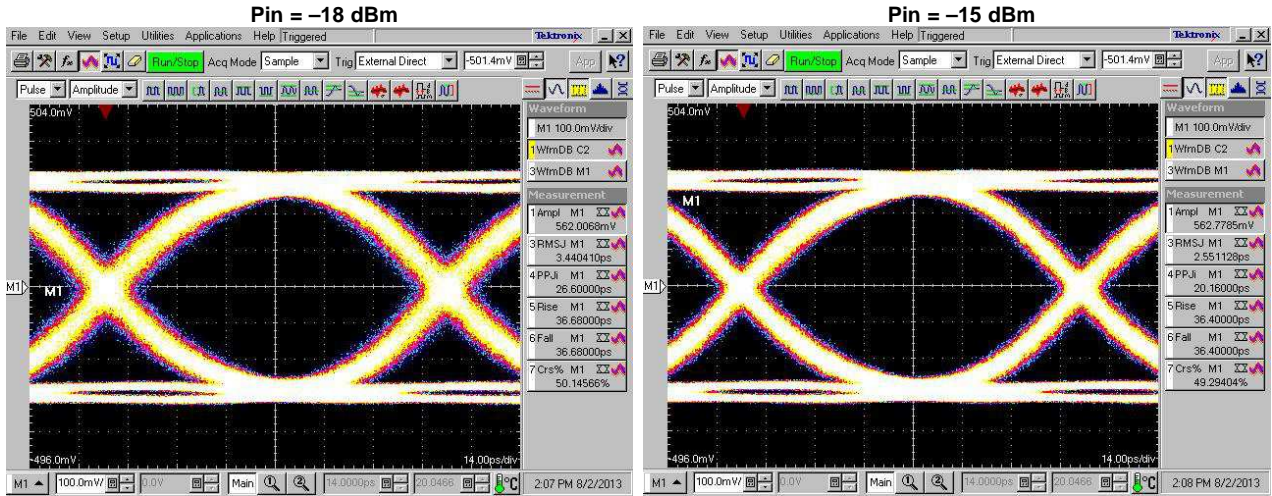
Pin = −18 dBm
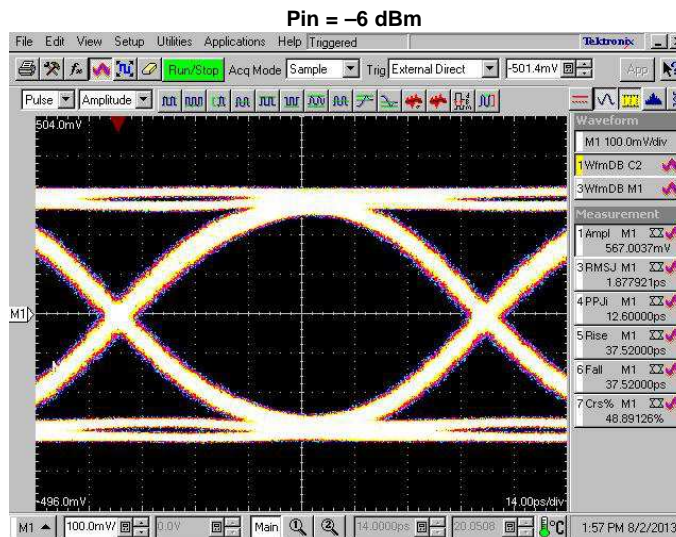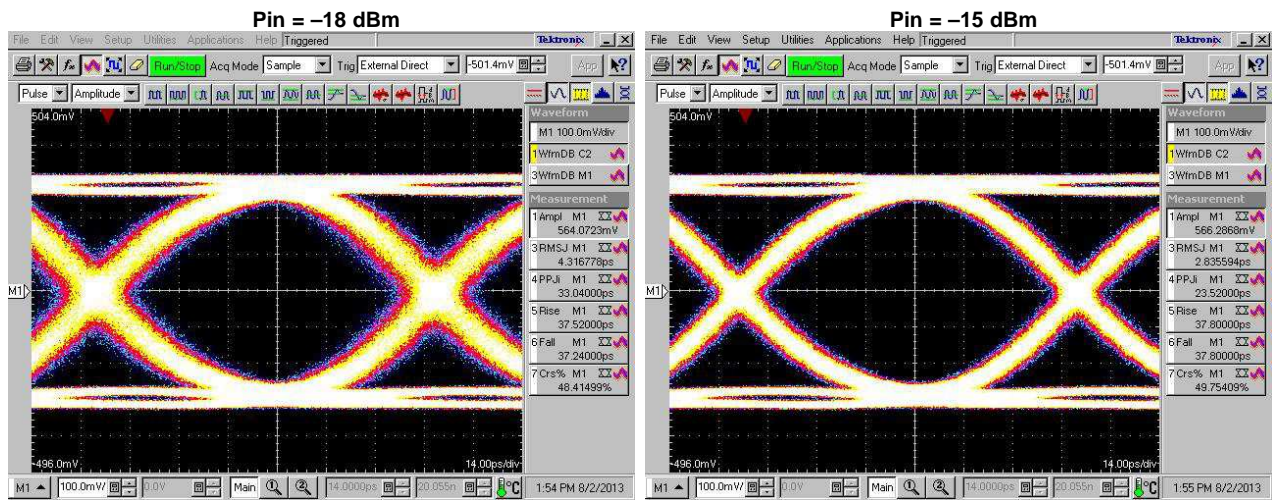
Pin = −15 dBm

Pin = −6 dBm

**Figure 18. At −10°C, 11-dB ER, 10.3125-Gbps, PRS31-1 Pattern
VCC = 3.3 V, ICC = 179 mA, Power Dissipation = 591 mW**

NOTE: The module power dissipation is approximately 0.94 × 591 = 556 mW, assuming 94% efficiency in the regulator.

Pin = –18 dBm

Pin = –15 dBm

Pin = –6 dBm

**Figure 19. At 25°C, 11-dB ER, 10.3125-Gbps, PRS31-1 Pattern
VCC = 3.3 V, ICC = 195 mA, Power Dissipation = 644 mW**

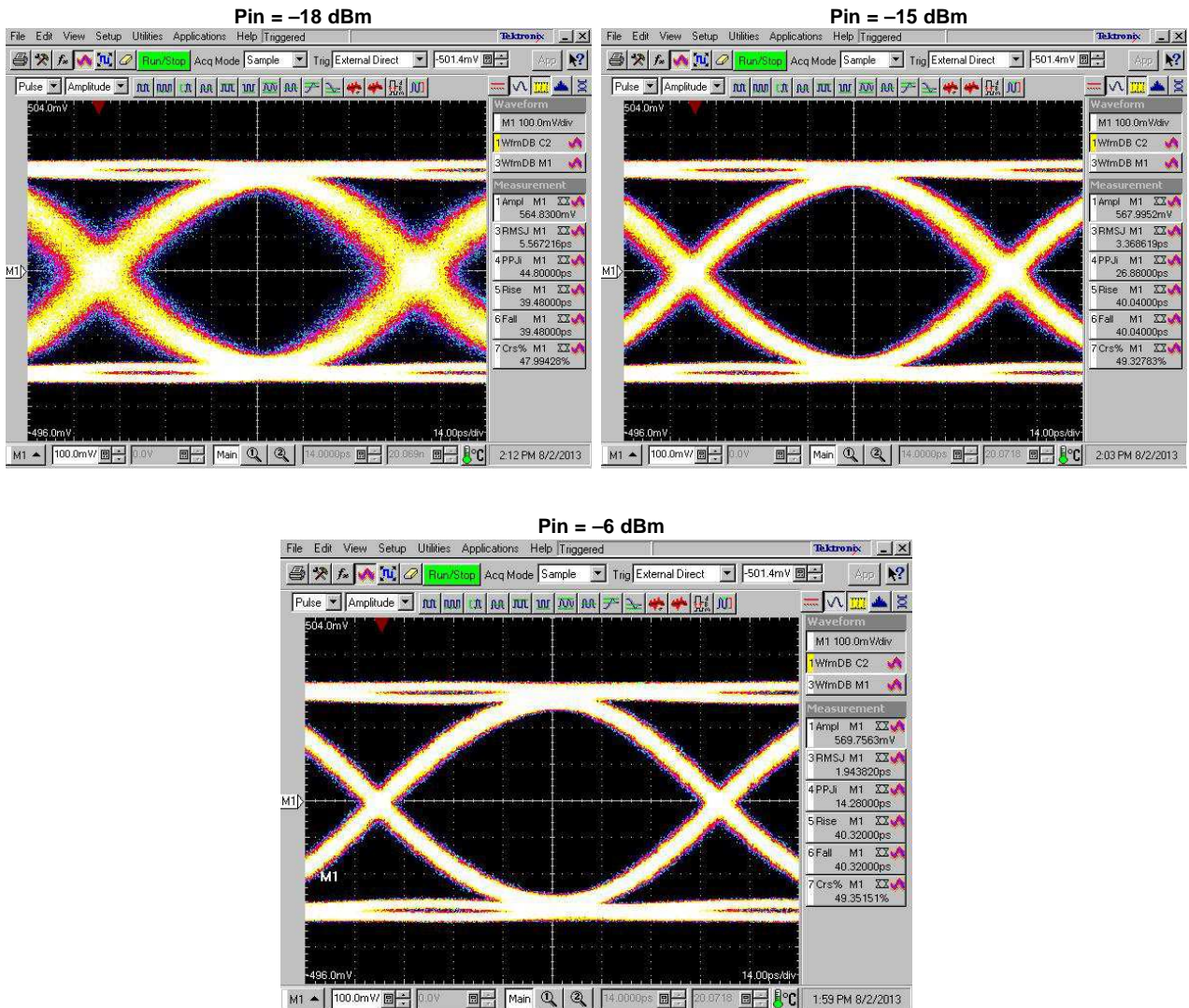**NOTE:** The module power dissipation is approximately 0.94 × 644 = 605 mW, assuming 94% efficiency in the regulator.

Pin = –18 dBm

Pin = –15 dBm

Pin = –6 dBm

Figure 20. At 85°C, 11-dB ER, 10.3125-Gbps, PRS31-1 Pattern
VCC = 3.3 V, ICC = 244 mA, Power Dissipation = 805 mW

NOTE: The module power dissipation is approximately 0.94 × 805 = 757 mW, assuming 94% efficiency in the regulator.
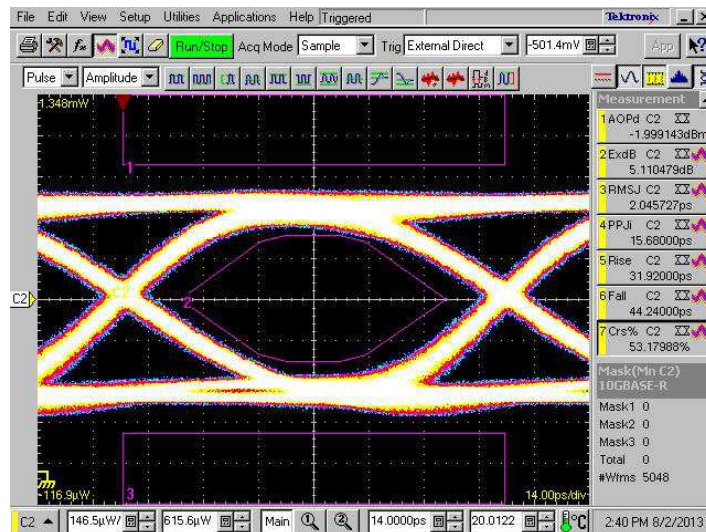
4.2 Module 2

Module 2 included the TX293K TOSA but not the TPS82693 step-down converter.

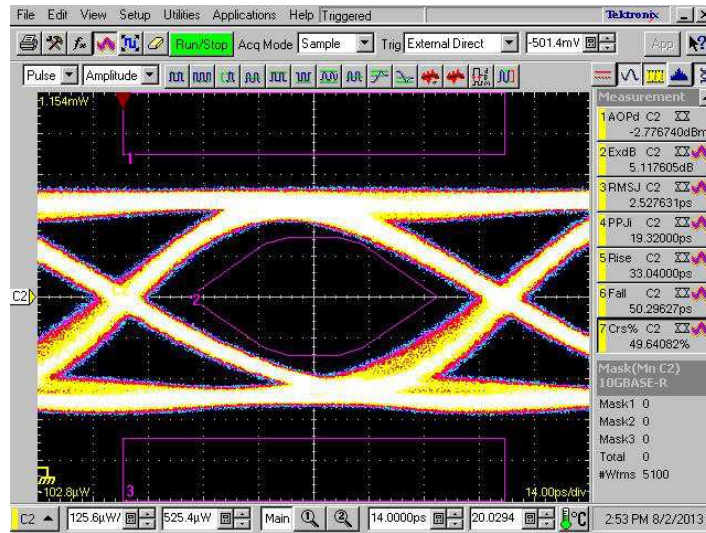### 4.2.1 Module 2 Transmitter Optical Eye Diagrams
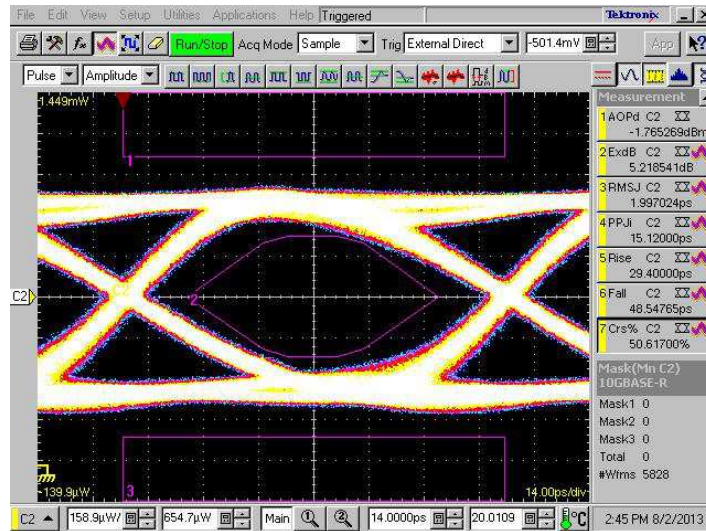
Reg0 = 0x82, Reg1 = 0x00, Reg2 = 0x00, Reg3 = 0x52 , Reg4 = 0x00, Reg5= 0x54 , Reg6 = 0x40, Reg7 = 0x00, Reg8 = 0x09, Reg9 = 0xFF, Reg10 = 0x00

Figure 21. At –10°C Closed-Loop 10.3125-Gbps PRBS31-1 Pattern
VCC = 2.85 V, ICC = 193 mA, Power Dissipation = 550 mW, 32% Mask Margin

Reg0 = 0x82, Reg1 = 0x00, Reg2 = 0x00, Reg3 = 0x58 , Reg4 = 0x00, Reg5= 0x54 , Reg6 = 0x40, Reg7 = 0x00, Reg8 = 0x0B, Reg9 = 0xFF, Reg10 = 0x00

Figure 22. At 25°C Closed-Loop 10.3125-Gbps PRBS31-1 Pattern
VCC = 2.85 V, ICC = 208 mA, Power Dissipation = 593 mW, 40% Mask Margin

Reg0 = 0x82, Reg1 = 0x00, Reg2 = 0x00, Reg3 = 0x74 , Reg4 = 0x00, Reg5= 0x54 , Reg6 = 0x40, Reg7 = 0x00, Reg8 = 0x09, Reg9 = 0xFF, Reg10 = 0x00

Figure 23. At 85°C Closed-Loop 10.3125-Gbps PRBS31-1 Pattern
VCC = 2.85 V, ICC = 260 mA, Power Dissipation = 741 mW, 30% Mask Margin
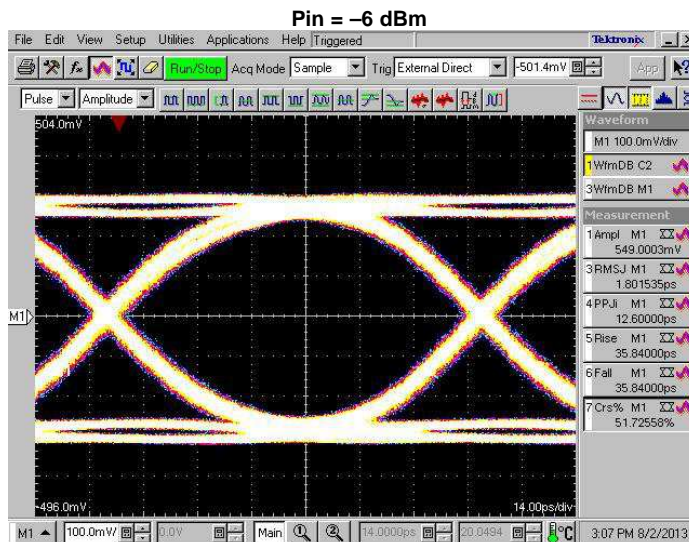
4.2.2 Module 2 Receiver Eye Diagrams
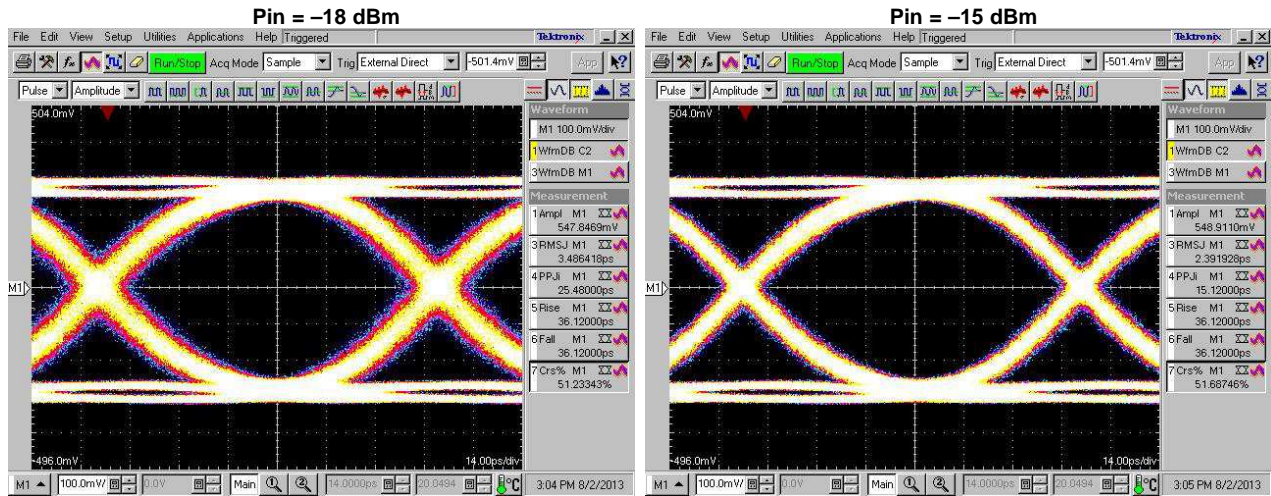
Pin = −18 dBm

Pin = −15 dBm

Pin = −6 dBm

Figure 24. At −10°C, 11-dB ER, 10.3125-Gbps, PRS31-1 Pattern
VCC = 2.85 V, ICC = 193 mA, Power Dissipation = 550 mW

Pin = –18 dBm

Pin = –15 dBm

Pin = –6 dBm

**Figure 25. At 25°C, 11-dB ER, 10.3125-Gbps, PRS31-1 Pattern
VCC = 2.85 V, ICC = 208 mA, Power Dissipation = 593 mW**

Pin = –18 dBm

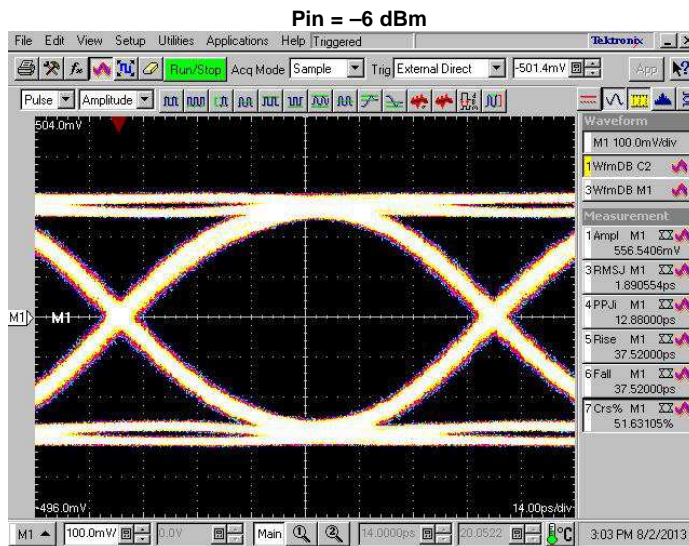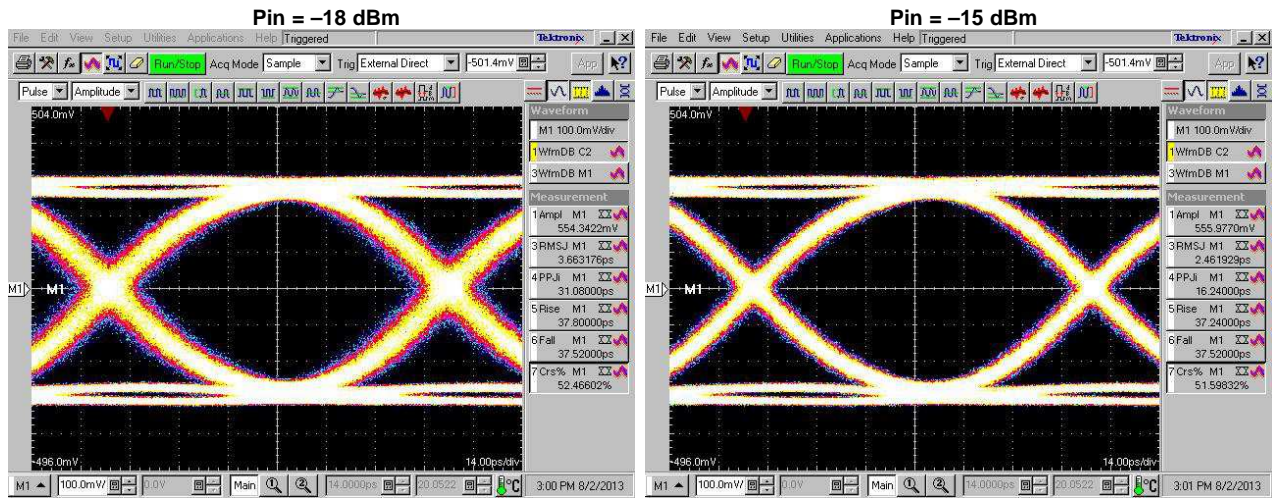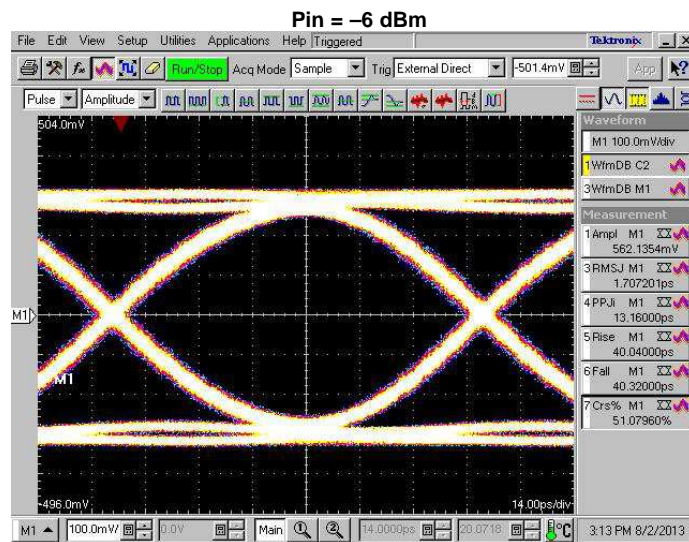**Pin = –15 dBm**

Pin = –6 dBm

**Figure 26. At 85°C, 11-dB ER, 10.3125-Gbps, PRS31-1 Pattern
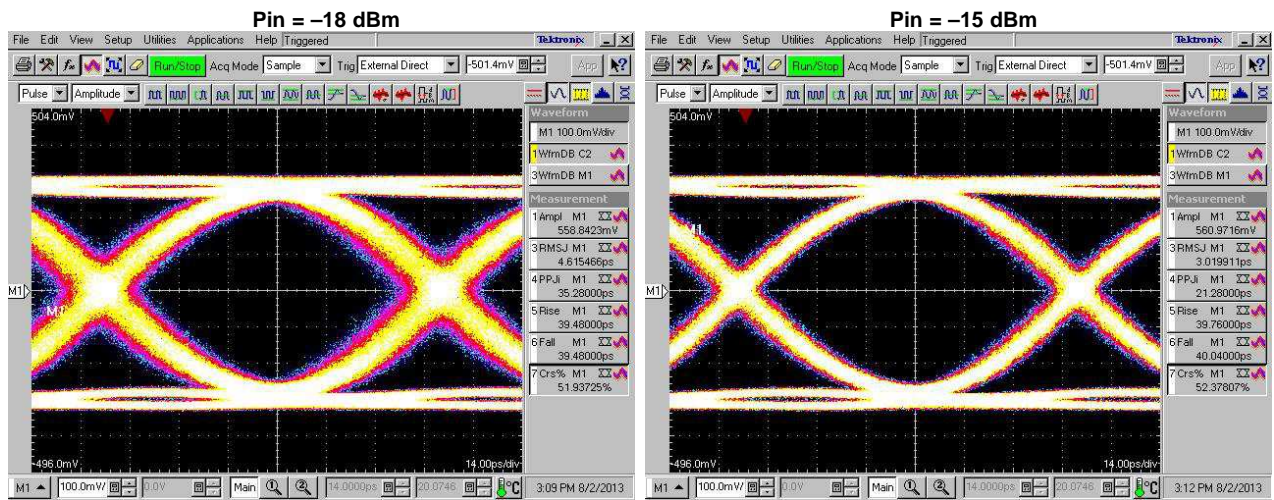VCC = 2.85 V, ICC = 260 mA, Power Dissipation = 741 mW**

4.3   Transmitter Test Results With the NX8349TS TOSA

4.3.1   Transmitter Optical Eye Diagrams
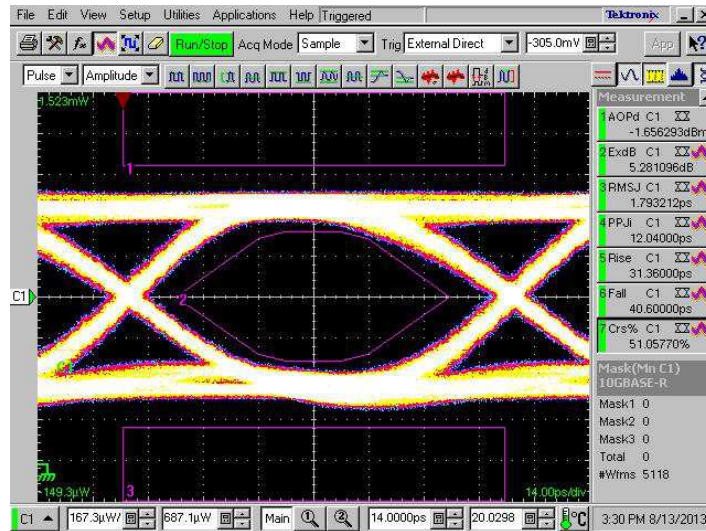
Reg0 = 0x8A, Reg1 = 0x00, Reg2 = 0x00, Reg3 = 0x50 , Reg4 = 0x00, Reg5= 0x78 , Reg6 = 0x60, Reg7 = 0x00, Reg8 = 0x07, Reg9 = 0x00, Reg10 = 0x00

Figure 27. At –10°C Closed-Loop 10.3125-Gbps PRBS31-1 Pattern
VCC = 3.3 V, ICC = 186 mA, Power Dissipation = 614 mW, 44% Mask Margin

Reg0 = 0x8A, Reg1 = 0x00, Reg2 = 0x00, Reg3 = 0x58 , Reg4 = 0x00, Reg5= 0x78 , Reg6 = 0x60, Reg7 = 0x00, Reg8 = 0x07, Reg9 = 0x00, Reg10 = 0x00

Figure 28. At 25°C Closed-Loop 10.3125-Gbps PRBS31-1 Pattern
VCC = 3.3 V, ICC = 202 mA, Power Dissipation = 667 mW, 42% Mask Margin

Reg0 = 0x8A, Reg1 = 0x00, Reg2 = 0x00, Reg3 = 0x70 , Reg4 = 0x00, Reg5= 0x78 , Reg6 = 0x60, Reg7 = 0x00, Reg8 = 0x07, Reg9 = 0x00, Reg10 = 0x00

Figure 29. At 85°C Closed-Loop 10.3125-Gbps PRBS31-1 Pattern
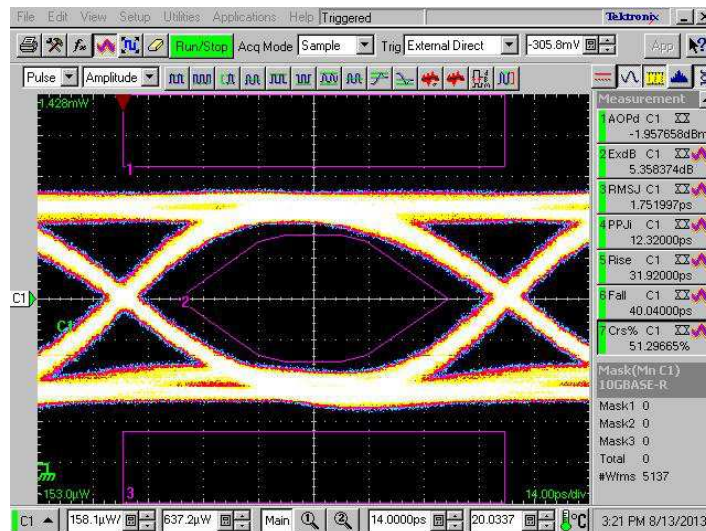**VCC = 3.3 V, ICC = 253 mA, Power Dissipation = 835 mW, 30% Mask Margin**

4.4 Transmitter Test Results With the NX8349TB TOSA

4.4.1 Transmitter Optical Eye Diagrams

Reg0 = 0x80, Reg1 = 0x00, Reg2 = 0x00, Reg3 = 0x68 , Reg4 = 0x00, Reg5= 0x9C , Reg6 = 0x00, Reg7 = 0x00, Reg8 = 0x07, Reg9 = 0xFF, Reg10 = 0x00

Figure 30. At –20°C Closed-Loop 10.3125-Gbps PRBS31-1 Pattern
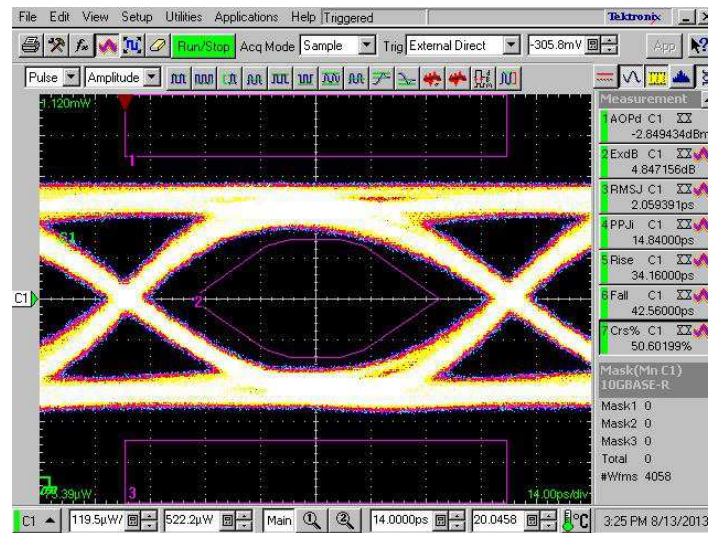**VCC = 3.3 V, ICC = 193 mA, Power Dissipation = 637 mW, 40% Mask Margin**

Reg0 = 0x80, Reg1 = 0x00, Reg2 = 0x00, Reg3 = 0x70 , Reg4 = 0x00, Reg5= 0x9C , Reg6 = 0x00, Reg7 = 0x00,
Reg8 = 0x07, Reg9 = 0xFF, Reg10 = 0x00

**Figure 31. At 25°C Closed-Loop 10.3125-Gbps PRBS31-1 Pattern
VCC = 3.3 V, ICC = 209 mA, Power Dissipation = 690 mW, 42% Mask Margin**

Reg0 = 0x80, Reg1 = 0x00, Reg2 = 0x00, Reg3 = 0x98 , Reg4 = 0x00, Reg5= 0x9C , Reg6 = 0x00, Reg7 = 0x00,
Reg8 = 0x07, Reg9 = 0xFF, Reg10 = 0x00

**Figure 32. At 85°C Closed-Loop 10.3125-Gbps PRBS31-1 Pattern
VCC = 3.3 V, ICC = 270 mA, Power Dissipation = 891 mW, 32% Mask Margin**
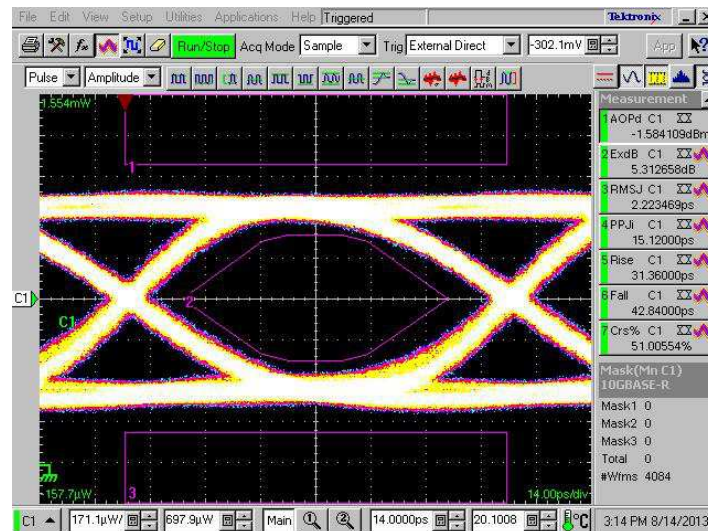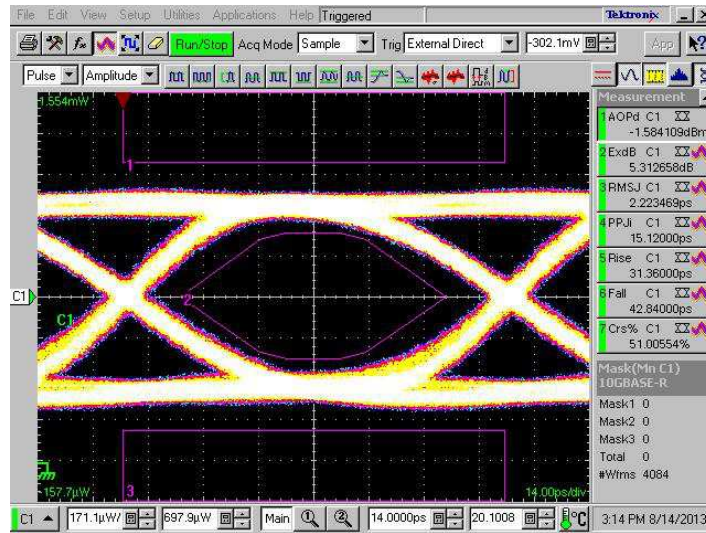
Reg0 = 0x80, Reg1 = 0x00, Reg2 = 0x00, Reg3 = 0x88 , Reg4 = 0x00, Reg5= 0x9C , Reg6 = 0x00, Reg7 = 0x00, Reg8 = 0x07, Reg9 = 0xFF, Reg10 = 0x00

Figure 33. At –20°C Closed-Loop 9.95-Gbps PRBS31-1 Pattern
VCC = 3.3 V, ICC = 212 mA, Power Dissipation = 700 mW, 16% Mask Margin

Reg0 = 0x80, Reg1 = 0x00, Reg2 = 0x00, Reg3 = 0x90 , Reg4 = 0x00, Reg5= 0x9C , Reg6 = 0x00, Reg7 = 0x00, Reg8 = 0x07, Reg9 = 0xFF, Reg10 = 0x00

Figure 34. At 25°C Closed-Loop 9.95-Gbps PRBS31-1 Pattern
VCC = 3.3 V, ICC = 234 mA, Power Dissipation = 772 mW, 22% Mask Margin
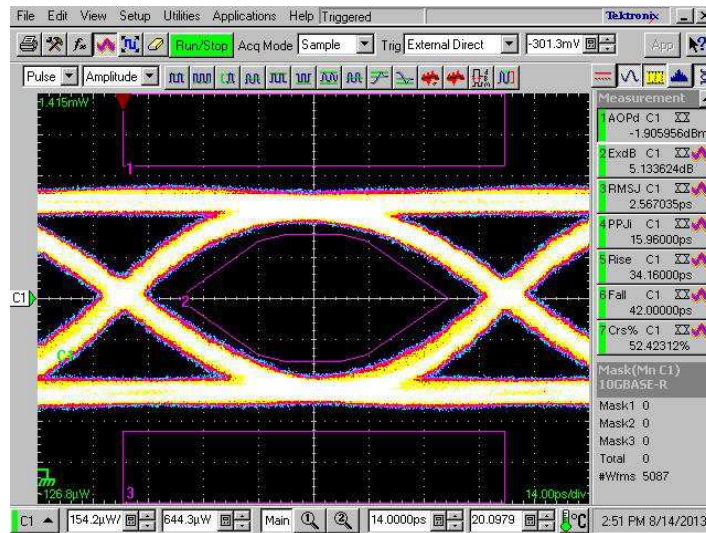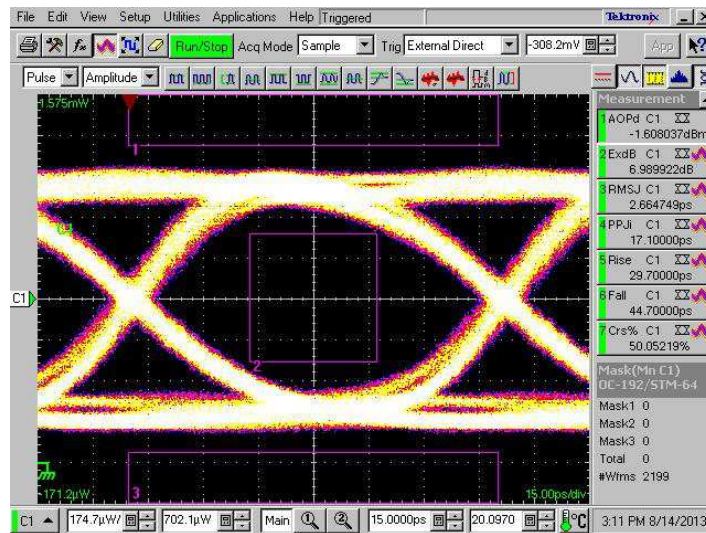
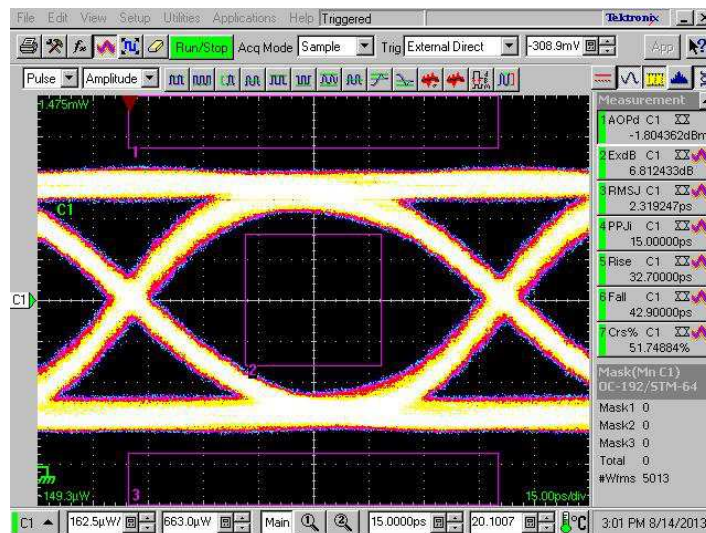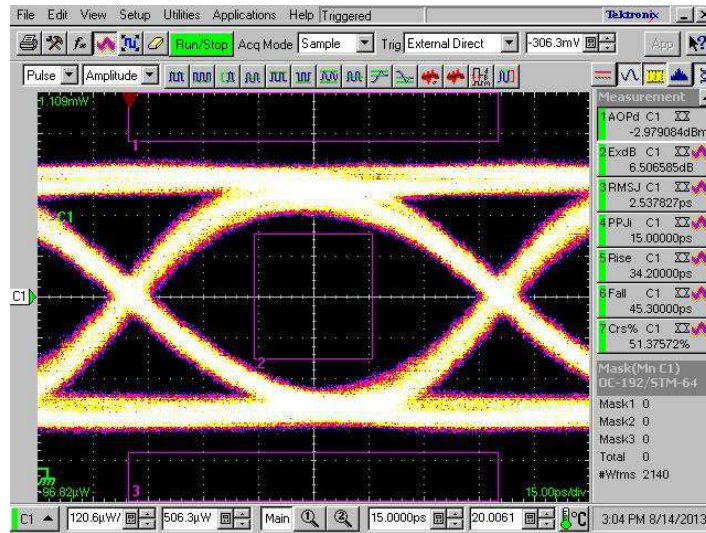Reg0 = 0x80, Reg1 = 0x00, Reg2 = 0x00, Reg3 = 0xB8 , Reg4 = 0x00, Reg5= 0x9C , Reg6 = 0x00, Reg7 = 0x00,
Reg8 = 0x07, Reg9 = 0xFF, Reg10 = 0x00

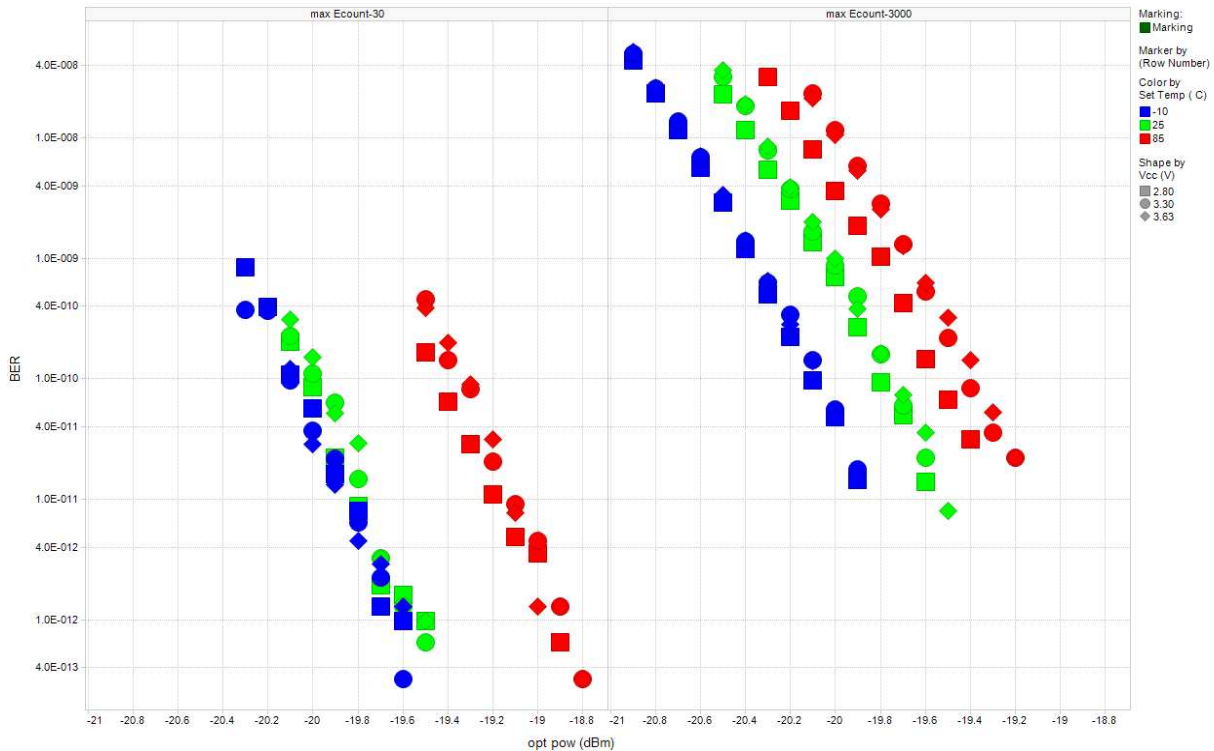**Figure 35. At 85°C Closed-Loop 9.95-Gbps PRBS31-1 Pattern**
VCC = 3.3 V, ICC = 284 mA, Power Dissipation = 937 mW, 15% Mask Margin

4.5 Typical Receiver Test Results

Figure 36. Receiver BER Versus Optical Input Power
10.3125-Gbps PRBS31-1 Pattern

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