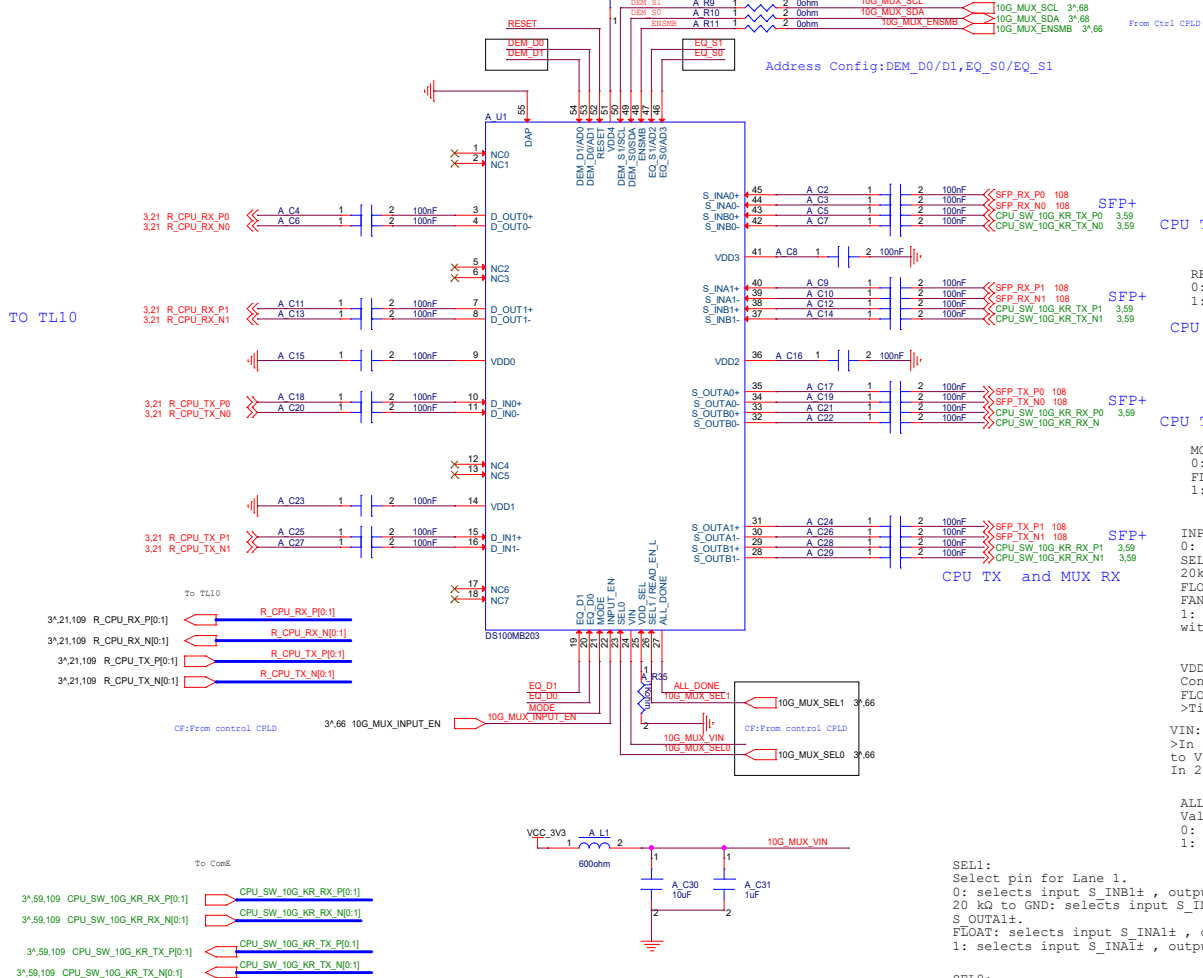


10G MUX Add netlist

To Control CPLD
 1.10G_MUX_ENSMB
 2.10G_MUX_SEL1
 3.10G_MUX_SELO
 4.10G_MUX_INPUT_EN

DS100MB203 default address
 0x67 (7'b 110 0111)



TO TL10

To Com2

SELO	SEL1	INPUT_EN	
1	1	0	D_OUT0 connects to S_INA0. D_OUT1 connects to S_INA1. D_IN0 connects to S_OUTA0. S_OUTB0 is in IDLE (output muted). D_IN1 connects to S_OUTA1. S_OUTB1 is in IDLE (output muted).

Table 6. Device Slave Address Bytes

AD[3:0] SETTINGS	ADDRESS BYTES (HEX)
0000	B0
0001	B2
0010	B4
0011	B6
0100	B8
0101	BA
0110	BC
0111	BE
1000	C0
1001	C2
1010	C4
1011	C6
1100	C8
1101	CA
1110	CC
1111	CE

CPU TX and MUX RX

CPU TX and MUX RX

CPU TX and MUX RX

RESET:
 0: Normal operation (device is enabled).
 1: Low power mode.

MODE:
 0: SATA/SAS, PCIe Gen 1/2 and 10GE
 FLOAT: AUTO (PCIe Gen 1/2 or GEN 3)
 1: 10G-KR

INPUT_EN:
 0: Normal operation, FANOUT is disabled, use SEL0/1 to select the A or B input/output (see SEL0/1 pin), input always enabled with 50 Ω.
 20kΩ to GND: Reserved
 FLOAT: AUTO - Use RX Detect, SEL0/1 to determine which input or output to enable, FANOUT is disable
 1: Normal operation, FANOUT is enabled (both S_OUT0/1 are ON). Input always enabled with 50 Ω.

VDD_SEL:
 Controls the internal regulator
 FLOAT: 2.5-V mode
 >Tied to GND: 3.3-V mode

VIN:
 >In 3.3-V mode, feed 3.3 V ± 10% to VIN
 In 2.5-V mode, leave floating.

ALL_DONE:
 Valid Register Load Status Output
 0: External EEPROM load passed
 1: External EEPROM load failed

SEL1:
 Select pin for Lane 1.
 0: selects input S_INB1±, output S_OUTB1±.
 20 kΩ to GND: selects input S_INB1±, output S_OUTA1±.
 FLOAT: selects input S_INA1±, output S_OUTB1±.
 1: selects input S_INA1±, output S_OUTA1±.

SEL0:
 Select pin for Lane 0.
 0: selects input S_INB0±, output S_OUTB0±.
 20 kΩ to GND: selects input S_INB0±, output S_OUTA0±.
 FLOAT: selects input S_INA0±, output S_OUTB0±.
 1: selects input S_INA0±, output S_OUTA0±.

