TEXAS INSTRUMENTS INCORPORATED

DS90UH947-Q1

1080p OLDI to FPD-Link III Bridge Serializer with HDCP

Implementation of ODD and EVEN Pixels on FPD-Link III Outputs

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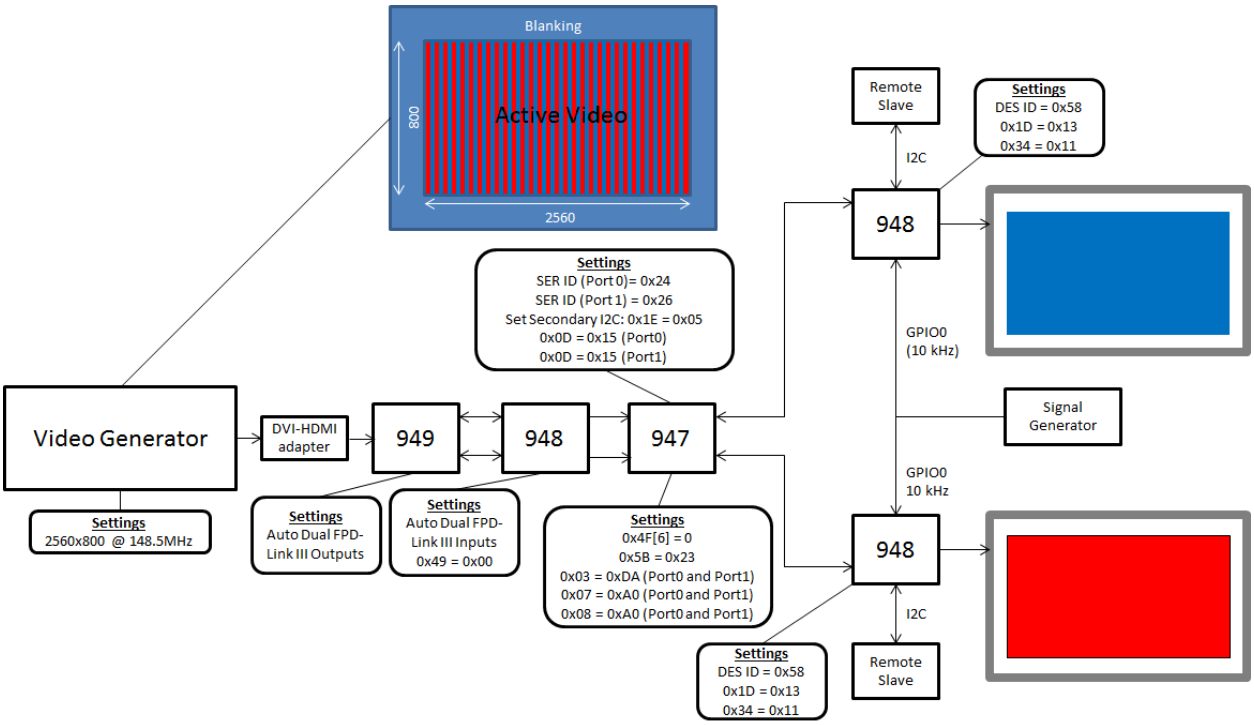
Contents

1) Objective

To assess the feasibility of sending two video streams combined as one, and split the combined video stream into two separate FPD-Link III outputs to two separate deserializers and two displays. I2C and GPIO operation will also be checked.

2) Bench Test Setup



- ASTRO VG-835 video generator was used to generated the HDMI input into the DS90UH949-Q1.
- 1x DS90UH949-Q1EVM, 1x DS90UH947-Q1EVM, 3x DS90UB948-Q1EVM were used.
- To generate the interleaving column pattern, the ASTRO VG-835 video generator was used that has HDMI output.
    - To interface the video generator with the DS90UH947, a DS90UH949 -> DS90UH948 was used to translate the interface from HDMI to OLDI. The DS90UH948's OLDI outputs were then used to drive the DS90UH947 OLDI inputs, which then drove two separate DS90UH948 on the display side.
- Onboard USB2ANY I2C interface was used to configure the chipsets.
- GPIO (at 10kHz) and I2C passthrough with remote slaves at each 948 on display side were also validated.

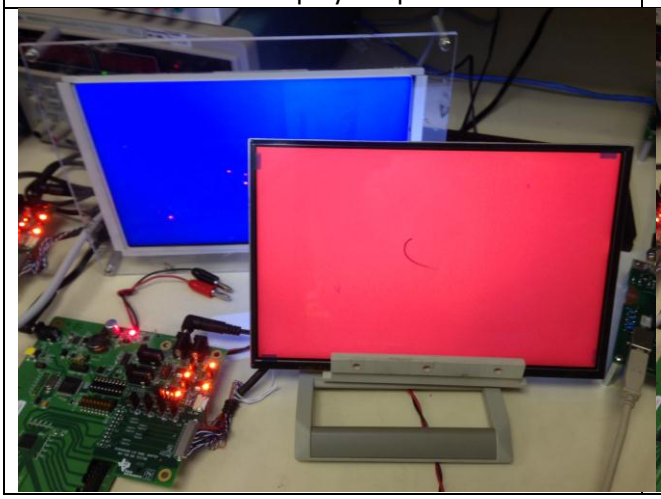
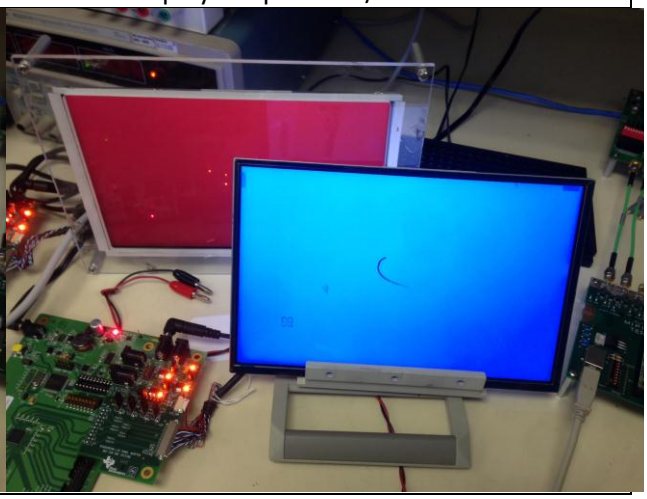
3) Test Conditions

VDD11/ VDD18 / VDDI2C	HDMI Clock	949 Output Mode	1st 948 Input/Output Mode	947 Input/Output Mode	2nd Tier 948 Input Mode	Final PCLK
1.1 / 1.8 V / 3.3V	148.5MHz	Dual	Dual/Dual	Dual/Dual	Single	74.25MHz

4) Procedure

a) Connect 949 EVM to 948 EVM.
b) Power on all EVMs using 12V power adapters.
c) Configure video generator to send striped-column pattern at 2560x800 resolution using 148.5MHz PCLK.
d) The 949 should auto-detect into Dual FPD-Link III Output Mode.
e) The 948 should auto-detect into Dual FPD-Link III Input Mode.
f) Set 948 to Dual OLDI Output: 0x49 = 0x00.
g) Set 947 to Dual OLDI Input: 0x4F[6] = 0 and Dual FPD-Link III Output: 0x5B = 0x23.
h) Set each 948 to FPD-Link III Single Input: 0x34 = 0x11.
i) Set each 948 to GPIO0 as input: 0x1D = 0x13.
j) Enable secondary I2C on 947: 0x0x1E = 0x05.
k) Set 947 GPIO0 and D_GPIO0 as output: 0x0D = 0x15 (Port0 and Port1).
l) Set remote slave ID on 947 (0x18 and 0x1A): 0x07 = 0xA0 and 0x08 = 0xA0.
m) Input test signal into each 948 and check GPIO outputs on 947's GPIO0 and D_GPIO0.
n) Validate I2C operation on each remote slave of 948.

5) Results

948 Display Output	948 Display Output ODD/EVEN Inverted
	

- Each 948 is showing ODD and EVEN pixels on their respective displays as expected.
- 10kHz signal input into GPIO0 of each 948 shows up on 949's GPIO0 and D_GPIO0.
- Remote I2C operation works between the devices, and remote slave access is also possible on each port from 947 -> each 948's remote slave.

6) Conclusion

Based on the above test results, splitting of ODD and EVEN pixels from OLDI inputs to FPD-Link III outputs is feasible.

Revision History

Revision	Date	Author	Comments
01	12/24/2014	Tran Dam	Initial report