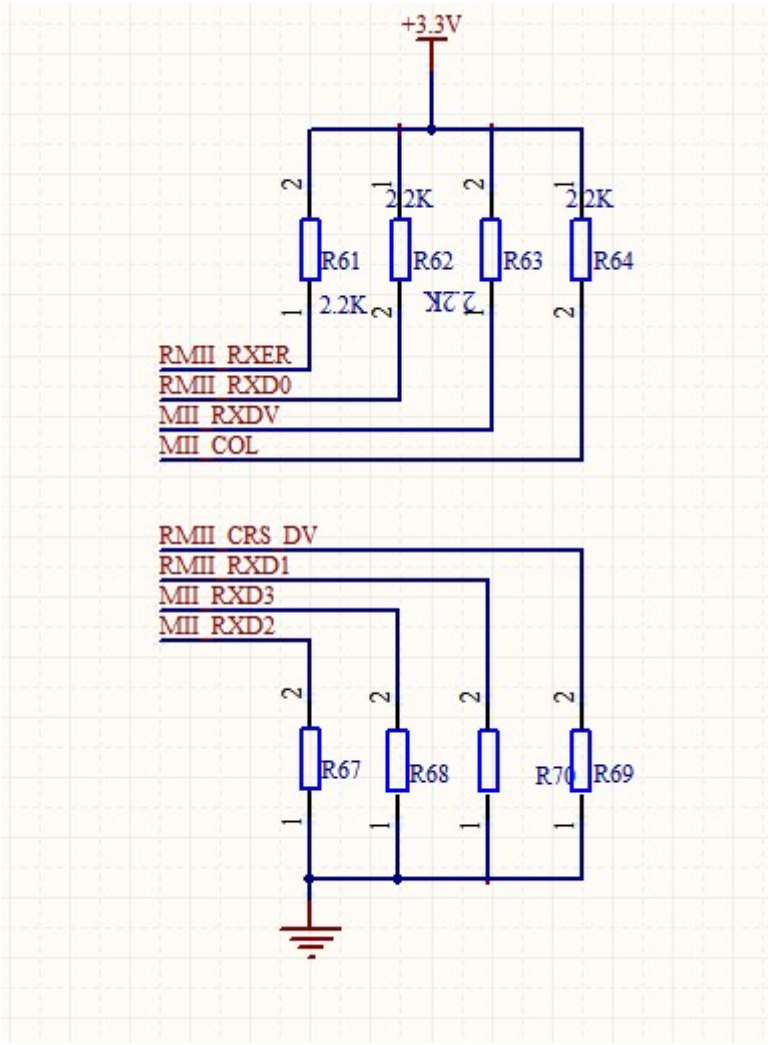
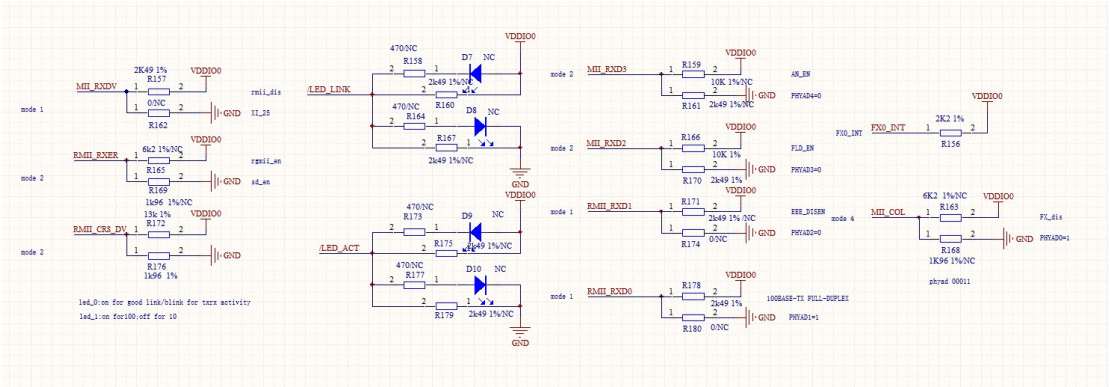
1、



DP83848 configuration

2、



DP83822 configuration

表 11. 4-Level Strap Pins

PIN NAME	PIN #	DEFAULT	STRAP FUNCTION			DESCRIPTION
COL	29	[01]	**MODE**	**FX_EN**	**PHY_AD0**	**FX_EN:** Enables 100BASE-FX when set to '1' **PHY_AD0:** PHY Address bit[0]
			1	0	0	
			2	1	0	
			3	1	1	
			4 (Default)	**0**	**1**	
RX_D0	30	[10]	**MODE**	**AN_1**	**PHY_AD1**	**AN_1:** See 表 12 below **PHY_AD1:** PHY Address bit[1]
			1 (Default)	**1**	**0**	
			2	0	0	
			3	0	1	
			4	1	1	
RX_D1	31	[00]	**MODE**	**EEE_EN**	**PHY_AD2**	**EEE_EN:** Enables EEE operation when set to '1' **PHY_AD2:** PHY Address bit [2]
			1 (Default)	**0**	**0**	
			2	1	0	
			3	1	1	
			4	0	1	
RX_D2	32	[00]	**MODE**	**FLD_EN**	**PHY_AD3**	**FLD_EN:** Enables Fast Link Drop when set to '1'. Energy Detection, Low SNR threshold and RX_ER will be enabled. **PHY_AD3:** PHY Address bit[3]
			1 (Default)	**0**	**0**	
			2	1	0	
			3	1	1	
			4	0	1	
RX_D3	1	[10]	**MODE**	**AN_EN**	**PHY_AD4**	**AN_EN:** See 表 12 below **PHY_AD4:** PHY Address bit[4]
			1 (Default)	**1**	**0**	
			2	0	0	
			3	0	1	
			4	1	1	
LED_0	17	[X1]	**MODE**	**RESERVED**	**AN_0**	**AN_0:** See 表 12 below
			1	X	0	
			2	X	0	
			3	X	1	
			4 (Default)	X	**1**	
CRS	27	[01]	**MODE**	**LED_SPEED**	**LED_CFG**	**LED_CFG:** See 表 13 below **LED_SPEED:** See 表 14 below
			1	0	0	
			2	1	0	
			3	1	1	
			4 (Default)	**0**	**1**	
RX_ER	28	[01]	**MODE**	**RGMII_EN**	**AMDIX_EN** ***(SD_EN)***	**AMDIX_EN:** Enables Auto-MDIX when set to '1' **RGMII_EN:** See 表 15 below **SD_EN:** Enables 100BASE-FX Signal Detection on LED_1 when set to '1'. FX_EN strap must be enabled for SD_EN strap to be functional. Signal Detection is Active LOW, but polarity can be changed using the General Configuration Register (GENCFG, address 0x0465).
			1	0	0	
			2	1	0	
			3	1	1	
			4 (Default)	**0**	**1**	

表 11. 4-Level Strap Pins (接下页)

PIN NAME	PIN #	DEFAULT	STRAP FUNCTION			DESCRIPTION
RX_DV	26	[00]	MODE	XI_50	RMII_EN	XI_50: See 表 15 below RMII_EN: See 表 15 below
			1 (Default)	0	0	
			2	1	0	
			3	0	1	
			4	1	1	

表 12. Modes of Operation

FX_EN	AN_EN	AN_1	AN_0	Description
Force Modes				
0	0	0	0	10BASE-Te, Half-Duplex
0	0	0	1	10BASE-Te, Full-Duplex
0	0	1	0	100BASE-TX, Half-Duplex
0	0	1	1	100BASE-TX, Full-Duplex
Advertised Modes				
0	1	0	0	10BASE-Te, Half-Duplex
0	1	0	1	10BASE-Te, Half/Full-Duplex
0	1	1	0	10BASE-Te, Half-Duplex 100BASE-TX, Half-Duplex
0	1	1	1	10BASE-Te, Half/Full-Duplex 100BASE-TX, Half/Full-Duplex
Fiber Modes				
1	X	X	0	100BASE-FX, Half Duplex
1	X	X	1	100BASE-FX, Full Duplex

表 13. LED_0 Configuration

Strap Mode	LED_CFG[0]	LED_0
4 & 3	1	ON for Good Link OFF for No Link
2 & 1	0	ON for Good Link BLINK for TX/RX Activity

表 14. LED_1 Configuration

Strap Mode	LED_SPEED	LED_1
4 & 1	0	LED_1 in Tri-State
3 & 2	1	ON for 100 Mbps SPEED OFF for 10 Mbps SPEED

表 15. MAC Interface Configuration

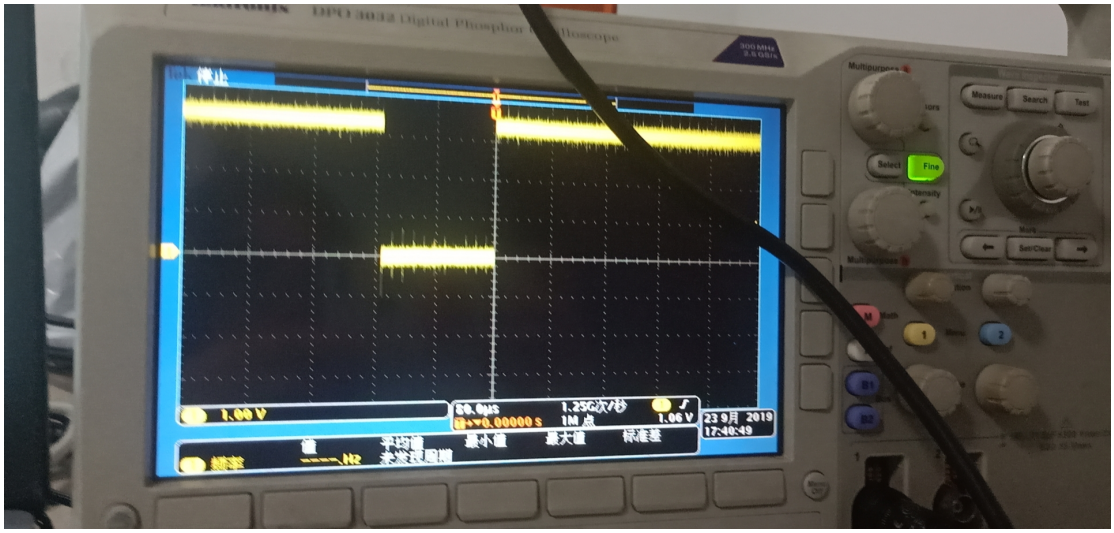
RGMII_EN	RMII_EN	XI_50	Description
0	0	0	MII, 25-MHz Reference Clock
0	0	1	**Reserved**
0	1	0	RMII, 25-MHz Reference Clock
0	1	1	RMII, 50-MHz Reference Clock
1	X	0	RGMII, 25-MHz Reference Clock
1	X	1	**Reserved**

Yellow marked as configuration information

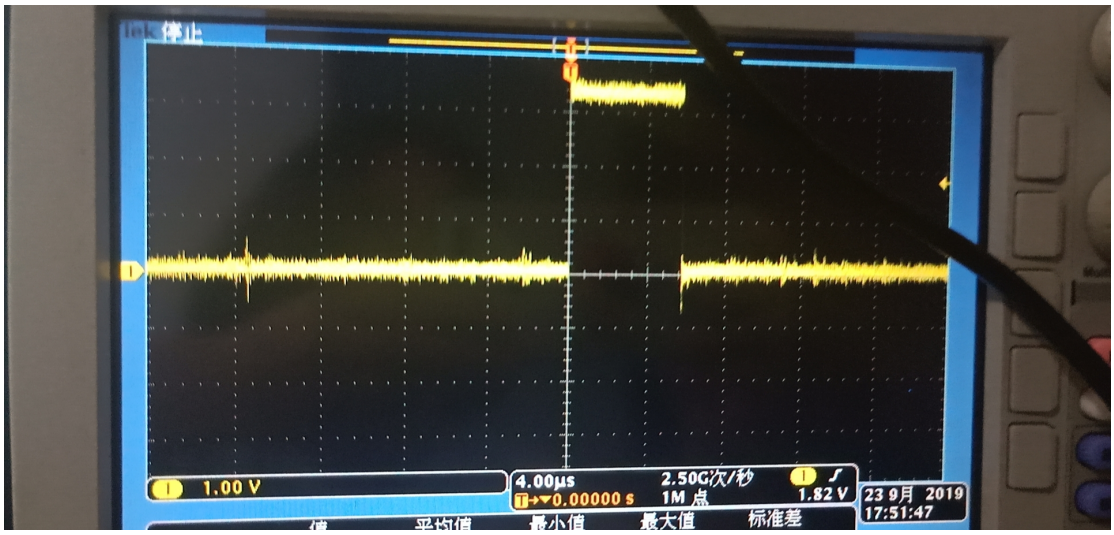
DP83822 is used as slave mode，a 50-MHz CMOS-level oscillator connected to the XI pin and shares the same clock with the MAC（RMII1__REF__CLK PIN）. USE THE SAME MAC INTERFACE WITH DP83848，The signal lines between all PHYs (DP83822 and DP83848) and the MAC are the same.

Why is the hardware configuration PHY address is 00011, the actual software reads out 00111, why is it inconsistent?

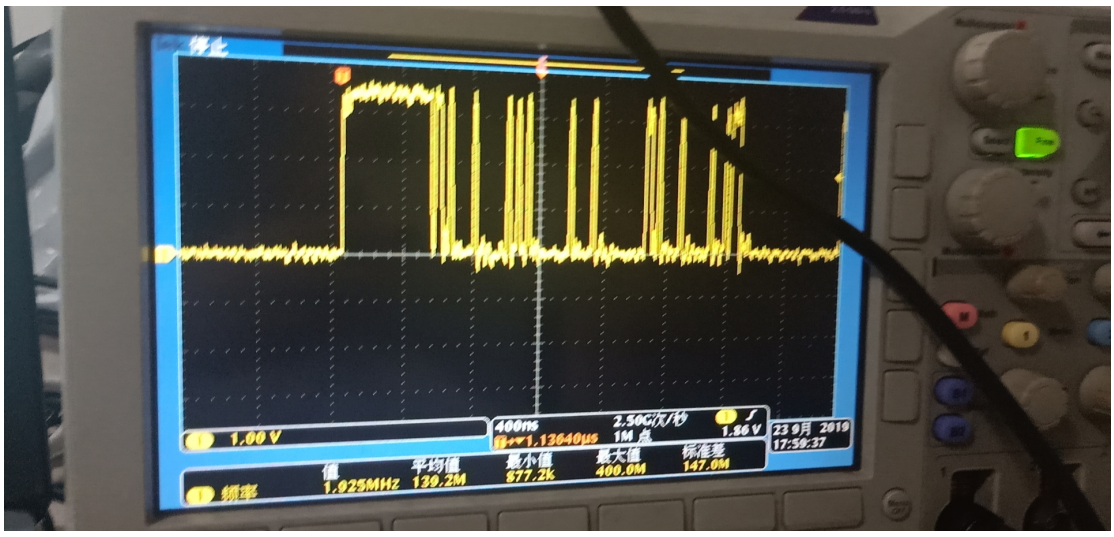
DP83822 RXER



DP83822 RXDV



DP83822 RXD1



DP83822 RXD0