KEYSIGHT TECHNOLOGIES

Test Report

Fail

Test Configuration Details	
Application	
Name	D9020DPHC MIPI D-PHY Test
Version	3.73.1.0
Device Description	
Fixture Setup	Auto Load Switching
High Speed Data Rate(Mbps)	800
CTS Version	v1.2
ZID	100 ohm
CLoad	50pF
Test Session Details	
Infiniium SW Version	06.55.00401
Infiniium Model Number	MSOS804A
Infiniium Serial Number	MY59290107
Debug Mode Used	No
Compliance Limits	MIPI D-PHY Test Limit v1.2 (official)
Probe (Channel 1)	Model: 1169A Serial: US44005715 Head: N5381A/B Atten: Calibrated (11 NOV 2021 11:01:02), Using Cal Atten (3.2214E+00) Skew: Calibrated (11 NOV 2021 11:01:16), Using Cal Skew
Probe (Channel 2)	Model: 1169A Serial: US44001644 Head: N5381A/B Atten: Calibrated (11 NOV 2021 16:53:50), Using Cal Atten (3.3478E+00) Skew: Calibrated (11 NOV 2021 16:54:07), Using Cal Skew
Probe (Channel 3)	Model: 1169A Serial: US44006114 Head: N5381A/B Atten: Calibrated (11 NOV 2021 16:55:49), Using Cal Atten (3.2542E+00) Skew: Calibrated (11 NOV 2021 17:04:29), Using Cal Skew
Probe (Channel 4)	Model: 1169A Serial: US44006104 Head: N5381A/B Atten: Calibrated (9 NOV 2021 17:18:31), Using Cal Atten (3.1661E+00) Skew: Calibrated (9 NOV 2021 17:19:22), Using Cal Skew
Last Test Date	2021-12-16 23:24:21 UTC +08:00

Summary of Results

Test Statistics	
Failed	7
Passed	25
Total	32

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name (click to jump)	Actual Value	Margin	Pass Limits
✓	0	1	1.3.7 HS Data TX Static Common Mode Voltage(Vcmtx)	203.86 mV	46.1	150.00 mV <= VALUE <= 250.00 mV
✓	0	1	1.3.8 HS Data TX Vcmtx Mismatc	1.73 mV	34.6	0.00000 V <= VALUE <= 5.00 mV
✓	0	1	1.3.10 HS Data TX Common-Level Variations Above 450MHz (VCMTX(HF))	3.92 mV	73.9	VALUE < 15.00 mV

✓	0	1	1.3.9 HS Data TX Common-Level Variati Between 50-450MHz (VCMTX(	14.45 mV	42.2	VALUE < 25.00 mV
✓	0	1	1.3.4 HS Data TX Differential Voltage(VOD0 Pulse)	-169.75 mV	22.9	-270.00 mV <= VALUE <= -140.00 mV
✓	0	1	1.3.4 HS Data TX Differe Voltage Pulse)	167.90 mV	21.5	140.00 mV <= VALUE <= 270.00 mV
✓	0	1	1.3.5 HS Data TX Differential Voltage Mismatch (Pulse)	1.85 mV	86.8	VALUE <= 14.00 mV
✓	0	1	1.3.6 HS Data TX Single Ended Output High Voltage Pulse)	290.19 mV	19.4	VALUE <= 360.00 mV
✓	0	1	1.4.17 HS Clock Instantaneous (UIinst)(Max)	1.603 ns	87.2	VALUE < 12.500 ns
✓	0	1	1.3.3 HS Entry: DATA TX THS-PREPARE ZERO	561.08 ns	248.5	VALUE >= TXTHSPrepareTHSZero_LimitMin s
✓	0	1	1.3.11 HS Data TX 20%-80% Rise Time (tR)[Burst Data]	289 ps	39.8	VALUE < DataRiseTime_LimitMax s
✓	0	1	1.3.12 HS Data TX 80%-20% Fall Time (tF)[Bu Data]	284 ps	40.8	VALUE < DataFallTime_LimitMax s
✓	0	1	1.4.7 HS Clock TX Static Common Mode Voltage(Vcmtx)	193.36 mV	43.4	150.00 mV <= VALUE <= 250.00 mV

✅	0	1	1.4.8 HS Clock TX Vcmtx Mismatc	3.97 mV	20.6	0.00000 V <= VALUE <= 5.00 mV
✅	0	1	1.4.10 HS Clock TX Common-Level Variations Above 450MHz (VCMTX(HF))	13.45 mV	10.3	VALUE < 15.00 mV
❌	1	1	1.4.9 HS Clock TX Common-Level Variati Between 50-450MHz (VCMTX(	113.89 mV	-355.6	VALUE < 25.00 mV
❌	1	1	1.4.4 HS Clock TX Differential Voltage(VOD0 Pulse)	-7.54 mV	-101.9	-270.00 mV <= VALUE <= -140.00 mV
❌	1	1	1.4.4 HS Clock TX Differe Voltage Pulse)	31.03 mV	-83.8	140.00 mV <= VALUE <= 270.00 mV
❌	1	1	1.4.5 HS Clock TX Differential Voltage Mismatch (Pulse)	23.49 mV	-67.8	VALUE <= 14.00 mV
✅	0	1	1.4.6 HS Clock TX Single Ended Output High Voltage Pulse)	276.21 mV	23.3	VALUE <= 360.00 mV
❌	1	1	1.4.11 HS Clock TX 20%-80% Rise Time (tR)[Continuous Clock, Burst Data]	99.900000000000 E36s	-208E+47	VALUE < CLKRiseTime_LimitMax s

✗	1	1	1.4.12 HS Clock TX 80%-20% Fall Time (tF)[Co Clock, Burst Data]	99.900000000000 E36s	-208E+47	VALUE < CLKFallTime_LimitMax s
✓	0	1	1.4.17 HS Clock Instantaneous (UIinst)(Min)	1.597 ns	160E+01	VALUE >= UIinst_Min_Limit s
✓	0	1	1.4.18 Clock Lane HS Clock Delta UI (UI variati	-170 m%	49.2	UIVariant_Limit_Min % <= VALUE <= UIVariant_Limit_Max %
✓	0	1	1.3.1 HS Entry: DATA TLPX	128.23 ns	156.5	VALUE >= 50.00 ns
✓	0	1	1.3.2 HS Entry: DATA TX THS-PREPARE	67.27 ns	43.3	THSPrepare_LimitMin s <= VALUE <= THSPrepare_LimitMax s
✓	0	1	1.3.13 HS Exit: DATA TX THS-TRAIL	94.56 ns	45.5	VALUE >= TXTHSTrail_LimitMin s
✓	0	1	1.3.14 HS Exit: DATA TX TREOT	6.11 ns	82.5	VALUE <= 35.00 ns
✓	0	1	1.3.15 HS Exit: DATA TX TEOT	100.68 ns	18.9	VALUE <= TXTEOT_LimitMax s
✓	0	1	1.3.16 HS Exit: DATA TX THS-EXIT	957.69 ns	857.7	VALUE >= 100.00 ns
✗	1	1	1.5.4 Data-to-Clock Skew (TSKEW(TX))(Max,Min)	-187 mUIinst	-12.3	MinMaxTSkewTest_LimitMin UIinst <= VALUE <= MinMaxTSkewTest_LimitMax UIinst
✓	0	1	1.5.4 Data-to-Clock Skew (TSKEW(	-139 mUIinst	3.7	MeanTSkewTest_LimitMin UIinst <= VALUE <= MeanTSkewTest_LimitMax UIinst

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✓ **1.3.7 HS Data TX Static Common Mode Voltage(Vcmtx)**

D-PHY Specification v1.2 Section 9.1.1 Table 19, CTS v1.2(Test 1.3.7)

HS transmit static common-mode voltage.
Actual Value Measurement Name: 811_Vcmtx(Worst)
Pass Limits: 150.00 mV <= VALUE <= 250.00 mV

Actual Value	Margin	HS Data TX Common Mode Voltage	Vcmtx(Differential-1)	Number of Vcmtx(Differential-1) Measured
203.86 mV	46.1	(See image)	203.86 mV	12.577000 k

Vcmtx(Differential-0)	Number of Vcmtx(Differential-0) Measured	ZID	DataLane	Number of HS Burst
200.40 mV	7.051000 k	100 ohm	Lane0	1

HS Data TX Common Mode Voltage

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1.3.8 HS Data TX Vcmtx Mismatch

D-PHY Specification v1.2 Section 9.1.1 Table 19, CTS v1.2(Test 1.3.8)

VCMTX mismatch when output is Differential-1 or Differential-0.
Actual Value Measurement Name: 812_Vcmtx Mismatch
Pass Limits: 0.00000 V <= VALUE <= 5.00 mV

Actual Value	Margin	Vcmtx(Differential-1)	Vcmtx(Differential-0)	ZID	DataLane	Number of HS Burst
1.73 mV	34.6	203.86 mV	200.40 mV	100 ohm	Lane0	1

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1.3.10 HS Data TX Common-Level Variations Above 450MHz (VCMTX(HF))

D-PHY Specification v1.2 Section 9.1.1 Table 20, CTS v1.2(Test 1.3.10)

Common-level variations above 450MHz.
Actual Value Measurement Name: 818_Vcmtx(HF)
Pass Limits: VALUE < 15.00 mV

Actual Value	Margin	Common Level Variations(>450Mhz)	ZID	DataLane	Number of HS Burst
3.92 mV	73.9	(See image)	100 ohm	Lane0	1

Common Level Variations(>450Mhz)

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1.3.9 HS Data TX Common-Level Variations Between 50-450MHz (VCMTX(LF))

D-PHY Specification v1.2 Section 9.1.1 Table 20, CTS v1.2(Test 1.3.9)

Common-level variation between 50-450MHz.
Actual Value Measurement Name: 819_Vcmtx(LF)
Pass Limits: VALUE < 25.00 mV

Actual Value	Margin	Common Level Variations(50-450MHz)	ZID	DataLane	Number of HS Burst
14.45 mV	42.2	(See image)	100 ohm	Lane0	1

Common Level Variations(50-450MHz)

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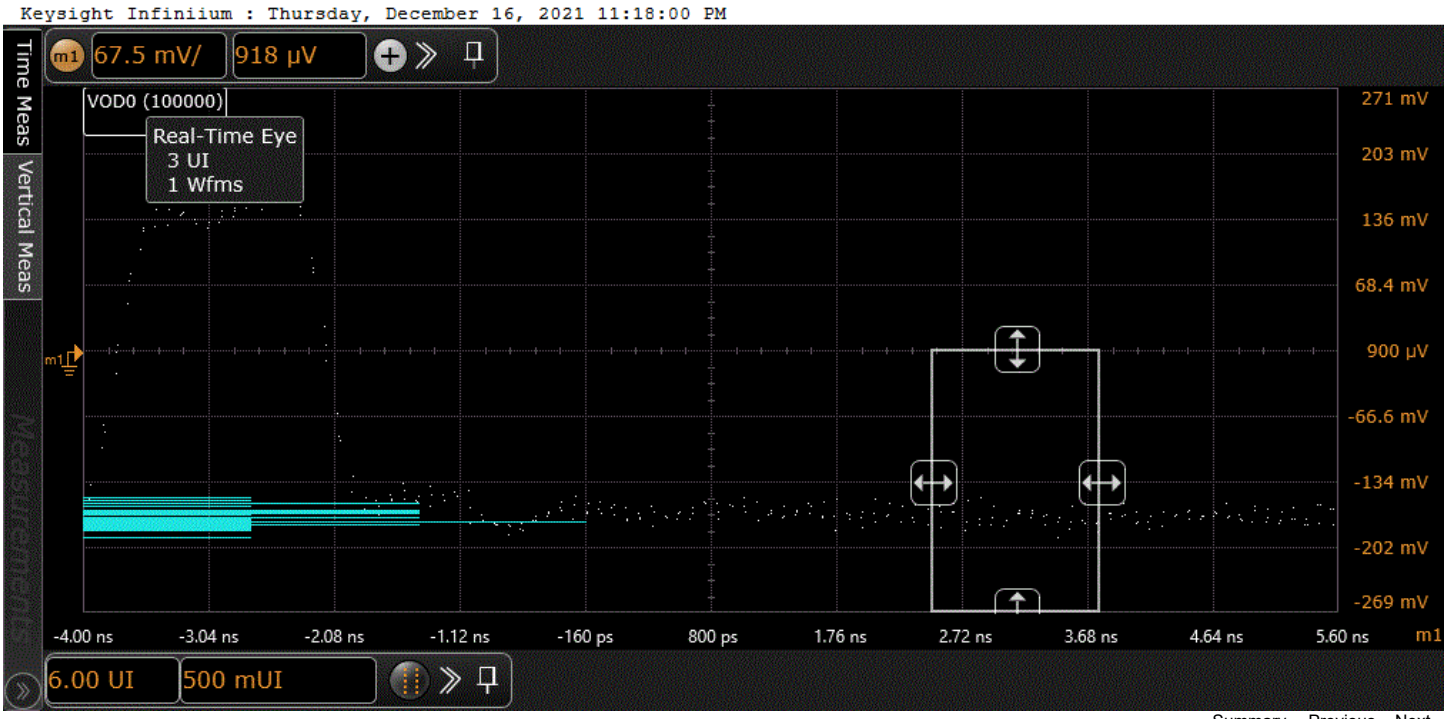
1.3.4 HS Data TX Differential Voltage(VOD0 Pulse)

D-PHY Specification v1.2 Section 9.1.1 Table 19, CTS v1.2(Test 1.3.4)

HS transmit differential voltage.
This test will measure the VOD0 based on the reference data patterns(100000) of differential signal.
Actual Value Measurement Name: 8131_Vod0(Mean)
Pass Limits: -270.00 mV <= VALUE <= -140.00 mV

Actual Value	Margin	VOD0 (100000)	Vod(Differential-0)	Number of measurement	ZID	DataLane	Number of HS Burst
-169.75 mV	22.9	(See image)	-169.75 mV	3.000	100 ohm	Lane0	1

VOD0 (100000)



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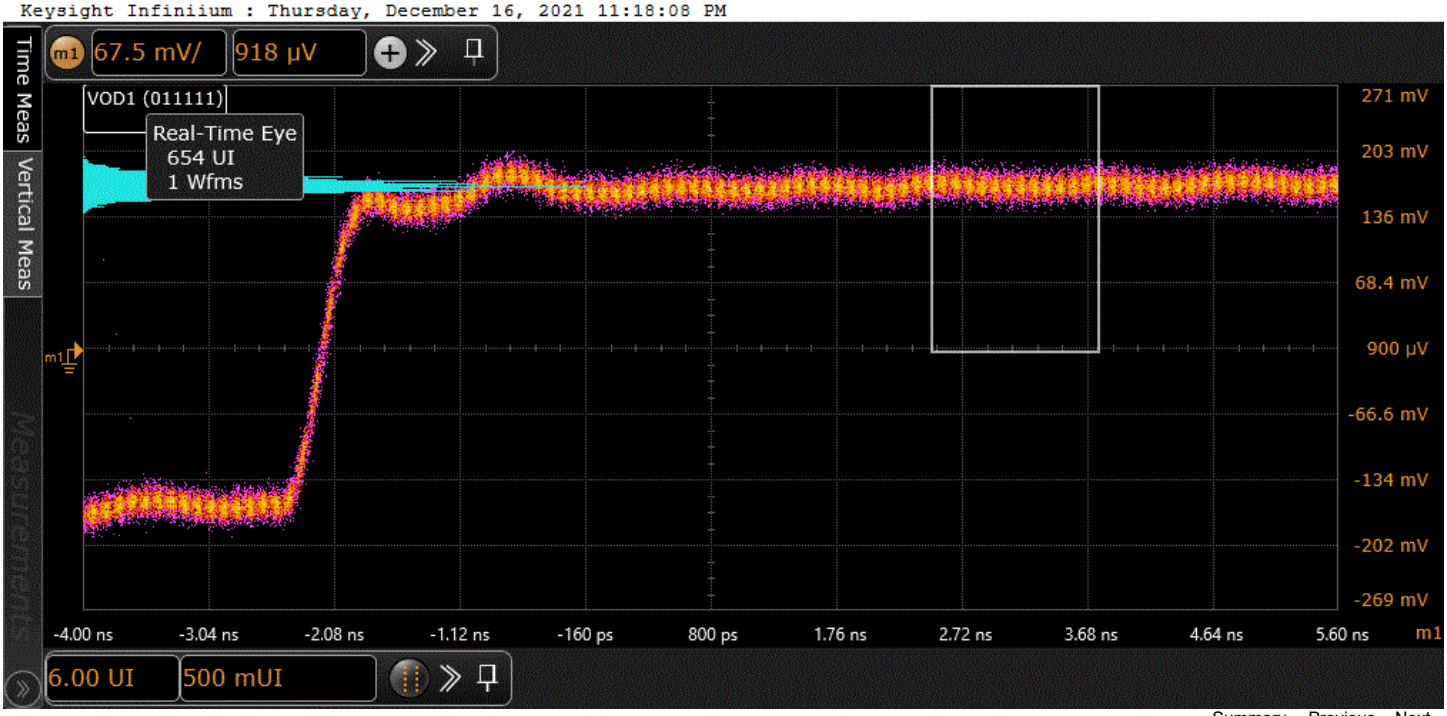
1.3.4 HS Data TX Differential Voltage(VOD1 Pulse)

D-PHY Specification v1.2 Section 9.1.1 Table 19, CTS v1.2(Test 1.3.4)

HS transmit differential voltage.
This test will measure the VOD1 based on the reference data patterns(011111) of differential signal.
Actual Value Measurement Name: 8132_Vod1(Mean)
Pass Limits: 140.00 mV <= VALUE <= 270.00 mV

Actual Value	Margin	VOD1 (011111)	Vod(Differential-1)	Number of measurement	ZID	DataLane	Number of HS Burst
167.90 mV	21.5	(See image)	167.90 mV	654.000	100 ohm	Lane0	1

VOD1 (011111)



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1.3.5 HS Data TX Differential Voltage Mismatch (Pulse)

D-PHY Specification v1.2 Section 9.1.1 Table 19, CTS v1.2(Test 1.3.5)

VOD mismatch when output is Differential-1 or Differential-0.
Actual Value Measurement Name: 8141_Vod Mismatch
Pass Limits: VALUE <= 14.00 mV

Actual Value	Margin	Vod(Differential-1)	Vod(Differential-0)	ZID	DataLane	Number of HS Burst
1.85 mV	86.8	167.90 mV	-169.75 mV	100 ohm	Lane0	1

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1.3.6 HS Data TX Single Ended Output High Voltage(VOHHS Pulse)

D-PHY Specification v1.2 Section 9.1.1 Table 19, CTS v1.2(Test 1.3.6)

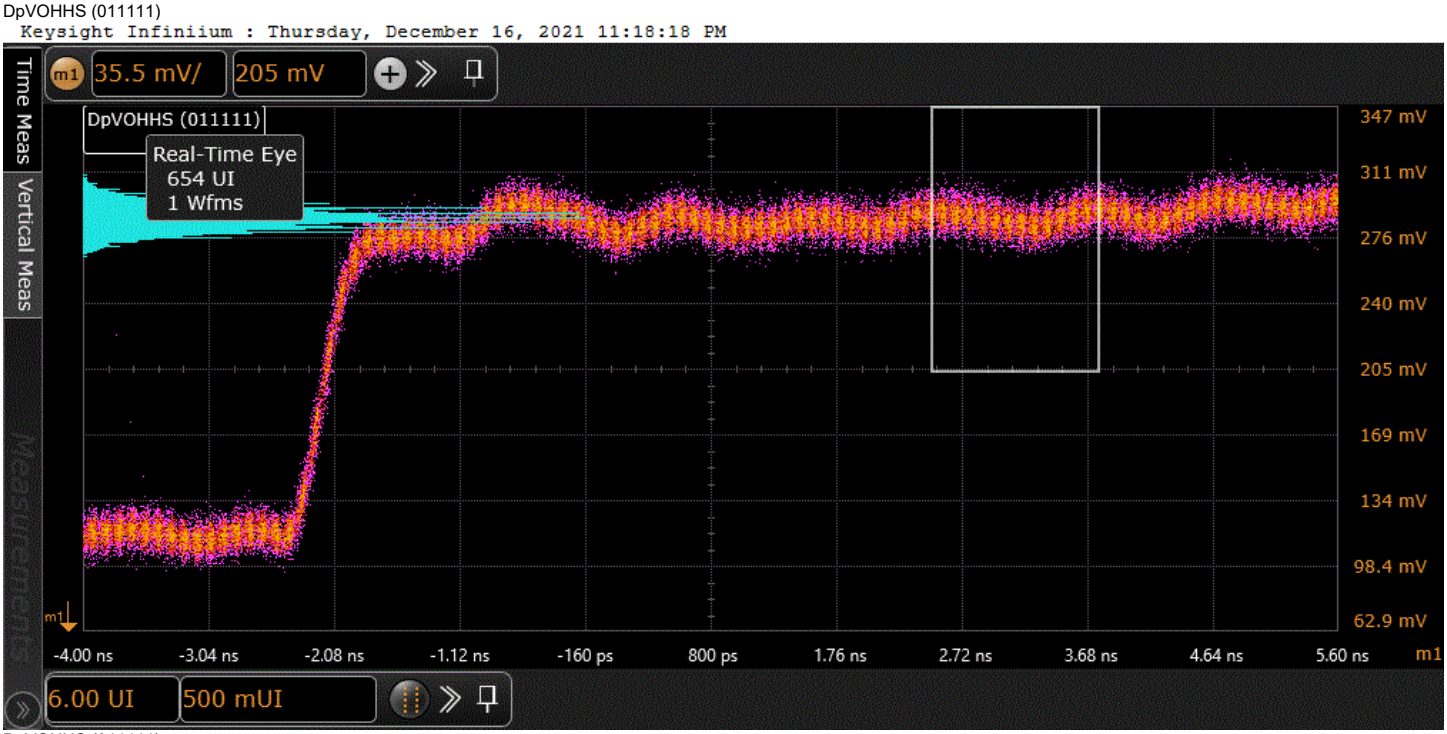
HS Single Ended output high voltage.
This test will measure the VOHHS based on the reference pulses(100000) of single-ended Dp and Dn signals.
Actual Value Measurement Name: 8151_Vohhs(Worst)
Pass Limits: VALUE <= 360.00 mV

Actual Value	Margin	DpVOHHS (011111)	DnVOHHS (011111)	Vohhs(Dp)	Vohhs(Dn)	Number of measurement Vohhs(Dp)

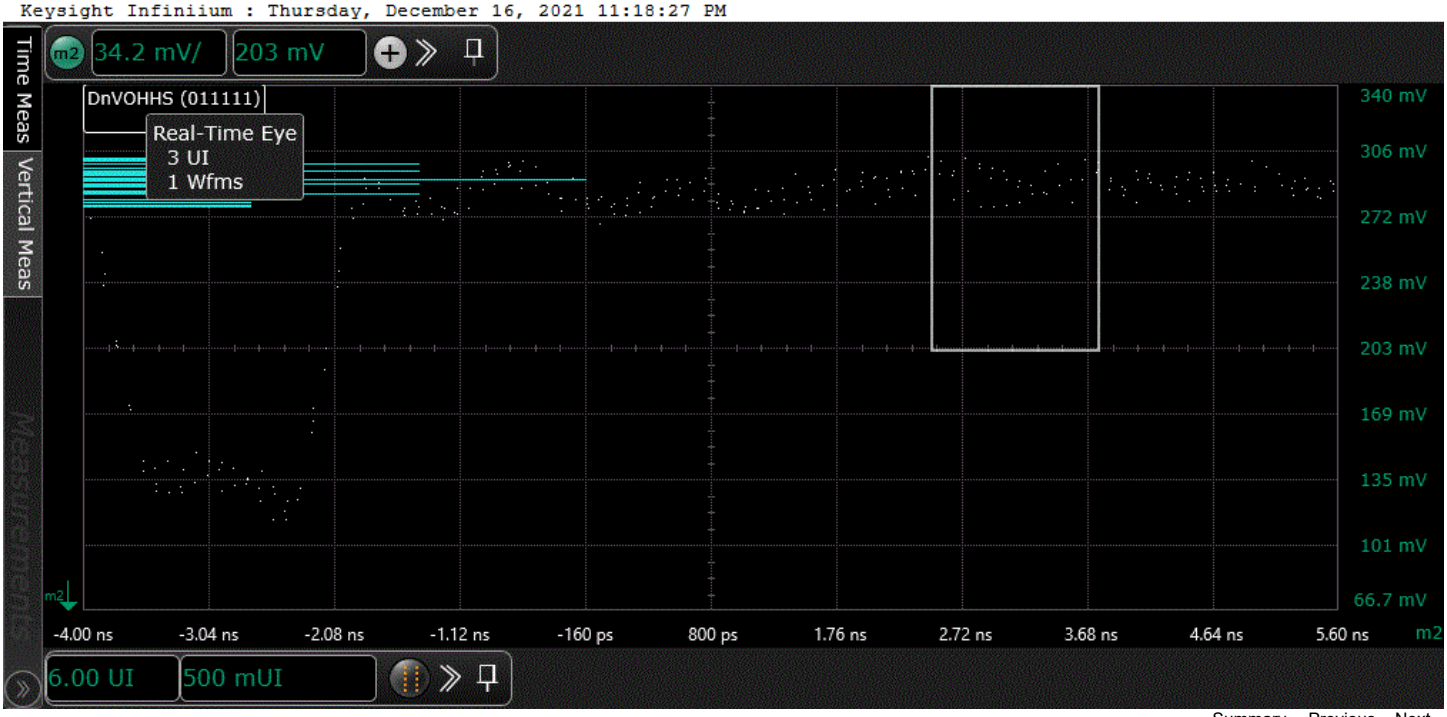
290.19 mV	19.4	(See image)	(See image)	286.46 mV	290.19 mV	654.000

Number of measurement Vohhs(Dn)	ZID	DataLane	Number of HS Burst
3.000	100 ohm	Lane0	1

DpVOHHS (011111)



DnVOHHS (011111)



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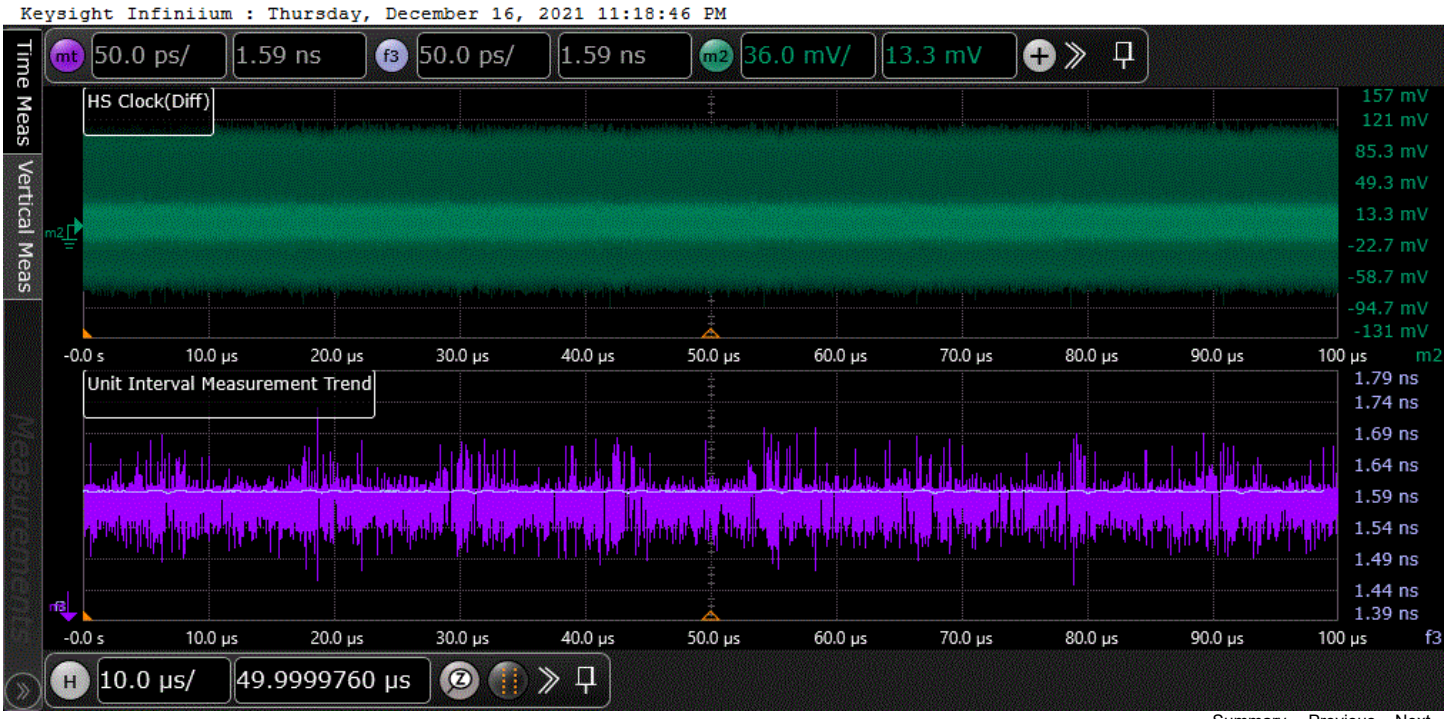
1.4.17 HS Clock Instantaneous (Ulinst)(Max)

D-PHY Specification v1.2 Section 10.1 Table 29, CTS v1.2(Test 1.4.17)

Maximum UI instantaneous of HS Clock.
Actual Value Measurement Name: 911_Ulinst(Max)
Pass Limits: VALUE < 12.500 ns

Actual Value	Margin	UIInst	UIINST(Max)	UIINST(Mean)	Number of UI	ZID	DataLane	Number of HS Burst
1.603 ns	87.2	(See image)	1.603 ns	1.600 ns	62.415000 k	100 ohm	Lane0	1

UIInst



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1.3.3 HS Entry: DATA TX THS-PREPARE+THS-ZERO

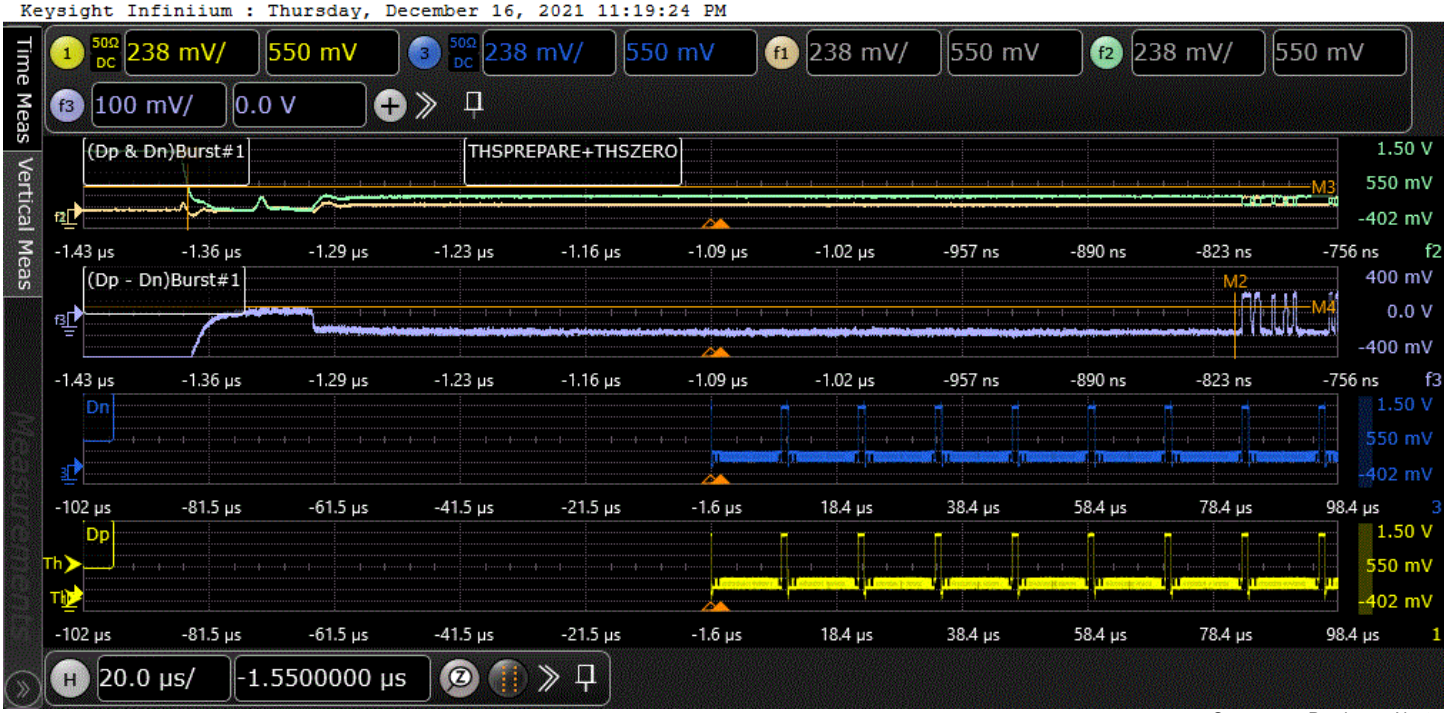
D-PHY Specification v1.2 Section 6.9 Table 14, CTS v1.2(Test 1.3.3)

THS-PREPARE+Time to drive HS-0 before Sync sequence.
TXTHSPrepareTHSZero_LimitMin is based on 145ns+10*UI.
Actual Value Measurement Name: 558_THS-PREPARE+THS-ZERO
Pass Limits: VALUE >= TXTHSPrepareTHSZero_LimitMin s

Actual Value	Margin	THSPREPARE_THSZERO	UIINST(Mean)	VHS_ZERO	ZID	DataLane
561.08 ns	248.5	(See image)	1.600 ns	-172.35 mV	100 ohm	Lane0

PassLimit Min (TXTHSPrepareTHSZero_LimitMin)	Number of HS burst
161.00 ns	1

THSPREPARE_THSZERO



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1.3.11 HS Data TX 20%-80% Rise Time (tR)[Burst Data]

D-PHY Specification v1.2 Section 9.1.1 Table 20, CTS v1.2(Test 1.3.11)

This test is to verify that the 20%-80% rise time of the HS Differential signal is less than the maximum conformance limit(DataRiseTime_LimitMax).
For CTS v1.2, the maximum conformance limit(DataRiseTime_LimitMax) is 0.3*UI for Datarate = 1Gbps, 0.35*UI for Datarate > 1Gbps and = 1.5Gbps , 0.4*UI for Datarate > 1.5Gbps.
This test will measure the rise time based on the reference data patterns(000111) of differential signal.
This test is applicable for Burst Data signal only.
The VHS_ZERO level measured from Data Lane will be used to calculate 20/80% reference voltage for rise time measurement in this test.
Actual Value Measurement Name: 81101_Rise Time
Pass Limits: VALUE < DataRiseTime_LimitMax s

Actual Value	Margin	HS TX Risetime	Transition Time Measurement Lower Threshold(%)	Vod(1)	Vod(0)	UIINST(Mean)
289 ps	39.8	(See image)	20	172.35 mV	-172.35 mV	1.600 ns

Number of Measurement	ZID	DataLane	PassLimit Max (DataRiseTime_LimitMax)	Number of HS Burst
689	100 ohm	Lane0	480 ps	1

HS TX Risetime

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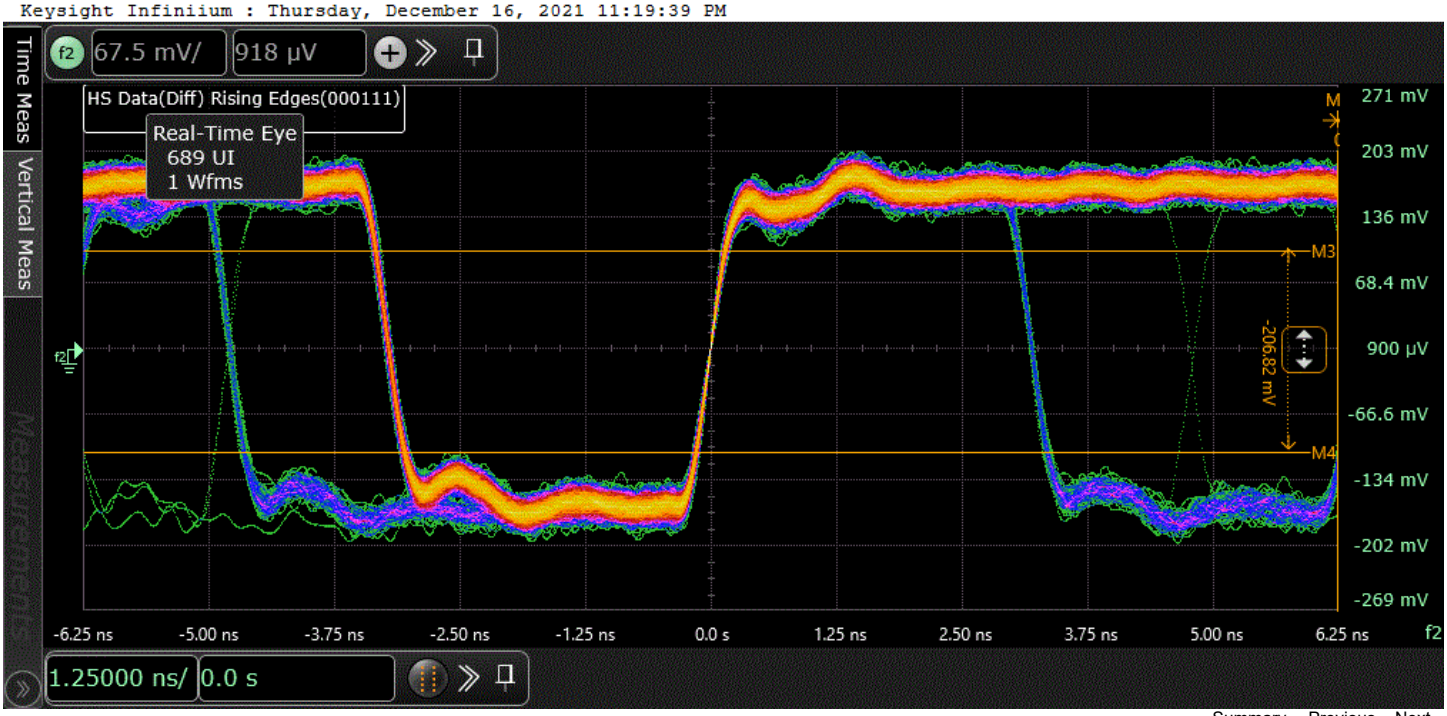

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1.3.12 HS Data TX 80%-20% Fall Time (tF)[Burst Data]

D-PHY Specification v1.2 Section 9.1.1 Table 20, CTS v1.2(Test 1.3.12)

This test is to verify that the 80%-20% fall time of the HS differential signal is less than the maximum conformance limit(DataFallTime_LimitMax).
For CTS v1.2, the maximum conformance limit(DataFallTime_LimitMax) is 0.3*UI for Datarate = 1Gbps, 0.35*UI for Datarate > 1Gbps and = 1.5Gbps , 0.4*UI for Datarate > 1.5Gbps.
This test will measure the fall time based on the reference data patterns(111000) of differential signal.
This test is applicable for Burst Data signal only.
The VHS_ZERO level measured from Data Lane will be used to calculate 20/80% reference voltage for fall time measurement in this test.
Actual Value Measurement Name: 81111_Fall Time
Pass Limits: VALUE < DataFallTime_LimitMax s

Actual Value	Margin	HS TX Falltime	Transition Time Measurement Lower Threshold(%)	Vod(1)	Vod(0)	UIINST(Mean)
284 ps	40.8	(See image)	20	172.35 mV	-172.35 mV	1.600 ns

Number of Measurement	ZID	DataLane	PassLimit Max (DataFallTime_LimitMax)	Number of HS Burst
686	100 ohm	Lane0	480 ps	1

HS TX Falltime

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1.4.7 HS Clock TX Static Common Mode Voltage(Vcmtx)

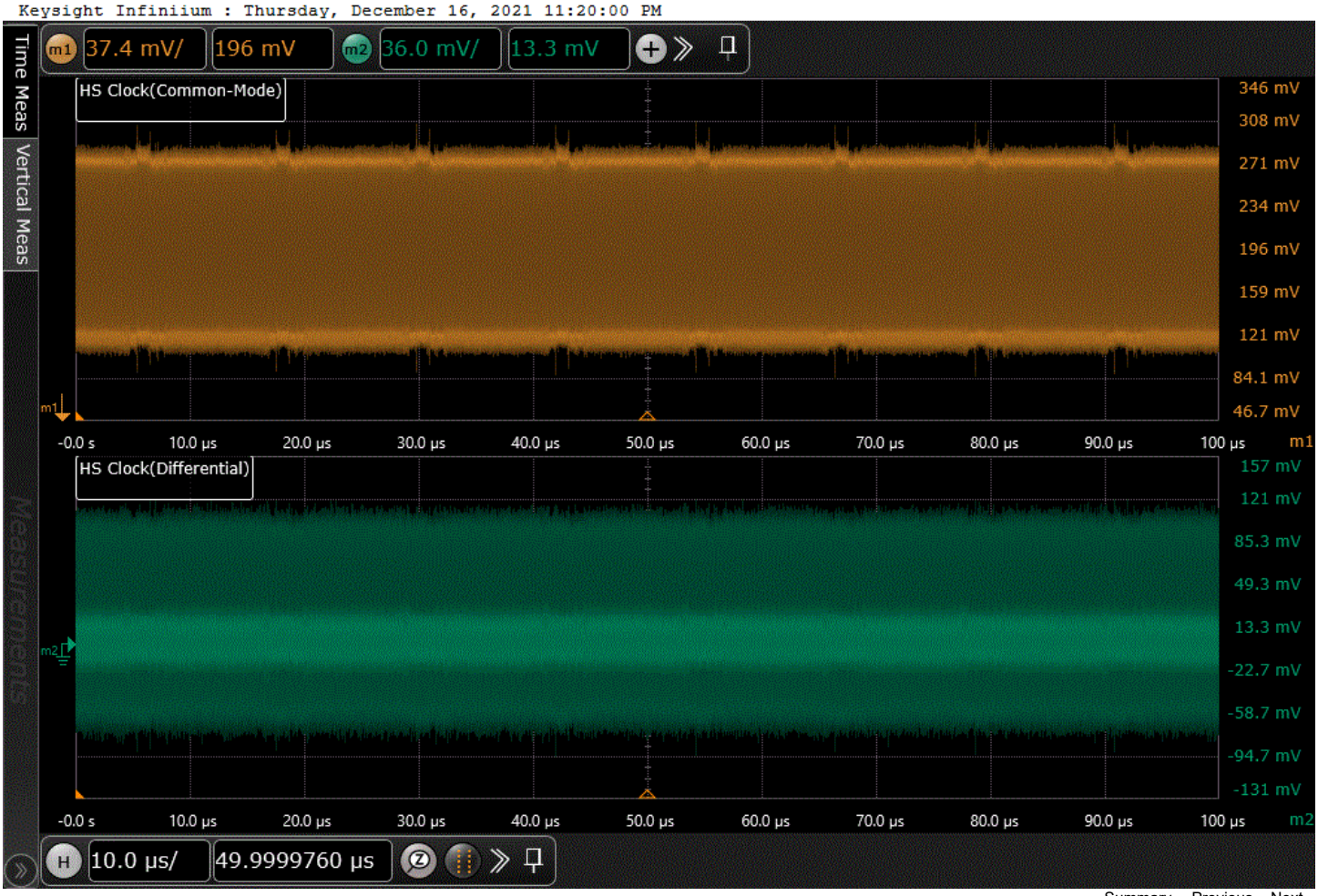
D-PHY Specification v1.2 Section 9.1.1 Table 19, CTS v1.2(Test 1.4.7)

HS transmit static common-mode voltage for Clock.
Actual Value Measurement Name: 1811_Vcmtx(Worst)
Pass Limits: 150.00 mV <= VALUE <= 250.00 mV

Actual Value	Margin	HS Clock TX Common Mode Voltage	Vcmtx(Differential-1)	Number of Vcmtx(Differential-1) Measured
193.36 mV	43.4	(See image)	193.36 mV	96.624000 k

Vcmtx(Differential-0)	Number of Vcmtx(Differential-0) Measured	ZID	Number of HS Burst
201.30 mV	96.045000 k	100 ohm	1

HS Clock TX Common Mode Voltage



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1.4.8 HS Clock TX Vcmtx Mismatch

D-PHY Specification v1.2 Section 9.1.1 Table 19, CTS v1.2(Test 1.4.8)

VCMTX mismatch when output is Differential-1 or Differential-0.
Actual Value Measurement Name: 1812_Vcmtx Mismatch
Pass Limits: 0.00000 V <= VALUE <= 5.00 mV

Actual Value	Margin	Vcmtx(Differential-1)	Vcmtx(Differential-0)	ZID	Number of HS Burst
3.97 mV	20.6	193.36 mV	201.30 mV	100 ohm	1

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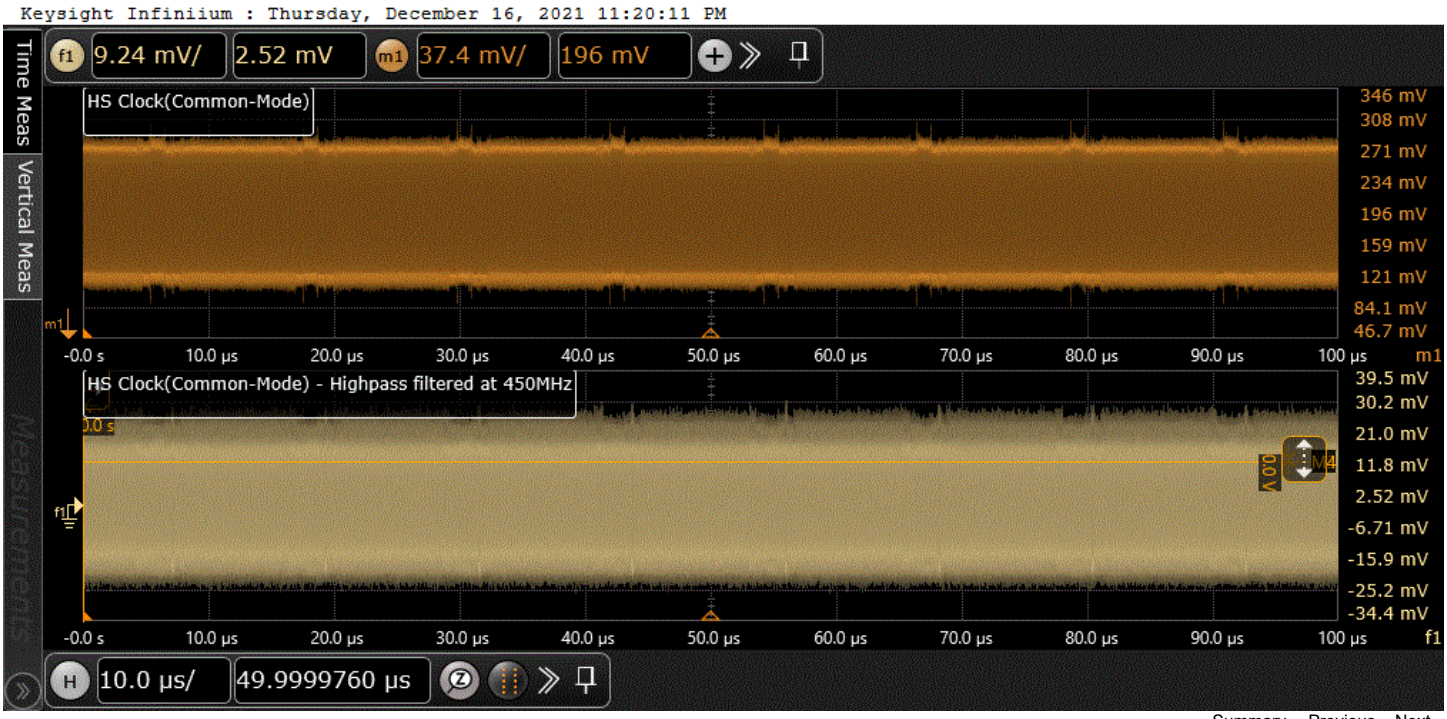
1.4.10 HS Clock TX Common-Level Variations Above 450MHz (VCMTX(HF))

D-PHY Specification v1.2 Section 9.1.1 Table 20, CTS v1.2(Test 1.4.10)

Common-level variations above 450MHz.
Actual Value Measurement Name: 1818_Vcmtx(HF)
Pass Limits: VALUE < 15.00 mV

Actual Value	Margin	Common Level Variations(>450Mhz)	ZID	Number of HS Burst
13.45 mV	10.3	(See image)	100 ohm	1

Common Level Variations(>450Mhz)



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1.4.9 HS Clock TX Common-Level Variations Between 50-450MHz (VCMTX(LF))

D-PHY Specification v1.2 Section 9.1.1 Table 20, CTS v1.2(Test 1.4.9)

Common-level variation between 50-450MHz.
Actual Value Measurement Name: 1819_Vcmtx(LF)
Pass Limits: VALUE < 25.00 mV

Actual Value	Margin	Common Level Variations(50-450MHz)	ZID	Number of HS Burst
113.89 mV	-355.6	(See image)	100 ohm	1

Common Level Variations(50-450MHz)

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1.4.4 HS Clock TX Differential Voltage(VOD0 Pulse)

D-PHY Specification v1.2 Section 9.1.1 Table 19, CTS v1.2(Test 1.4.4)

HS clock transmitter differential voltage.
Actual Value Measurement Name: 18131_Vod0(Mean)
Pass Limits: -270.00 mV <= VALUE <= -140.00 mV

Actual Value	Margin	Clock VOD0 (10)	Vod(Differential-0)	Number of measurement	ZID	Number of HS Burst
-7.54 mV	-101.9	(See image)	-7.54 mV	30.851000 k	100 ohm	1

Clock VOD0 (10)

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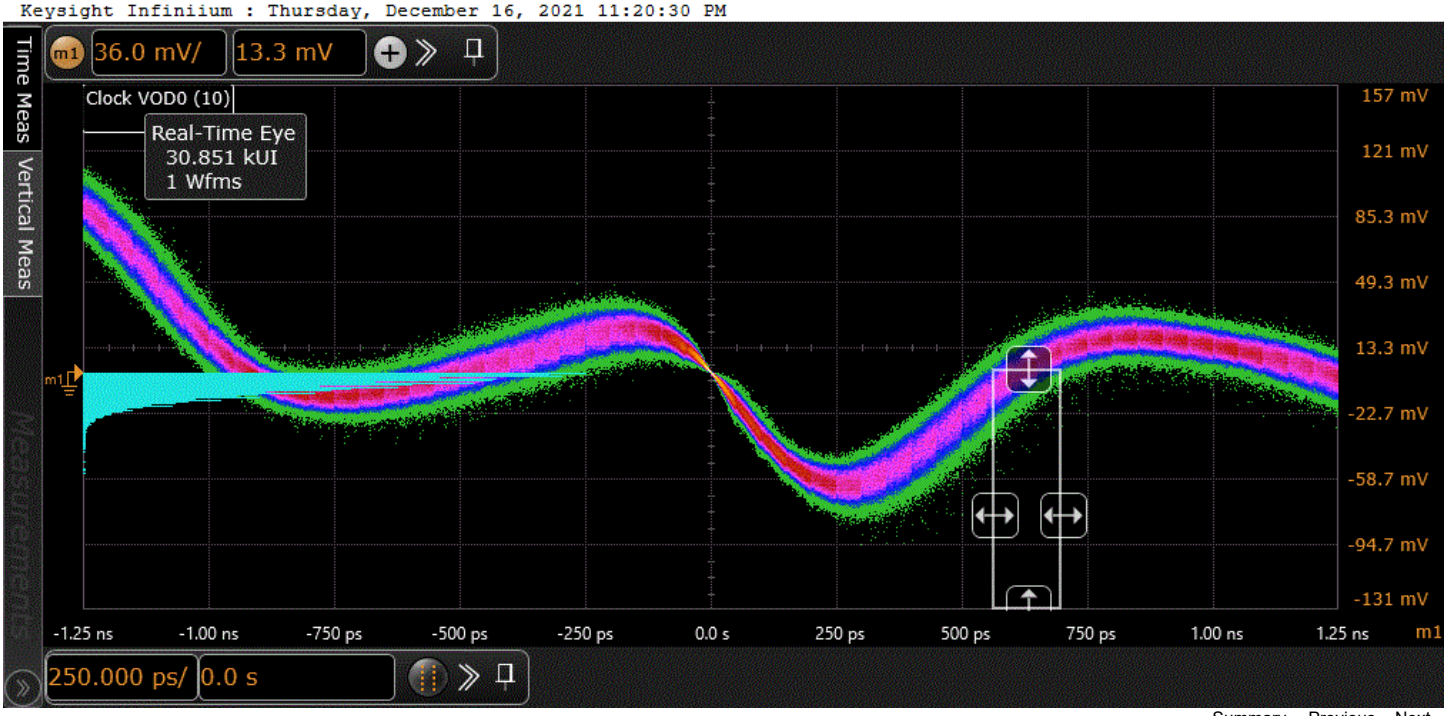

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1.4.4 HS Clock TX Differential Voltage(VOD1 Pulse)

D-PHY Specification v1.2 Section 9.1.1 Table 19, CTS v1.2(Test 1.4.4)

HS clock transmitter differential voltage.
Actual Value Measurement Name: 18132_Vod1(Mean)
Pass Limits: 140.00 mV <= VALUE <= 270.00 mV

Actual Value	Margin	Clock VOD1 (01)	Vod(Differential-1)	Number of measurement	ZID	Number of HS Burst
31.03 mV	-83.8	(See image)	31.03 mV	30.851000 k	100 ohm	1

Clock VOD1 (01)

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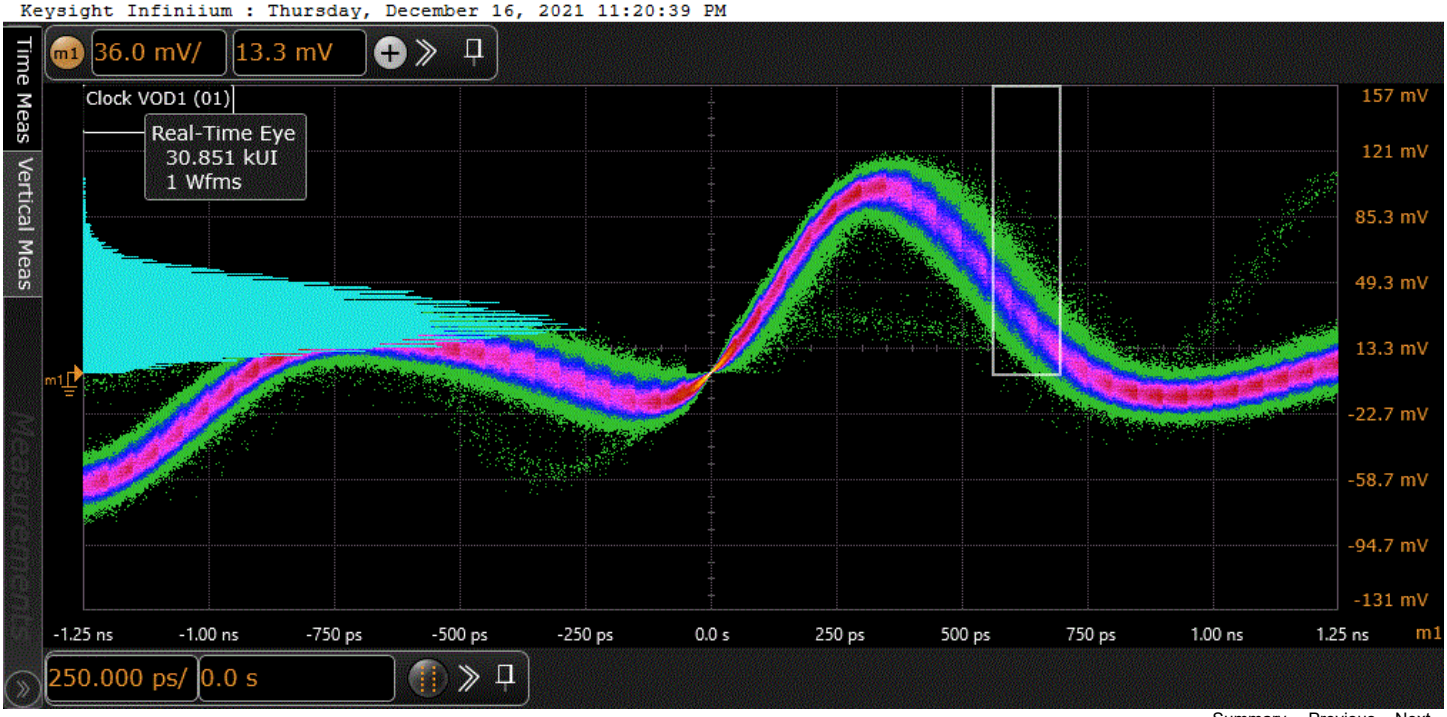

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1.4.5 HS Clock TX Differential Voltage Mismatch (Pulse)

D-PHY Specification v1.2 Section 9.1.1 Table 19, CTS v1.2(Test 1.4.5)

VOD mismatch when output is Differential-1 or Differential-0.
Actual Value Measurement Name: 18141_Vod Mismatch
Pass Limits: VALUE <= 14.00 mV

Actual Value	Margin	Vod(Differential-1)	Vod(Differential-0)	ZID	Number of HS Burst
23.49 mV	-67.8	31.03 mV	-7.54 mV	100 ohm	1

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1.4.6 HS Clock TX Single Ended Output High Voltage(VOHHS Pulse)

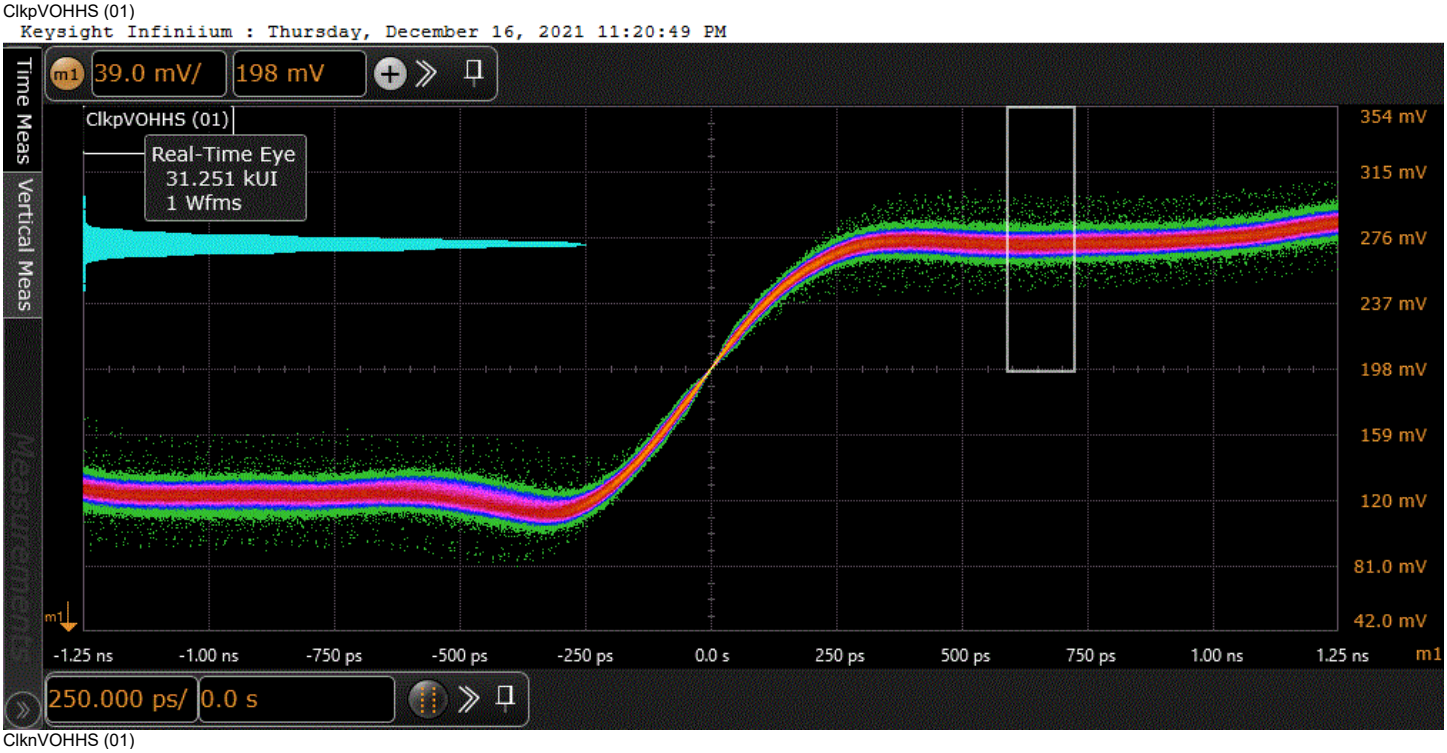
D-PHY Specification v1.2 Section 9.1.1 Table 19, CTS v1.2(Test 1.4.6)

HS Single Ended output high voltage.
Actual Value Measurement Name: 18151_Vohhs(Worst)
Pass Limits: VALUE <= 360.00 mV

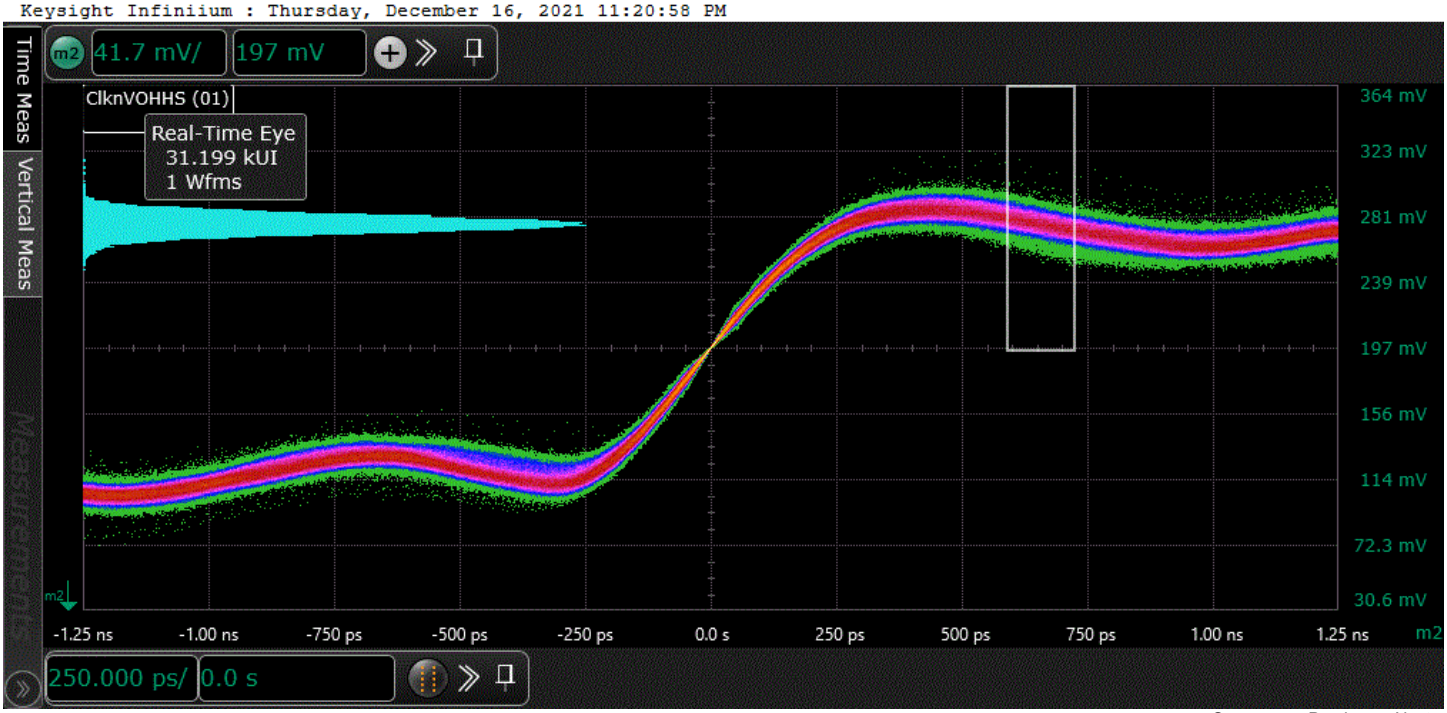
Actual Value	Margin	ClkpVOHHS (01)	ClknVOHHS (01)	Vohhs(Clkp)	Vohhs(Clkn)	Number of measurement Vohhs(Clkp)
276.21 mV	23.3	(See image)	(See image)	272.16 mV	276.21 mV	31.251000 k

Number of measurement Vohhs(Clkn)	ZID	Number of HS Burst
31.199000 k	100 ohm	1

ClkpVOHHS (01)



ClknVOHHS (01)



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1.4.11 HS Clock TX 20%-80% Rise Time (tR)[Continuous Clock, Burst Data]

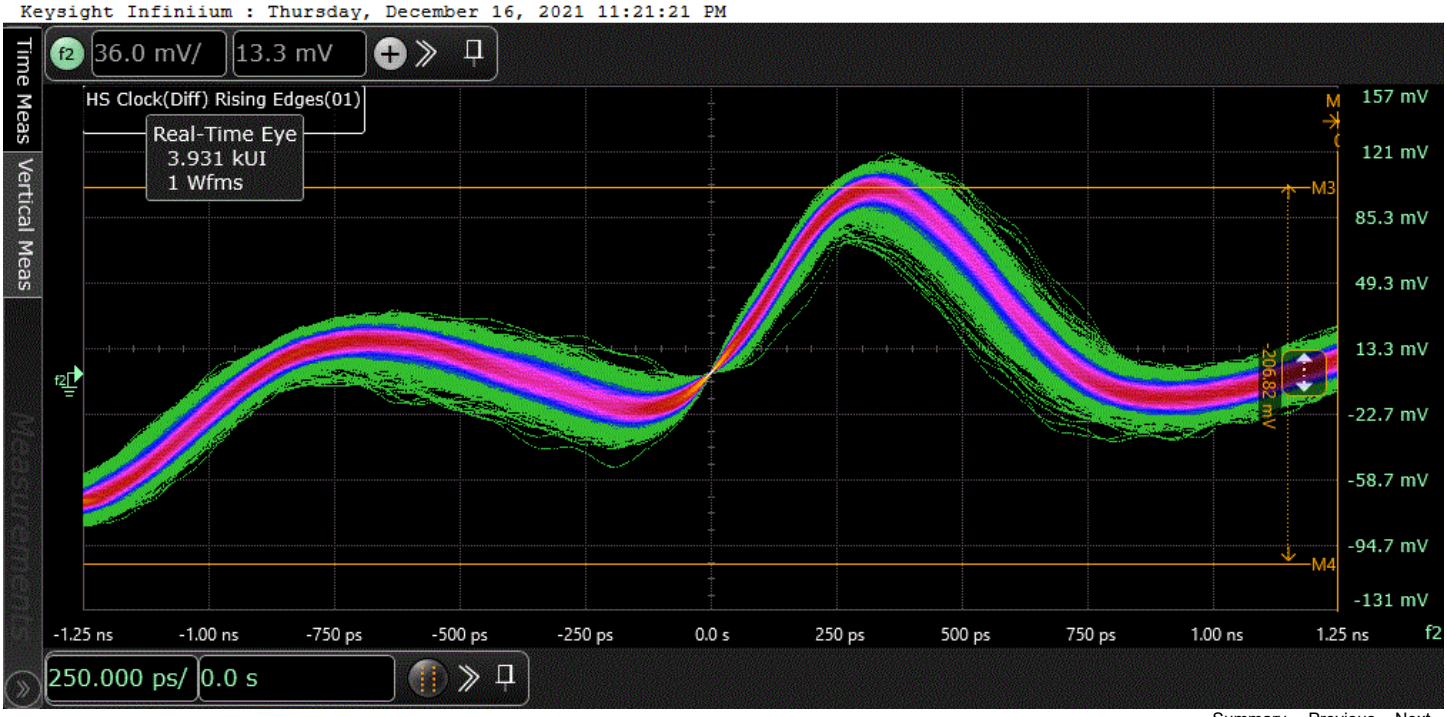
D-PHY Specification v1.2 Section 9.1.1 Table 20, CTS v1.2(Test 1.4.11)

This test is to verify that the 20%-80% rise time of the HS differential signal is less than the maximum conformance limit(CLKRiseTime_LimitMax).
For CTS v1.2, the maximum conformance limit(CLKRiseTime_LimitMax) is 0.3*UI for Datarate = 1Gbps, 0.35*UI for Datarate > 1Gbps and = 1.5Gbps , 0.4*UI for Datarate > 1.5Gbps.
This test is applicable for Continuous Clock and Burst Data signal only.
The VHS_ZERO level measured from Data Lane will be used to calculate 20/80% reference voltage for rise time measurement in this test.
Actual Value Measurement Name: 181102_Rise Time
Pass Limits: VALUE < CLKRiseTime_LimitMax s

Actual Value	Margin	HS Clock TX Risetime	Transition Time Measurement Lower Threshold(%)	Vod(1)	Vod(0)
99.900000000000 E36s	-208E+47	(See image)	20	172.35 mV	-172.35 mV

UIINST(Mean)	Number of Measurement	ZID	PassLimit Max (CLKRiseTime_LimitMax)	Number of HS Burst
1.600 ns	0	100 ohm	480 ps	1

HS Clock TX Risetime



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1.4.12 HS Clock TX 80%-20% Fall Time (tF)[Continuous Clock, Burst Data]

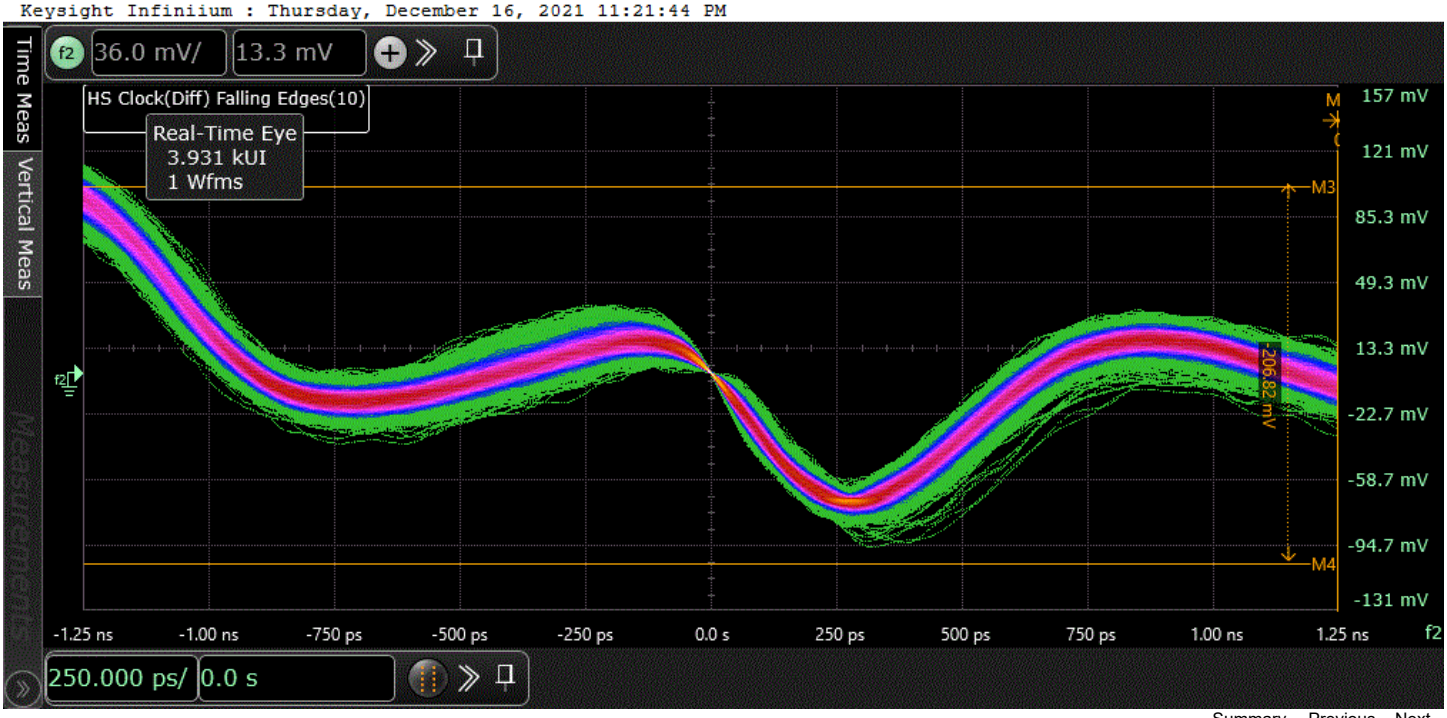
D-PHY Specification v1.2 Section 9.1.1 Table 20, CTS v1.2(Test 1.4.12)

This test is to verify that the 80%-20% fall time of the HS differential signal is less than the maximum conformance limit(CLKFallTime_LimitMax).
For CTS v1.2, the maximum conformance limit(CLKFallTime_LimitMax) is 0.3*UI for Datarate = 1Gbps, 0.35*UI for Datarate > 1Gbps and = 1.5Gbps , 0.4*UI for Datarate > 1.5Gbps.
This test is applicable for Continuous Clock and Burst Data signal only.
The VHS_ZERO level measured from Data Lane will be used to calculate 20/80% reference voltage for fall time measurement in this test.
Actual Value Measurement Name: 181112_Fall Time
Pass Limits: VALUE < CLKFallTime_LimitMax s

Actual Value	Margin	HS Clock TX Falltime	Transition Time Measurement Lower Threshold(%)	Vod(1)	Vod(0)
99.900000000000 E36s	-208E+47	(See image)	20	172.35 mV	-172.35 mV

UIINST(Mean)	Number of Measurement	ZID	PassLimit Max (CLKFallTime_LimitMax)	Number of HS Burst
1.600 ns	0	100 ohm	480 ps	1

HS Clock TX Falltime



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1.4.17 HS Clock Instantaneous (Ulinst)(Min)

D-PHY Specification v1.2 Section 10.1 Table 29, CTS v1.2(Test 1.4.17)

Minimum UI instantaneous (Min) of HS Clock.
Actual Value Measurement Name: 914_Ulinst(Min)
Pass Limits: VALUE >= Ulinst_Min_Limit s

Actual Value	Margin	UIINST(Min)	UIINST(Mean)	Number of UI	ZID	DataLane	PassLimit Min (UIinst_Min_Limit)
1.597 ns	160E+01	1.597 ns	1.600 ns	62.415000 k	100 ohm	Lane0	0.000000000000 s

Number of HS Burst
1

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1.4.18 Clock Lane HS Clock Delta UI (UI variation)

D-PHY Specification v1.2 Section 10.1 Table 29, CTS v1.2(Test 1.4.18)

This test is to verify that the Clock lane HS Clock Delta UI is in between the minimum conformance limit(UIVariant_Limit_Min) and the maximum conformance limit(UIVariant_Limit_Max).
For CTS v1.1, UIVariant_Limit_Min is -10% and UIVariant_Limit_Max is 10% for Datarate = 1Gbps, UIVariant_Limit_Min is -5% and UIVariant_Limit_Max is 5% for Datarate > 1Gbps.
For CTS v1.2, UIVariant_Limit_Min is -10% and UIVariant_Limit_Max is 10% for Datarate = 1Gbps, UIVariant_Limit_Min is -5% and UIVariant_Limit_Max is 5% for Datarate > 1Gbps and = 1.5Gbps .
Actual Value Measurement Name: 1911_UIVariant(Min)
Pass Limits: UIVariant_Limit_Min % <= VALUE <= UIVariant_Limit_Max %

Actual Value	Margin	UIINST(Min)	UIINST(Max)	UIINST(Mean)	Number of UI	DataLane	UIVariant_min	UIVariant_max	ZID
-170 m%	49.2	1.597 ns	1.603 ns	1.600 ns	62.415000 k	Lane0	-170 m%	160 m%	100 ohm

PassLimit Min (UIVariant_Limit_Min)	PassLimit Max (UIVariant_Limit_Max)	Number of HS Burst
-10.00 %	10.00 %	1

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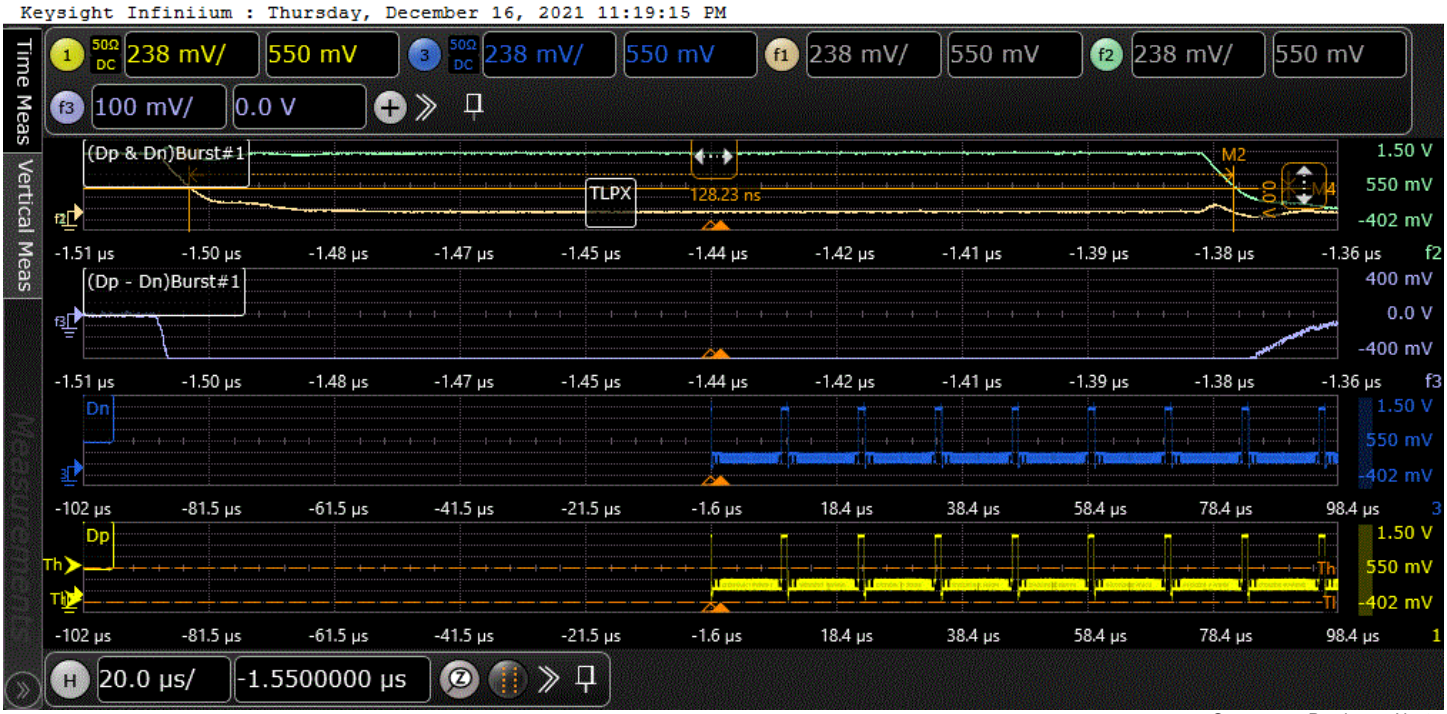
1.3.1 HS Entry: DATA TLPX

D-PHY Specification v1.2 Section 6.9 Table 14, CTS v1.2(Test 1.3.1)

Length of any Low-Power state period.
Actual Value Measurement Name: 511_TLPX
Pass Limits: VALUE >= 50.00 ns

Actual Value	Margin	TLPX	ZID	DataLane	Number of HS burst
128.23 ns	156.5	(See image)	100 ohm	Lane0	1

TLPX



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1.3.2 HS Entry: DATA TX THS-PREPARE

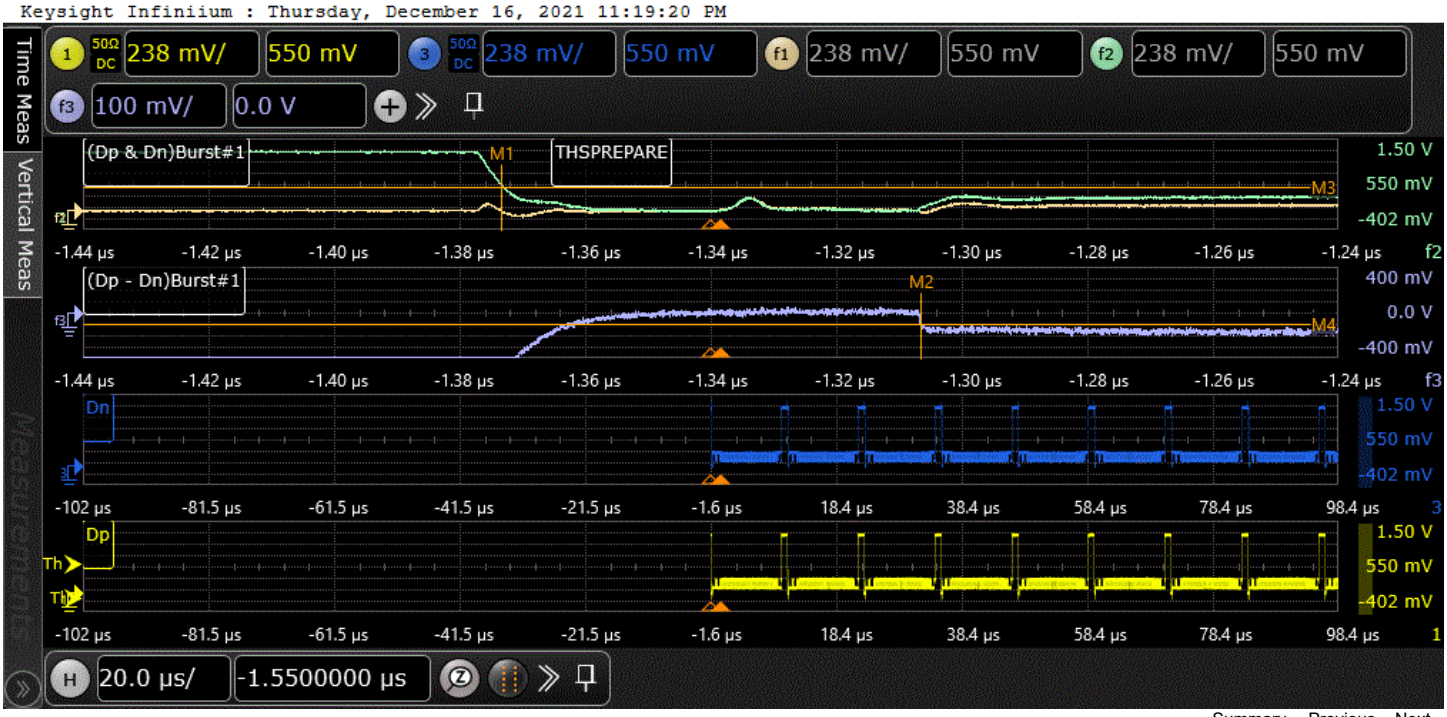
D-PHY Specification v1.2 Section 6.9 Table 14, CTS v1.2(Test 1.3.2)

Time to drive LP-00 to prepare for HS Transmission.
THSPrepare_LimitMin is based on 40ns+4*UI.
THSPrepare_LimitMax is based on 85ns+6*UI.
Actual Value Measurement Name: 557_THS-PREPARE
Pass Limits: THSPrepare_LimitMin s <= VALUE <= THSPrepare_LimitMax s

Actual Value	Margin	THSPREPARE	UIINST(Mean)	ZID	DataLane	PassLimit Min (THSPrepare_LimitMin)
67.27 ns	43.3	(See image)	1.600 ns	100 ohm	Lane0	46.40 ns

PassLimit Max (THSPrepare_LimitMax)	Number of HS burst
94.60 ns	1

THSPREPARE



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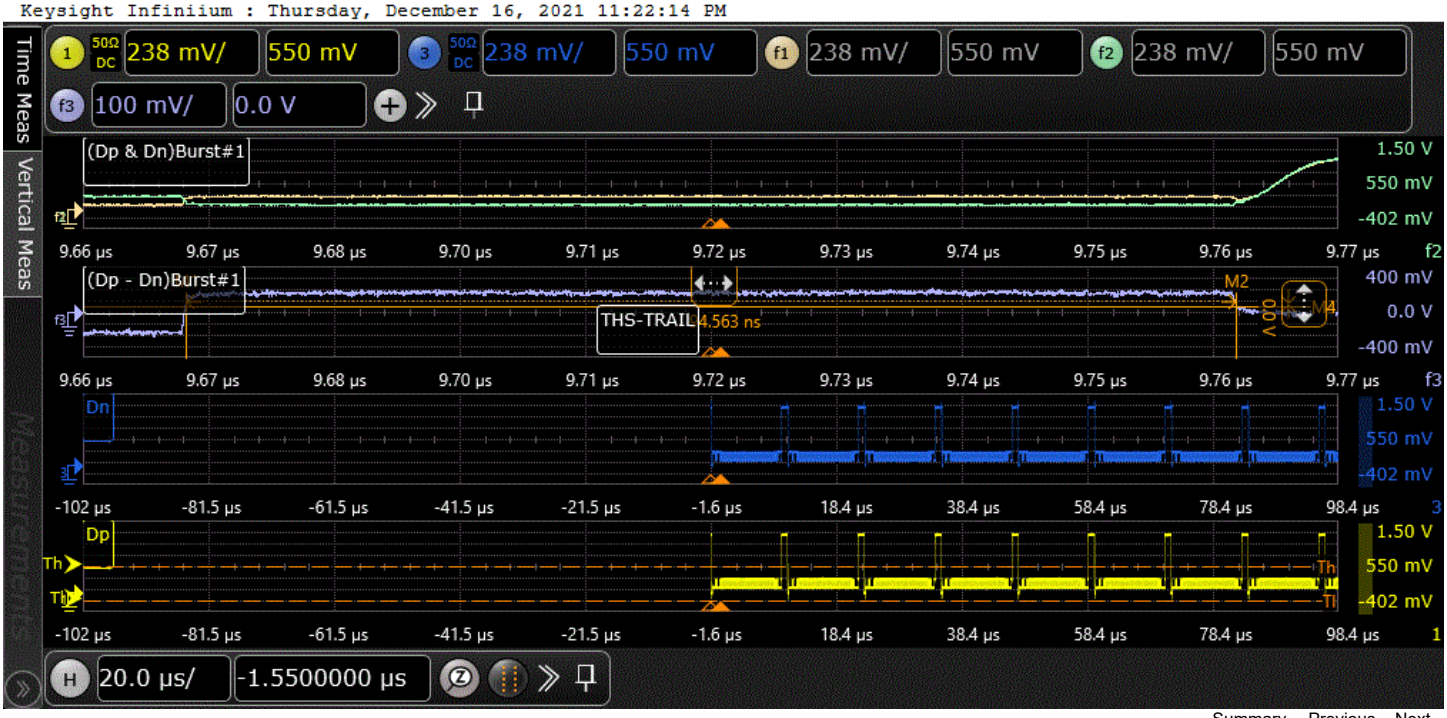
1.3.13 HS Exit: DATA TX THS-TRAIL

D-PHY Specification v1.2 Section 6.9 Table 14, CTS v1.2(Test 1.3.13)

Time to drive flipped differential state after last payload data bit of a HS transmission burst.
TXTHSTrail_LimitMin is based on 60ns+n*4*UI.
The THS-SKIP parameter is useful to avoid glitch problem during THS-TRAIL measurement.
Any transition on the Data Lane in THS-SKIP time interval will be ignored when finding last payload data bit of HS transmission burst.
The default value of THS-SKIP is set to 0s to prevent invalid THS-TRAIL measurement.
Actual Value Measurement Name: 546_THS-TRAIL
Pass Limits: VALUE >= TXTHSTrail_LimitMin s

Actual Value	Margin	THSTRAIL	THS-SKIP(s)	ZID	DataLane	PassLimit Min (TXTHSTrail_LimitMin)	Number of HS burst
94.56 ns	45.5	(See image)	0.0000000000000 s	100 ohm	Lane0	65.00 ns	1

THSTRAIL



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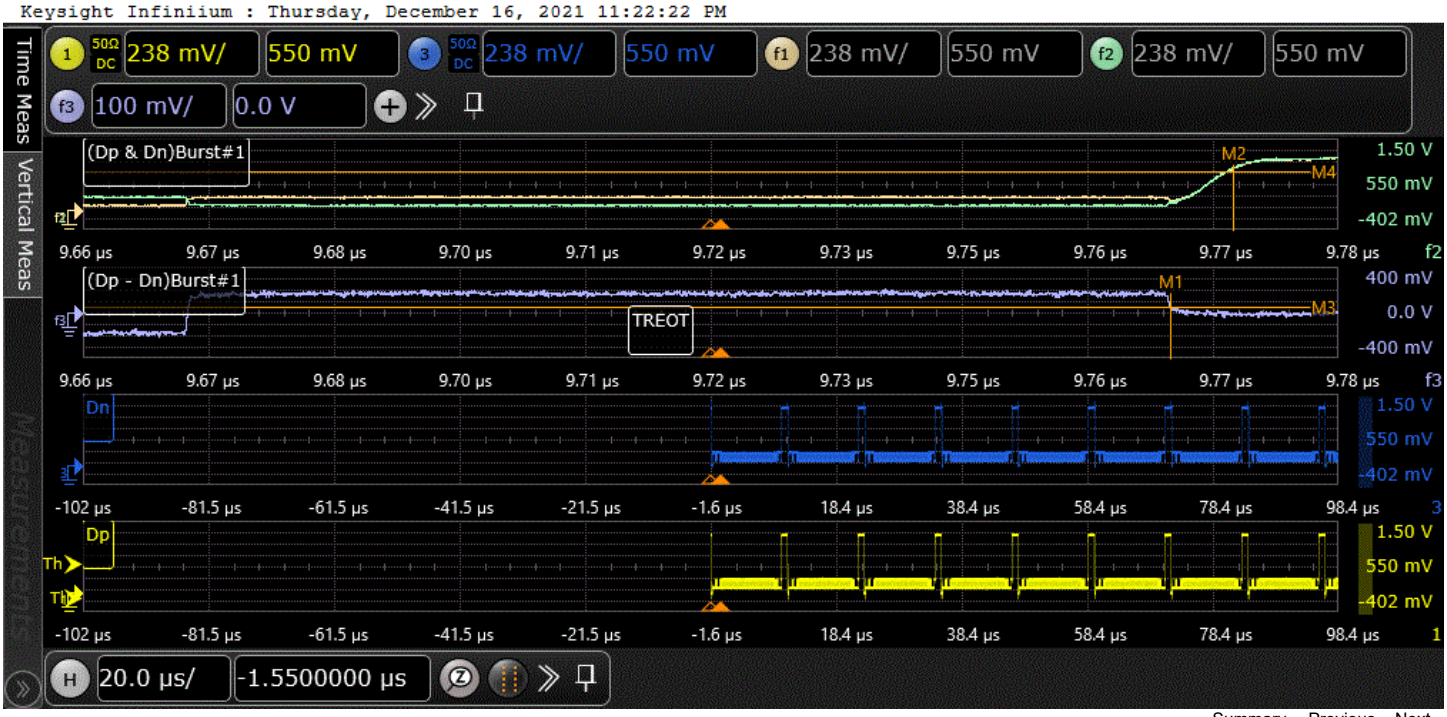
1.3.14 HS Exit: DATA TX TREOT

D-PHY Specification v1.2 Section 9.1.2 Table 22, CTS v1.2(Test 1.3.14)

30%-85% rise time and fall time
Actual Value Measurement Name: 549_TREOT
Pass Limits: VALUE <= 35.00 ns

Actual Value	Margin	TREOT	ZID	DataLane	Number of HS burst
6.11 ns	82.5	(See image)	100 ohm	Lane0	1

TREOT



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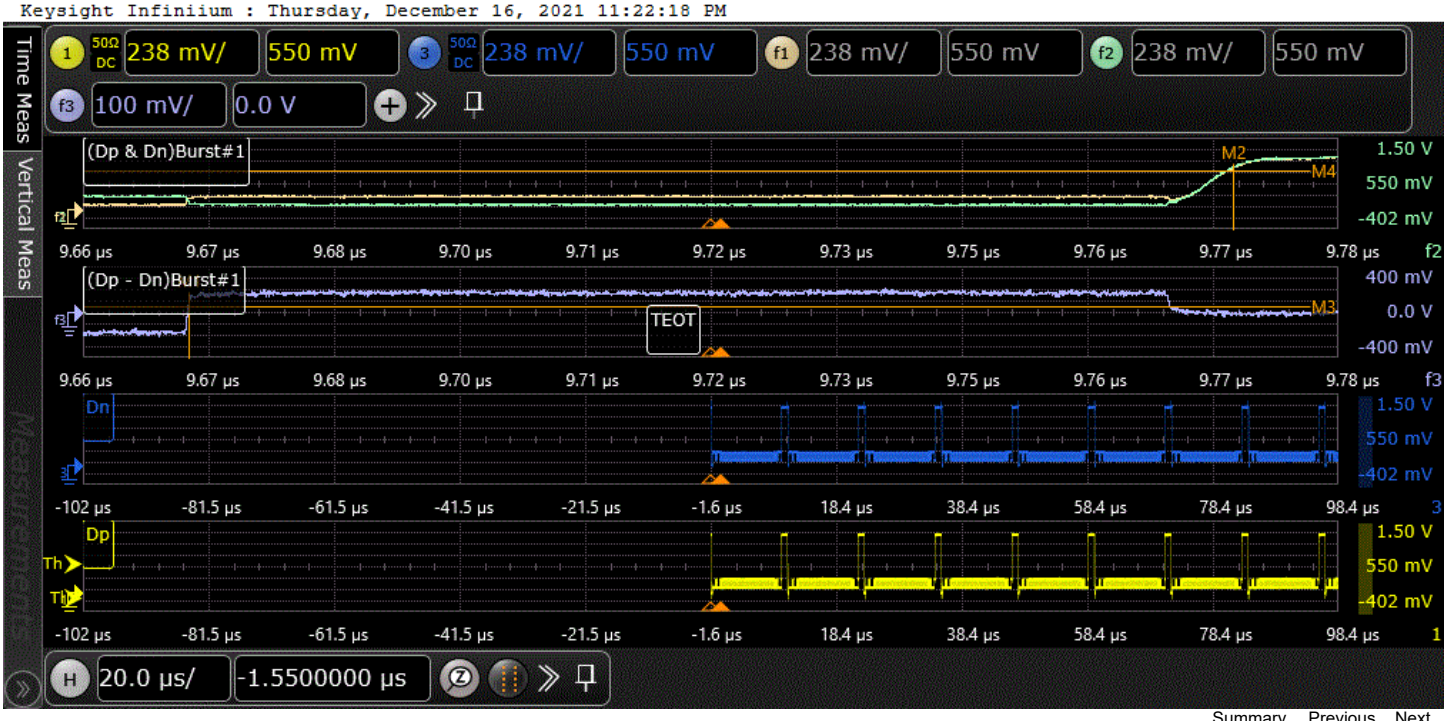
1.3.15 HS Exit: DATA TX TEOT

D-PHY Specification v1.2 Section 6.9 Table 14, CTS v1.2(Test 1.3.15)

Time from start of THS-TRAIL period to start of LP-11 state.
TXTEOT_LimitMax is based on 105ns+n*12*UI.
Actual Value Measurement Name: 547_TEOT
Pass Limits: VALUE <= TXTEOT_LimitMax s

Actual Value	Margin	TEOT	UIINST(Mean)	ZID	DataLane	PassLimit Max (TXTEOT_LimitMax)	Number of HS burst
100.68 ns	18.9	(See image)	1.600 ns	100 ohm	Lane0	124.20 ns	1

TEOT



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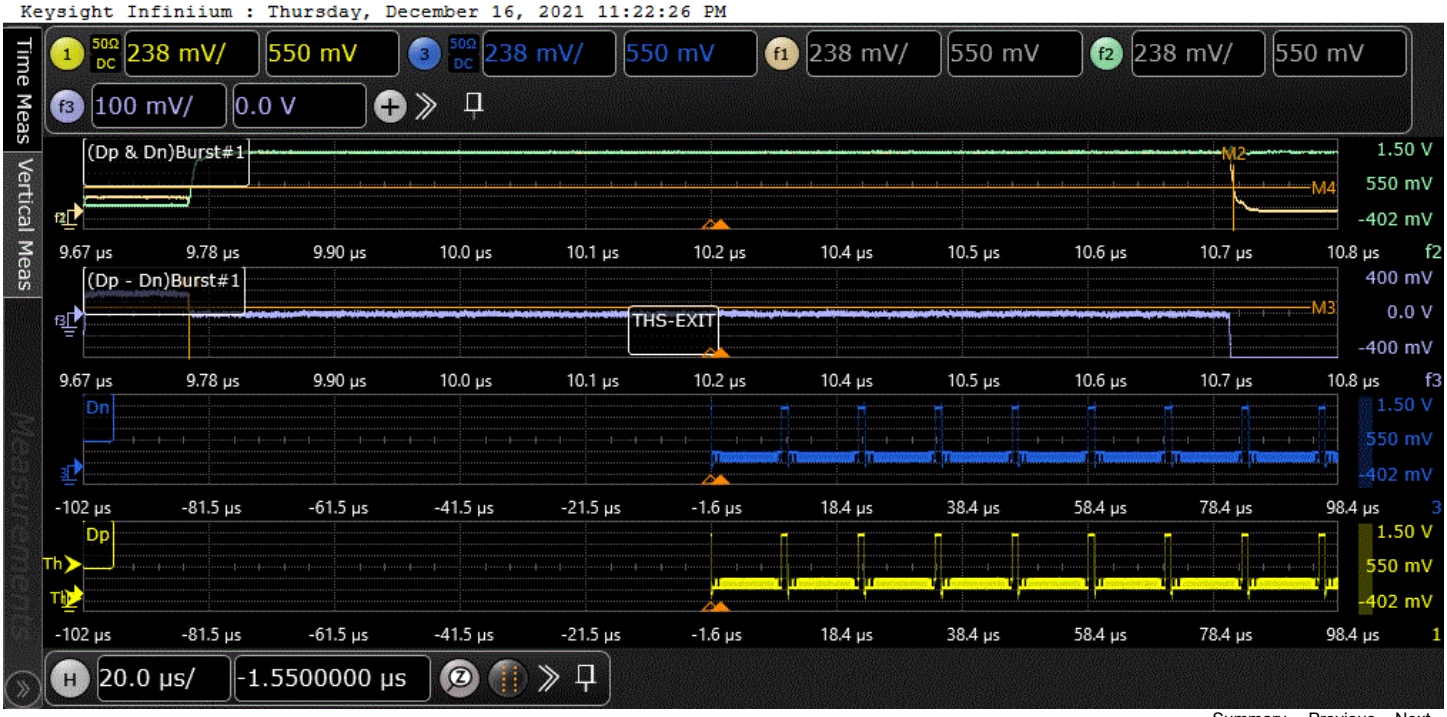
1.3.16 HS Exit: DATA TX THS-EXIT

D-PHY Specification v1.2 Section 6.9 Table 14, CTS v1.2(Test 1.3.16)

Time to drive LP-11 after HS burst.
Actual Value Measurement Name: 548_THS-EXIT
Pass Limits: VALUE >= 100.00 ns

Actual Value	Margin	THSEXIT	Notes:	ZID	DataLane	Number of HS burst
957.69 ns	857.7	(See image)		100 ohm	Lane0	1

THSEXIT



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1.5.4 Data-to-Clock Skew (TSKEW(TX))(Max,Min)

D-PHY Specification v1.2 Section 10.2.1 Table 30, CTS v1.2(Test 1.5.4)

Data to Clock Skew [measured at transmitter].
Actual Value Measurement Name: 913_Tskew(Worst)
Pass Limits: MinMaxTSkewTest_LimitMin UIinst <= VALUE <= MinMaxTSkewTest_LimitMax UIinst

Actual Value	Margin	LeftCrossing	UIINST(Mean)	TSkew(Min)	TSkew(Max)	No Of Measurement	ZID	DataLane
-187 mUIinst	-12.3	(See image)	1.6000 ns	-298.5 ps	-175.7 ps	1.594000 k	100 ohm	Lane0

PassLimit Min (MinMaxTSkewTest_LimitMin)	PassLimit Max (MinMaxTSkewTest_LimitMax)	Number of HS Burst
-150 mUIinst	150 mUIinst	1

LeftCrossing

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1.5.4 Data-to-Clock Skew (TSKEW(TX))(Mean)

D-PHY Specification v1.2 Section 10.2.1 Table 30, CTS v1.2(Test 1.5.4)

Data to Clock Skew [measured at transmitter].
Actual Value Measurement Name: 9131_Tskew(Mean)
Pass Limits: MeanTSkewTest_LimitMin UIinst <= VALUE <= MeanTSkewTest_LimitMax UIinst

Actual Value	Margin	UIINST(Mean)	TSkew(Mean)	No Of Measurement	ZID	DataLane	PassLimit Min (MeanTSkewTest_LimitMin)
-139 mUIinst	3.7	1.6000 ns	-221.8 ps	1.594000 k	100 ohm	Lane0	-150 mUIinst

PassLimit Max (MeanTSkewTest_LimitMax)	Number of HS Burst
150 mUIinst	1