Application Report
SLVA944–November 2017

ESD224 HDMI® 2.0 Compliance and Protection

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ABSTRACT

This application report presents HDMI® 2.0 Compliance and ESD clamping data for the ESD224 4-channel HDMI ESD protection device. The low clamping and high-differential bandwidth provided by the on-chip ESD protection network of the ESD224 makes it possible to be able to cleanly pass HDMI 2.0 signals while providing robust protection to downstream HDMI devices.

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Trademarks

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1 Introduction to ESD224

The ESD224 is a bidirectional TVS ESD protection diode array for high-speed applications such as HDMI 2.0 applications. The ESD224 employs on-chip differentially matched series elements to enhance down-stream ESD clamping performance while maintaining the signal compliance for HDMI. Due to the presence of the on-chip series elements for enhanced ESD clamping, the device is in a non-flow-through DQA package. The ESD224 is suitable to protect both the TMDS data lines (D0±, D1±, D2±) and TMDS clock lines (CLK±). See *ESD224 Low Clamping 4-Channel ESD Protection Device for HDMI Interface* for more information.

This document describes the modeling environment and RF simulations performed during device design and demonstrates the devices RF performance through comparisons of modeled and silicon data. The ESD224 was evaluated for HDMI 2.0 compliance in a reference design using the TI TDP158 HDMI retimer. ESD clamping and protection performance was evaluated by measuring the downstream clamping performance of the ESD224 on an application board employing a common set-top box (STB) system-on-a-chip (SoC).

2 HDMI® Simulations During Design

2.1 Bandwidth

The goal of the ESD224 was to provide a low clamping device while still being able to pass HDMI 2.0 (6 Gbps). In order to prove this during the concept phase, a 3D model with the internal structure was built for the lead frame of the device. Using this model in the Advanced Design System (ADS) from Keysight™, and adding in the lumped elements could give us the S-parameter data needed to show HDMI compliance. The lumped elements of the device are represented by a capacitor, because if the ESD diode is not turned on for an ESD event, the diodes can just be represented by their junction capacitance. Figure 1 shows the S-parameter model generation that was created during the Design Phase of ESD224 development.

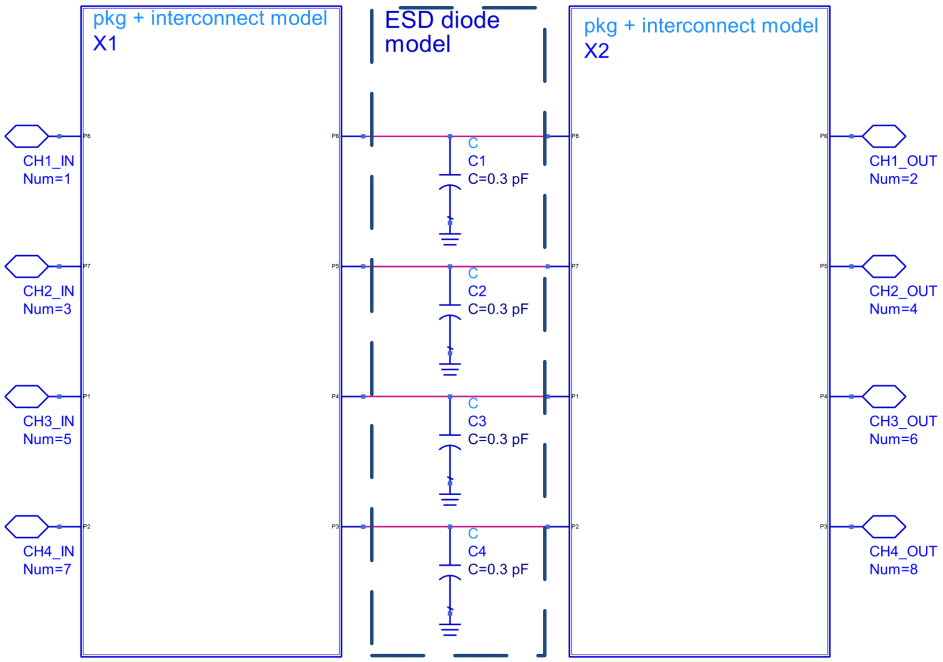

Figure 1. Model Plus Lumped Elements for S-Parameter

Observe the ADS schematic in Figure 1 only has a lumped capacitance added for the ESD clamp and not the detailed on-die design structure. The S-parameter file for the internal structure (X1 and X2 in Figure 1) without the main ESD diode was modeled in a separate environment using a detailed 3D buildup of the silicon die, bond wires, and package. Therefore, the only parameter that needs to be added is the ESD clamp capacitance, which was calculated to be 0.3 pF, based on design and process considerations. This is a good approximation for a first-order model. When the lumped capacitance of the ESD diodes is added to the S-parameter model of rest of the device, the resulting lumped capacitance was 0.5 pF, and then confirmed in measurements of 0.5 pF at 1 MHz.

The model in Figure 1 allowed the frequency response of the ESD224 device to be simulated and optimized using ADS. The bandwidth of the device is shown by plotting the insertion loss over frequency and measuring where the –3 dB point occurs. For HDMI 2.0, the –3 dB point needs to be greater than 6 Gbps (3 GHz). Once the device design was finalized, characterization boards were designed and fabricated to measure the actual bandwidth of the ESD224. Figure 2 shows the board design. Since the bandwidth of the device itself is of primary concern, a calibration board was made to mimic the connectors and traces without the ESD224. The calibration board was then used to de-embed the ESD224 from the bandwidth board and show the bandwidth of the device alone (see Figure 3). In this graph, the plot Diff21_SIM is the differential bandwidth of the ESD224 as calculated by the simulation model. The plot Diff21_EVM is the differential bandwidth as measured on the calibration board.

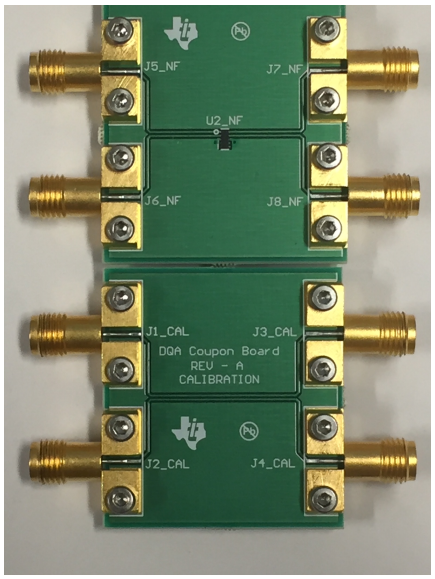

Figure 2. ESD224 Bandwidth and Calibration Board

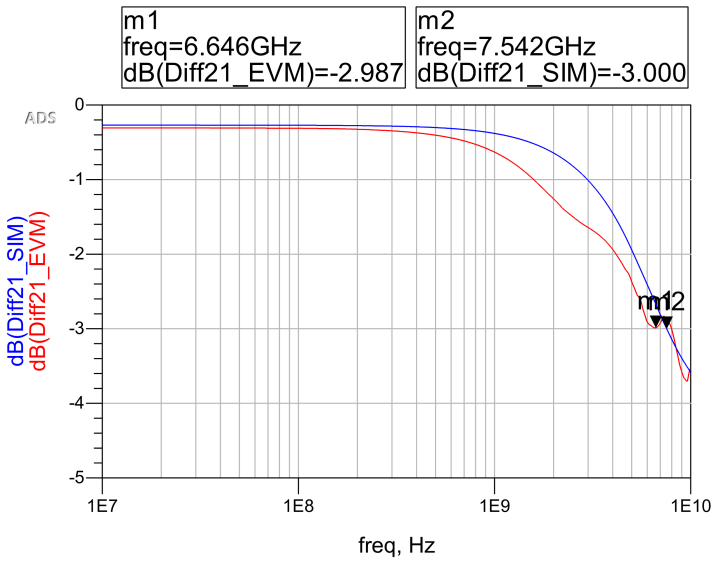

Figure 3. Insertion Loss From Simulation and Measurements

M1 is the –3 dB point of the measured results while M2 is the –3 dB point of the simulation results. It can be seen that the measured and simulated results diverge after approximately 1 GHz due to inconsistency in the simulation model vs the measured result. What is important is the simulation and measured results are a close approximation for a first-order model. This means that we are confident enough in our data to continue on with the testing.

2.2 Time Domain Response

Using the ADS *Time Domain Function*, it is also possible to simulate the *Time Domain Response* (TDR) test required for HDMI 2.0. TDR analysis uses a voltage source to generate a pulse with a specific rise time and then measure the reflections. TDR analyzes the impedance versus time to see the changes in impedance due to the connector, board traces, and the device itself. The TDR requirements of HDMI 2.0 are shown in Table 1.

Table 1. Sink Impedance Characteristics for 3.4 Gbps < R_{bit} ≤ 6.0 Gbps at TP2

Item	Value
TDR Rise Time at TP2 (10%–90%)	≤ 200 ps
Through Connection Impedance(1)	100 Ω ± 15%(2)
Sink Termination Impedance	90 Ω to 100 Ω

(1) Impedance from TP2 to *Sink Termination*.
(2) A single excursion is permitted out to a maximum or minimum of 100 Ω ±25% and of duration less than 250 ps.

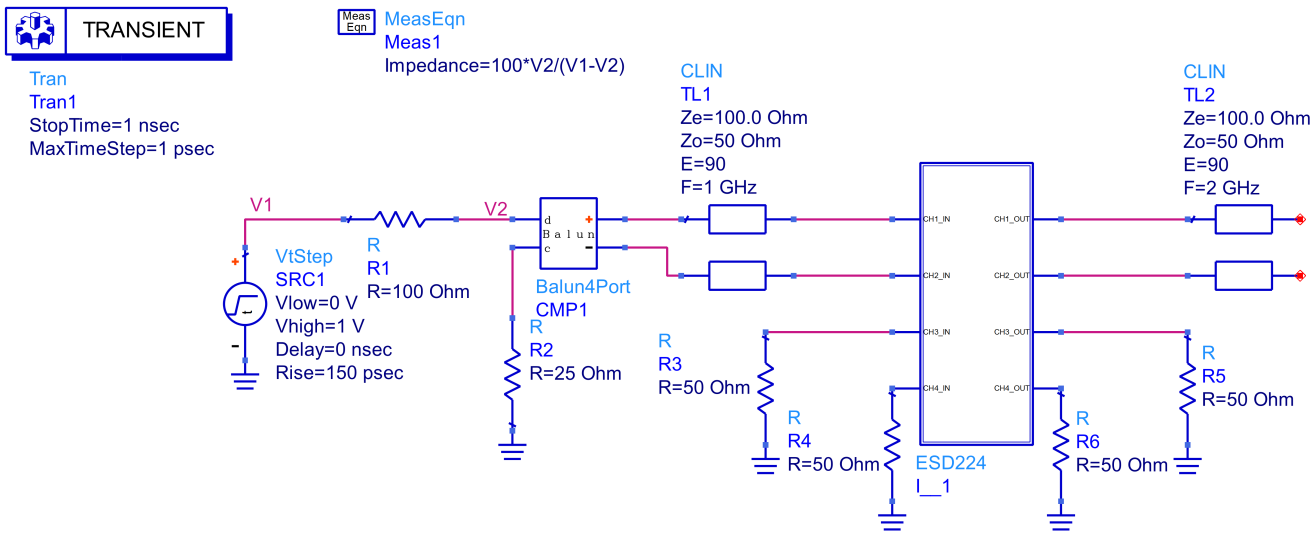

Figure 4. HDMI® 2.0 TDR Schematic With ESD224

Using the simulation setup in Figure 4 the results were obtained in Figure 5. When this simulation is run, the result shows a TDR that meets the requirement of a single excursion of 100 Ω ±25% for 250-ps maximum rise time as shown in Table 1.

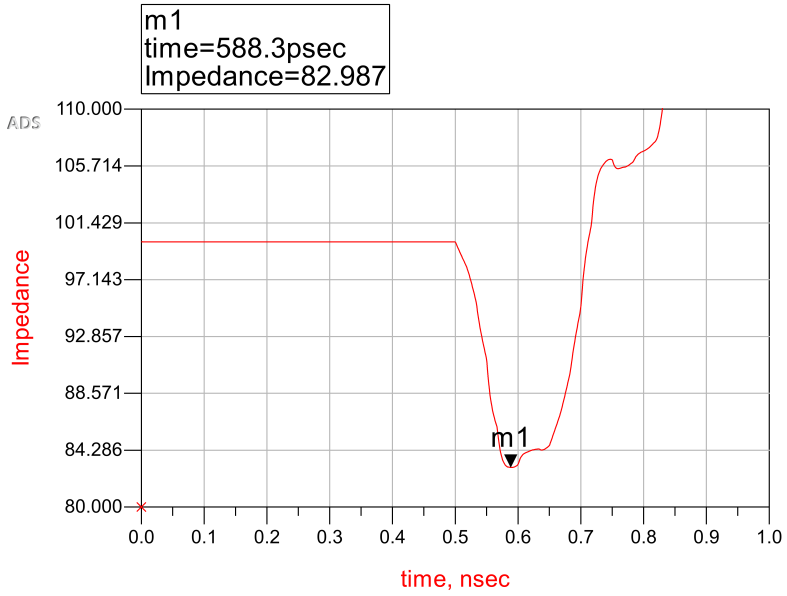

Figure 5. TDR Simulation With ESD224

Simulated TDR results were verified using actual TDR measurments. The same board that was used to do the bandwidth measurements of the ESD224 was used to do the TDR measurements. Two of the connectors were connected to an oscilloscope to do the measurement while the other side was left open. Figure 6 shows the measurement data taken. This measurement was taken at 150-ps rise time in compliance with the HDMI 2.0 requirement.

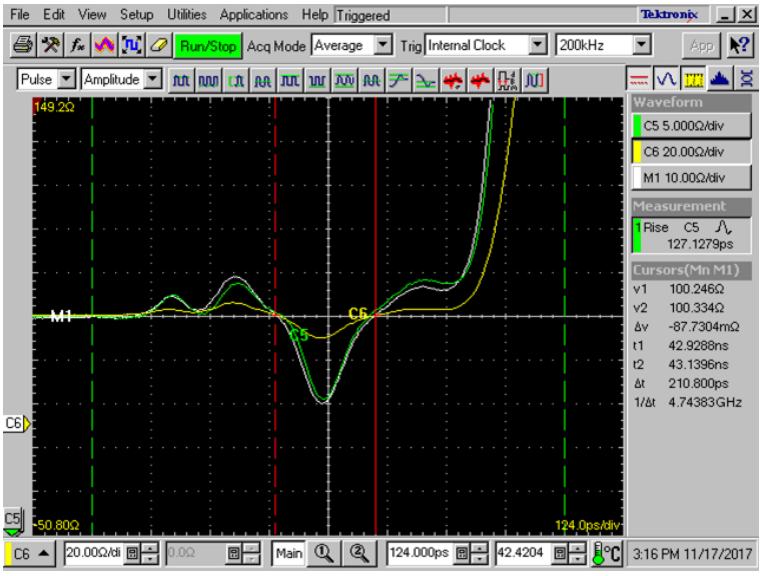

Figure 6. TDR Measurement Data

Figure 6 shows two single-ended measurements, C5 and C6, and the differential measurement of M1. Note that each of these graphs have a different scaling. The M1 plot is on 10 Ω/div while the C5 graph is 5 Ω/div and the C6 plot is 20 Ω/div. The middle line of the X axis set at 100 Ω for the M1 differential measurement. The first two peaks that show up in the plots are from the SMA connector and the traces leading up to the actual device. The device shows up as the valley in the middle of the graph. This valley is representative of the ESD224 device which is dominated by the lumped capacitance of the ESD diode

inside the IC. As is shown by the red cursors on the graph, the excursion is at 210 ps and from the M1 plot it can be seen that the minimum point is > 80 Ω, both of which meet the requirement of the HDMI 2.0 standard. The small peak after the device is the second connector and associated traces but since the device overshadows it, it looks like just one lump. After the last connector, the board connection is open so the impedance goes to infinity.

2.3 HDMI® 2.0 Simulation

After having confirmed good correlation in the bandwidth and TDR measurements between the simulated and measured device data, the ESD224 was simulated in a HDMI 2.0 compliance test bench to ensure that it could pass the required eye diagram. The ADS software from Keysight Technologies contains an *HDMI 2.0 Compliance Test Bench*. The ESD224 S-Parameter model generated earlier was inserted in the appropriate location in the ADS HDMI test bench.

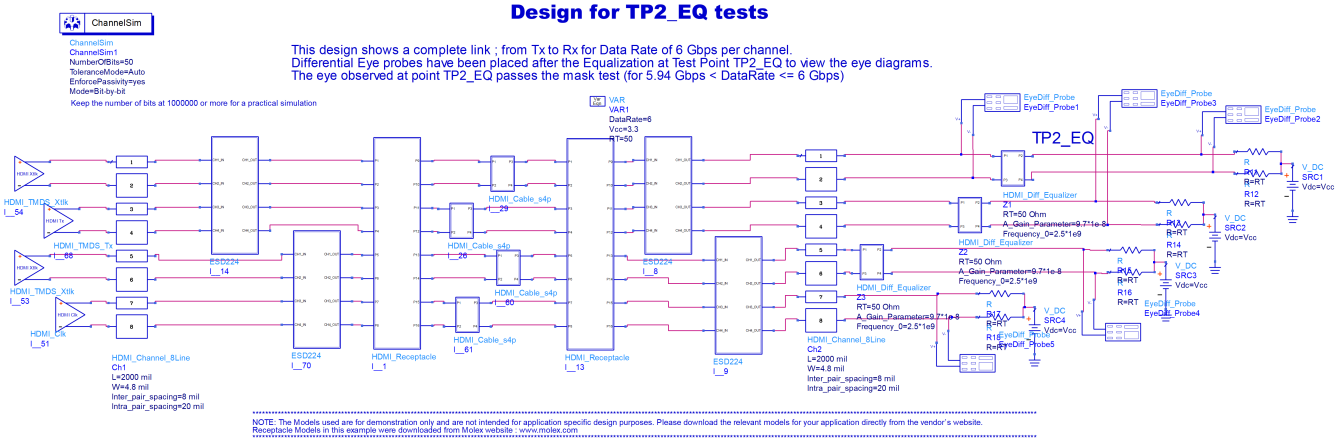

Figure 7. HDMI® 2.0 Compliance Test Bench Circuit With ESD224

Running the simulation yielded a passing eye diagram for HDMI 2.0.

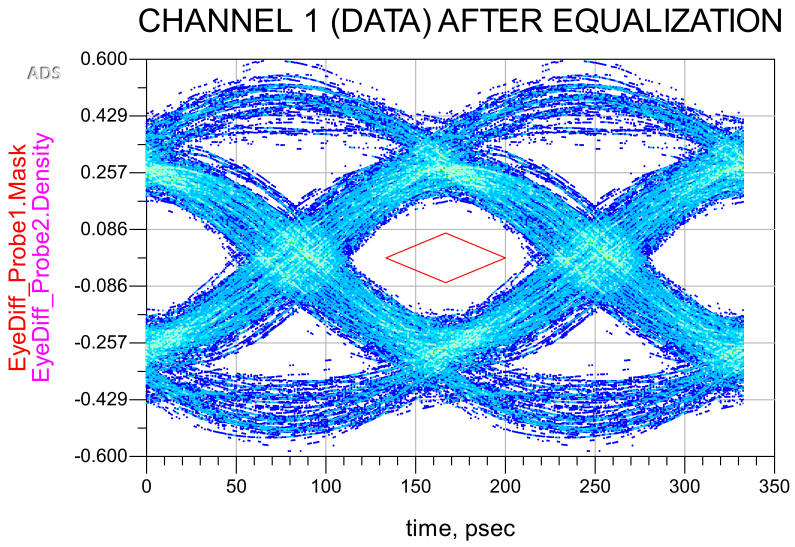

Figure 8. Eye Diagram from Simulation With ESD224

3 HDMI® Compliance Data From Testing with TDP158

With the confidence from the simulations of bandwidth, TDR, and HDMI 2.0 compliance test bench, the ESD224 was placed onto the TDP158RSBEVM.

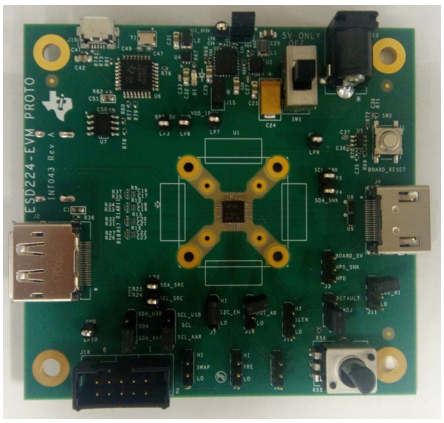

Figure 9. TDP158RSBEVM With ESD224

The TDP158 evaluation module (EVM) is used to characterize the HDMI 2.0 retimer from Texas Instruments. The TDP158EVM board had all of the relevant items for HDMI 2.0 compliance testing so to modify it for HDMI compliance with the ESD224 was straightforward. The ESD224s (U8, U9) were placed near the HDMI connector for best protection of the HDMI port. After making the board, the HDMI 2.0 testing needed to be done. This involved sending signals to the retimer on the clock, and data lines having them pass through the ESD224, and then were read on an oscilloscope running HDMI 2.0 compliance software. Figure 10 shows this setup.

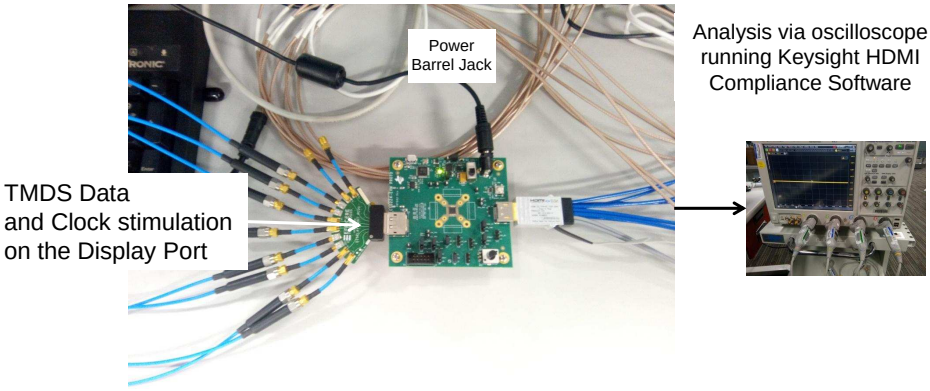

Figure 10. EVM Connected Between HDMI® Source and Sink

The HDMI 2.0 compliance test consists of testing VL, rise time and fall time, inter- and intra-pair skew, differential voltage, clock duty cycle, clock jitter, data eye diagram, and differential impedance. More information about the HDMI compliance tests is found in *TI ESD Protection Devices and the HDMI CTS*.

3.1 Measured Data

Table 2 shows the results of the HDMI compliance tests.

Table 2. HDMI® Test Report

Overall Result: Pass	
Test Configuration Details	
Device Description	
Device ID	Transmitter
Fixture Type	N1080H04
Probe Connection	4 Probes
Probe Head Type	N5380A/B
Lane Connection	1 Data Lane
HDMI Specification	2.0
HDMI Test Type	TMDS Physical Layer Tests
Test Session Details	
Infiniium™ SW Version	05.52.0004
Infiniium Model Number	DSOX91604A
Infiniium Serial Number	MY50270161
Application SW Version	2.12.0001
Debug Mode Used	No
Probe (Channel 1)	Model: 1169A
	Serial: US49410841
	Head: N5380A/B
	Atten: Calibrated (15 NOV 2017 13:33:51), Using Cal Atten (2.0177E+000)
	Skew: Calibrated (15 NOV 2017 13:34:04), Using Cal Skew
Probe (Channel 2)	Model: 1169A
	Serial: US44005778
	Head: N5380A/B
	Atten: Calibrated (15 NOV 2017 13:28:35), Using Cal Atten (2.1007E+000)
	Skew: Calibrated (15 NOV 2017 13:28:48), Using Cal Skew
Probe (Channel 3)	Model: 1169A
	Serial: US49411926
	Head: N5380A/B
	Atten: Calibrated (15 NOV 2017 13:29:49), Using Cal Atten (2.0610E+000)
	Skew: Calibrated (15 NOV 2017 13:30:01), Using Cal Skew
Probe (Channel 4)	Model: 1169A
	Serial: US53270572
	Head: N5380A/B
	Atten: Calibrated (15 NOV 2017 13:31:07), Using Cal Atten (2.1060E+000)
	Skew: Calibrated (15 NOV 2017 13:31:23), Using Cal Skew
Last Test Date	2017-11-17 14:12:54 UTC -06:00

Table 3 shows a summary of the results showing the margin of passing.

Table 3. Summary of Results with Margins

Pass	Test Name	Actual Value	Margin	Pass Limits
Yes	HF1-2: Clock Rise Time	142.907 ps	90.5 %	VALUE >= 75.000 ps
Yes	HF1-2: Clock Fall Time	142.120 ps	89.5 %	VALUE >= 75.000 ps
Yes	HF1-6: Clock Duty Cycle(Minimum)	49.230	23.1 %	>=40%
Yes	HF1-6: Clock Duty Cycle(Maximum)	49.990	16.7 %	<=60%
Yes	HF1-7: Differential Clock Voltage Swing, Vs (TP1)	506 mV	13.3 %	400 mV < VALUE < 1.200 V
Yes	HF1-7: Clock Jitter (TP2_EQ with Worst Case Positive Skew)	136 mTbit	54.7 %	VALUE <= 300 mTbit
Yes	HF1-7: Clock Jitter (TP2_EQ with Worst Case Negative Skew)	134 mTbit	55.3 %	VALUE <= 300 mTbit
Yes	HF1-5: D0 Maximum Differential Voltage	571 m	26.8 %	VALUE <= 780 m
Yes	HF1-5: D0 Minimum Differential Voltage	–540 m	30.8 %	VALUE >= –780 m
Yes	HF1-2: D0 Rise Time	62.478 ps	47.0 %	VALUE >= 42.500 ps
Yes	HF1-2: D0 Fall Time	59.785 ps	40.7 %	VALUE >= 42.500 ps
Yes	HF1-8: D0 Mask Test (TP2_EQ with Worst Case Positive Skew)	0.000	50.0 %	No Mask Failures
Yes	HF1-8: D0 Mask Test (TP2_EQ with Worst Case Negative Skew)	0.000	50.0 %	No Mask Failures
Yes	HF1-1: VL Clock +	2.894 V	25.8 %	2.300 V <= VALUE <= 3.100 V
Yes	HF1-1:Clock + VSwing	257 mV	14.3 %	200 mV <= VALUE <= 600 mV
Yes	HF1-1: VL Clock –	2.891 V	26.1 %	2.300 V <= VALUE <= 3.100 V
Yes	HF1-1:Clock - VSwing	257 mV	14.3 %	200 mV <= VALUE <= 600 mV
Yes	HF1-4: Intra-Pair Skew - Clock	116 mTbit	11.3 %	–150 mTbit <= VALUE <= 150 mTbit
Yes	HF1-1: VL D0+	2.570 V	45.0 %	2.300 V <= VALUE <= 2.900 V
Yes	HF1-1: D0+ VSwing	444 mV	22.0 %	400 mV <= VALUE <= 600 mV
Yes	HF1-1: VL D0–	2.531 V	38.5 %	2.300 V <= VALUE <= 2.900 V
Yes	HF1-1: D0- VSwing	453 mV	26.5 %	400 mV <= VALUE <= 600 mV
Yes	HF1-4: Intra-Pair Skew - Data Lane 0	14 mTbit	45.3 %	–150 mTbit <= VALUE <= 150 mTbit
Yes	HF1-5: D1 Maximum Differential Voltage	573 m	26.5 %	VALUE <= 780 m
Yes	HF1-5: D1 Minimum Differential Voltage	-534 m	31.5 %	VALUE >= –780 m
Yes	HF1-2: D1 Rise Time	66.171 ps	55.7 %	VALUE >= 42.500 ps
Yes	HF1-2: D1 Fall Time	66.123 ps	55.6 %	VALUE >= 42.500 ps
Yes	HF1-8: D1 Mask Test (TP2_EQ with Worst Case Positive Skew)	0.000	50.0 %	No Mask Failures
Yes	HF1-8: D1 Mask Test (TP2_EQ with Worst Case Negative Skew)	0.000	50.0 %	No Mask Failures
Yes	HF1-1: VL D1+	2.560 V	43.3 %	2.300 V <= VALUE <= 2.900 V
Yes	HF1-1: D1+ VSwing	440 mV	20.0 %	400 mV <= VALUE <= 600 mV
Yes	HF1-1: VL D1–	2.527 V	37.7 %	2.300 V <= VALUE <= 2.900 V
Yes	HF1-1: D1- VSwing	479 mV	39.5 %	400 mV <= VALUE <= 600 mV
Yes	HF1-4: Intra-Pair Skew - Data Lane 1	–13 mTbit	45.7 %	–150 mTbit <= VALUE <= 150 mTbit
Yes	HF1-5: D2 Maximum Differential Voltage	609 m	21.9 %	VALUE <= 780 m
Yes	HF1-5: D2 Minimum Differential Voltage	–563 m	27.8 %	VALUE >= –780 m
Yes	HF1-2: D2 Rise Time	64.868 ps	52.6 %	VALUE >= 42.500 ps
Yes	HF1-2: D2 Fall Time	71.854 ps	69.1 %	VALUE >= 42.500 ps
Yes	HF1-8: D2 Mask Test (TP2_EQ with Worst Case Positive Skew)	0.000	50.0 %	No Mask Failures

Table 3. Summary of Results with Margins (continued)

Pass	Test Name	Actual Value	Margin	Pass Limits
Yes	HF1-8: D2 Mask Test (TP2_EQ with Worst Case Negative Skew)	0.000	50.0 %	No Mask Failures
Yes	HF1-1: VL D2+	2.514 V	35.7 %	2.300 V <= VALUE <= 2.900 V
Yes	HF1-1: D2+ VSwing	488 mV	44.0 %	400 mV <= VALUE <= 600 mV
Yes	HF1-1: VL D2–	2.461 V	26.8 %	2.300 V <= VALUE <= 2.900 V
Yes	HF1-1: D2- VSwing	486 mV	43.0 %	400 mV <= VALUE <= 600 mV
Yes	HF1-4: Intra-Pair Skew - Data Lane 2	2 mTbit	49.3 %	–150 mTbit <= VALUE <= 150 mTbit

Figure 11 through Figure 16 illustrate pictures of the key data measurements.

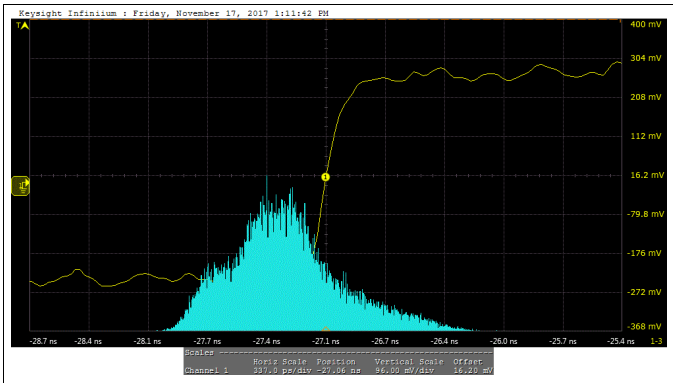

Figure 11. Clock Rise Time

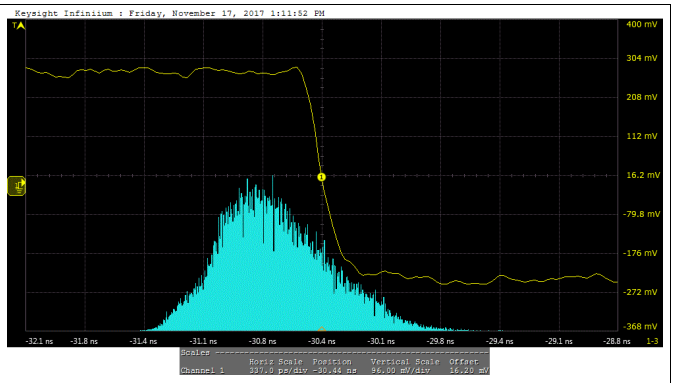

Figure 12. Clock Fall Time

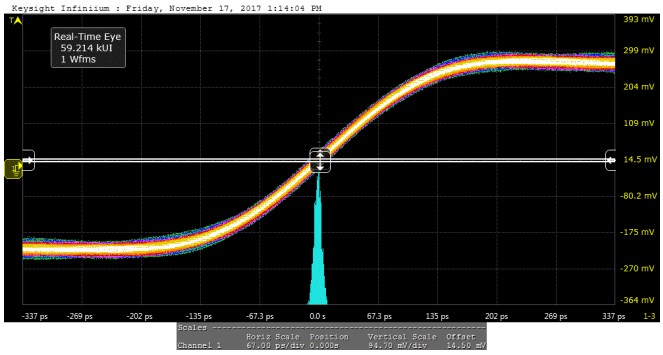

Figure 13. Clock Jitter (With Worst-Case Positive Skew)

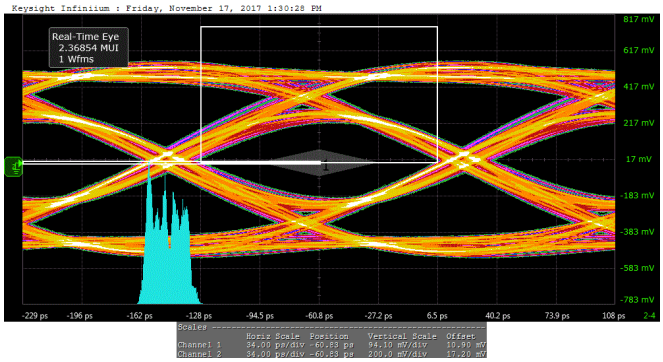

Figure 14. Data Lane 0 Mask Test

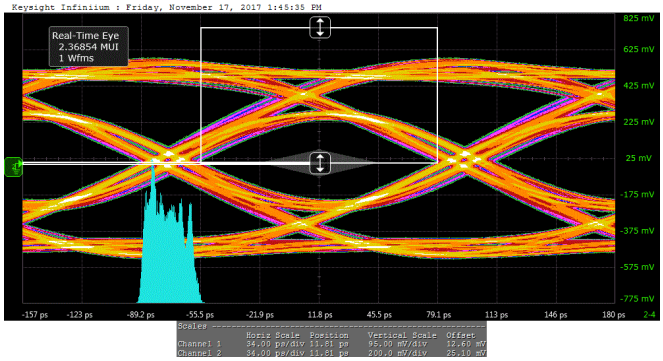

Figure 15. Data Lane 1 Mask Test

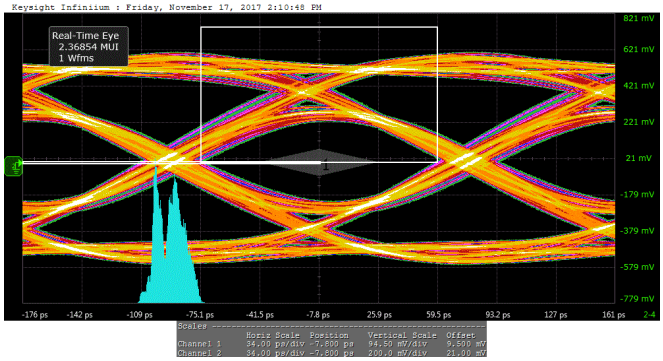

Figure 16. Data Lane 2 Mask Test

These eye diagrams can be compared to the EVM board without any ESD protection.

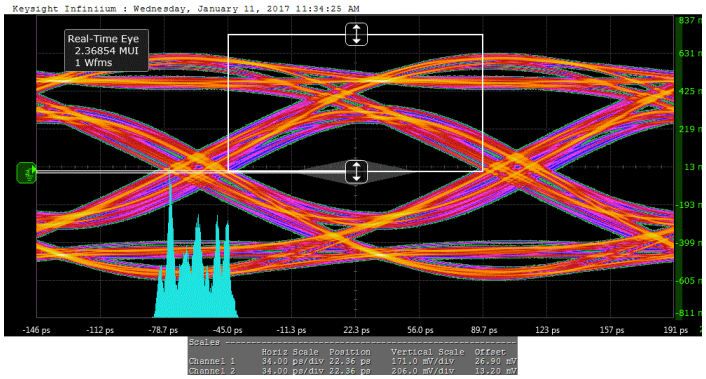

Figure 17. TDP158RSBEVM Without ESD224 Data Lane 2 Mask Test

4 ESD224 Protection of Down Stream Devices

The ESD224 has internal circuitry that allows the device to have a low system-side clamping voltage during ESD tests. In order to show the low clamping voltage of the device, a board was built with the ESD224 protecting the HDMI lines of the BCM7250 Broadcom SoC used in STBs. This board allowed the HDMI lines to be struck with an ESD pulse in various scenarios. These scenarios are striking the line through a cable, striking the BCM7250 chip with just ESD224 protection, striking BCM7250 chip with ESD224 and common-mode choke (CMC) protection, and striking BCM7250 with TPD4E02B04 and CMC protection for comparison.

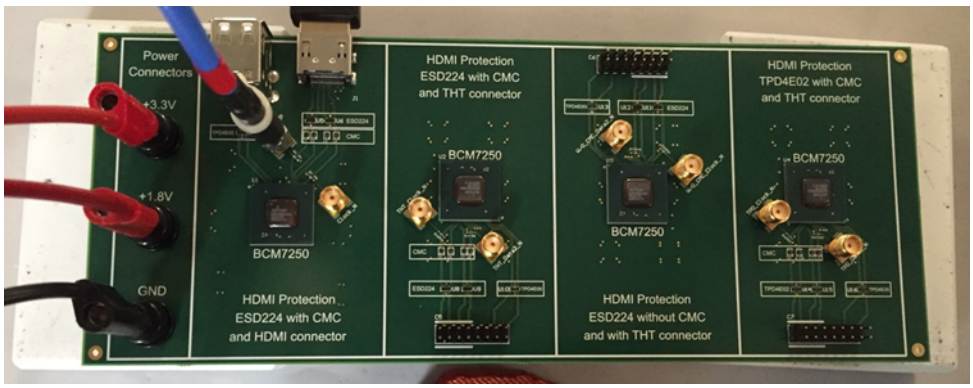

Figure 18. ESD224 Clamping PCB

In order to know what the clamping voltage that the BCM7250 downstream sees, SMA headers were placed hanging off of the HDMI lines to see the clamping waveform during an ESD strike. The device was then struck on the individual HDMI lines and the clamping voltage measured on an oscilloscope.

It is also important to note that the BCM7250 was powered on so that all of its internal ESD structures were biased to the correct level. The board was struck with ±8 kV according to the IEC 61000-4-2 standard and the clamping waveform was captured. The clamping voltage of an ESD diode is defined at 30 ns. This shows that the clamping voltage is 7.8 V at 30 ns for +8-kV ESD strike and –5 V at 30 ns for –8-kV ESD strike.

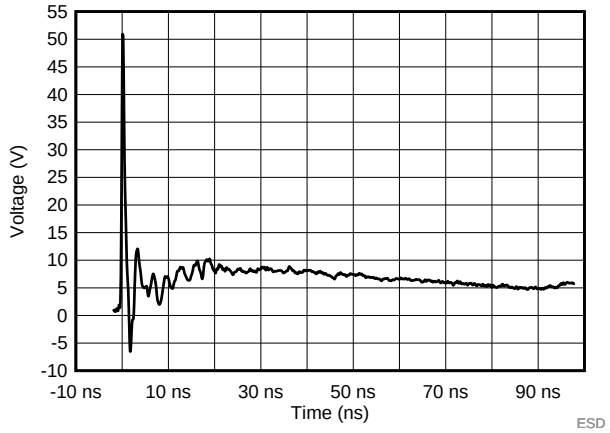

Figure 19. ESD224 ESD Clamping Waveform +8-kV With BCM7250

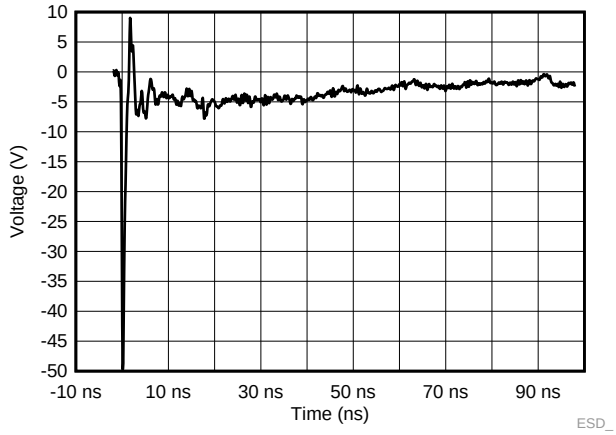

Figure 20. ESD224 ESD Clamping Waveform –8-kV With BCM7250

This clamping waveform is a reflection also of how much current the BCM7250 draws. The internal series clamping circuit is designed to limit the residual ESD current flowing through the downstream device and drop a portion of the clamping voltage across the series clamping circuit to reduce the voltage presented to the system side.

When the system device downstream fails, the leakage into that pin will change. For the BCM7250 the leakage into the pin during powered on mode and before the ESD strike is 8.67 µA. After the ESD strike occurs, the leakage was 8.7 µA, showing that the device has not been damaged.

5 Summary

The process from design to validation that TI undergoes is thorough, allowing TI to accurately predict the behavior of the devices during every stage of the device cycle. The ESD224 device was specifically made with the specifications in order to provide the most robust solution possible. Even though the ESD224 is a non-flow through device, the ESD224 is an ultra-low clamping, HDMI-compliant ESD protection device. It provides protection for the TMDS data and clock lines while also allowing the system to be compliant with the HDMI protocol.

6 References

- Texas Instruments, *ESD224 Low Clamping 4-Channel ESD Protection Device for HDMI Interface Data Sheet*

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