Data-rate independent half-duplex repeater design for RS-485

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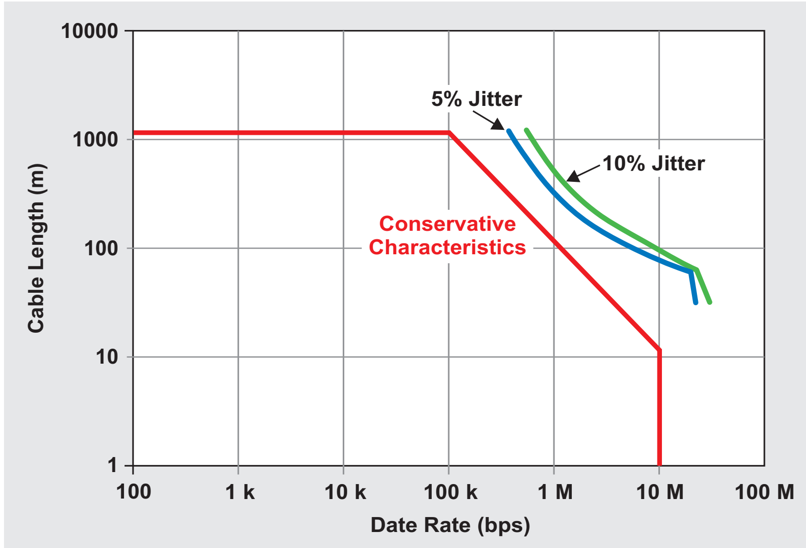
A question frequently posed by engineers is how to design a data-rate independent half-duplex repeater for RS-485 applications. Examples include designing a long-haul network beyond the suggested maximum cable length of 1200 m, adding long stubs to an existing network, or designing a network using a star topology. The data rates applied can vary between systems from 10 kbps up to 200 kbps.

Ground-potential differences (GPDs) between remotely located nodes can assume voltages exceeding the maximum common-mode voltage range of most bus transceivers, making galvanic isolation necessary between the network node electronics and the bus.

In Reference 1, the characteristic for cable length versus data rate suggests that a maximum cable length of 1200 m, or about 4000 ft, should be used (Figure 1). At this length, the resistance of the commonly applied 120-Ω, AWG24 unshielded twisted-pair (UTP) cable approaches the value of the termination resistor and reduces the bus signal swing by half, or 6 dB.

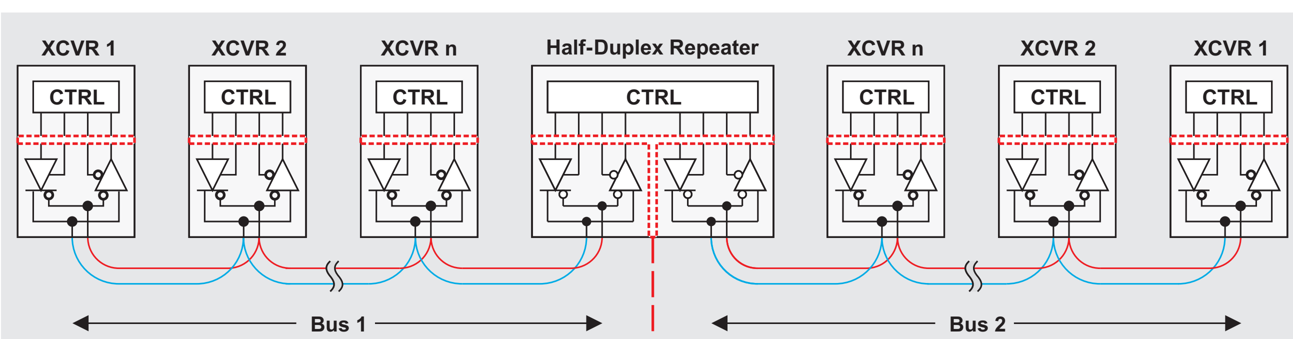
In RS-485 literature, transceiver datasheets often show a full-duplex repeater design for simplicity's sake. In long-haul networks, however, it is undesirable to run a full-duplex cable for thousands of meters because cable and wiring are very expensive.

Figure 1. Cable length versus data rate



To operate an extended long-haul network in half-duplex mode, implementing a half-duplex repeater is a must. A system block diagram is shown in Figure 2. Because a half-duplex repeater interfaces to two bus segments, the repeater must comprise two separate transceivers, each connecting to its respective bus via signal isolators, and a control logic isolated from both transceiver sections. The control logic performs timely enabling and disabling of the repeater's driver and receiver sections. This is initiated by the incoming data signal from either direction.

Figure 2. Bus extension with dual isolated half-duplex repeater



The two most commonly applied timing-control methods are the one-shot circuit in Figure 3 and the inverting buffer with a time delay in Figure 4. To ensure correct switching behavior, both methods require defined start conditions after power up and bus idling. This is accomplished through fail-safe biasing resistors, R_{FS}, which create a fail-safe voltage, V_{FS}, above the receiver input sensitivity of V_{FS} > +200 mV when no transceiver is actively driving the bus.

A run-through of the one-shot circuit's functional sequence (numbered here and in Figure 3) clarifies the repeater operation:

1. During bus idling, the receiver outputs of both repeater ports are high due to V_{FS}. Thus, both transceivers hold each other in receive mode.
2. Next, the arriving start bit of an incoming data packet on port 1 drives the output of RX_1 low. This transition triggers the one-shot circuit, driving its output high and enabling driver DR_2.
3. The time constant, $R_D \times C_D$, must be so calculated that the one-shot circuit's output remains high for the entire time of the data packet.
4. DR_2 continues driving bus 2 for the duration of the one-shot time constant. $XCVR_{OUT}$ represents the receiver output state of a remote transceiver on bus 2. Note that while DR_2 is enabled, the pull-up resistor, R_{PU}, pulls the disabled receiver's (RX_2's) output high in order to keep RX_1 enabled.

A drawback of this solution is that the R-C time constant depends on the data-packet length and the data rate at which the signal is transmitted. Also, one-shot circuits are sensitive to noise transients, which can cause false triggering and repeater breakdown.

Figure 3. Transceiver timing control with a one-shot circuit

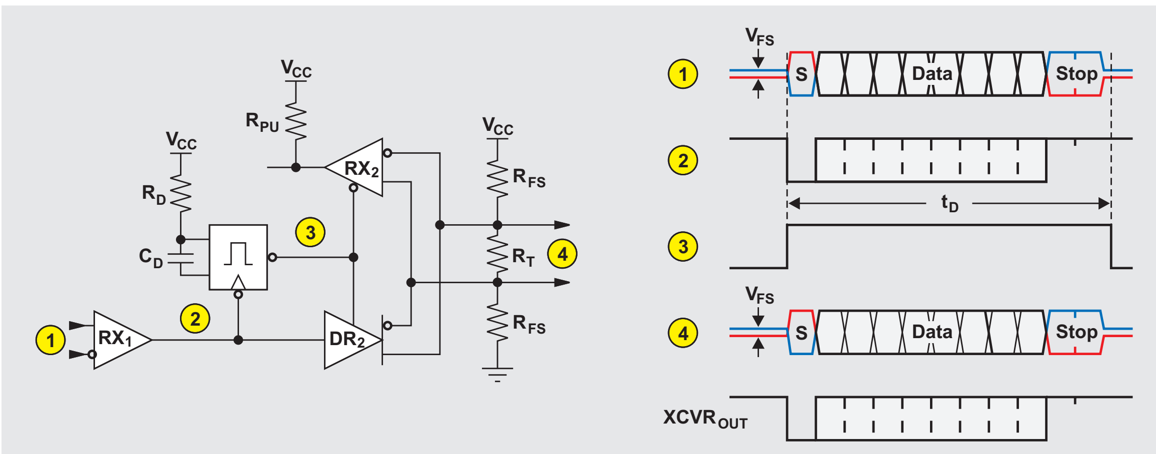
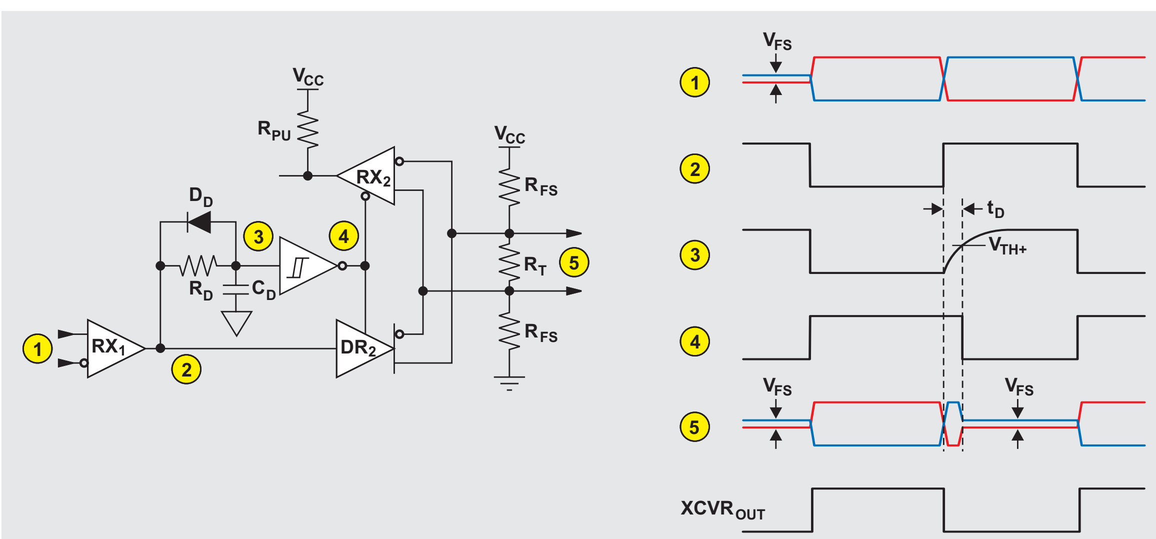


Figure 4. Transceiver timing control with an inverting buffer



Nevertheless, one-shot circuits are used often in interface bridges such as RS-232 to RS-485 converters. These converters directly connect an RS-485 network to the RS-232 ports of older PCs or RS-232-controlled machinery.

A more robust and data-rate-independent alternative to the one-shot circuit is timing control through an inverting Schmitt-trigger buffer with different charge and discharge times. The underlying principle is to actively drive a bus during logic-low states and to disable the driver during logic-high states. The enabling and disabling sequences then occur on a per-bit basis, which makes the repeater function independent of data rate and packet length.

A run-through of the inverter-controlled repeater's functional sequence (numbered here and in Figure 4) clarifies its operation:

1. During bus idling, the receiver outputs of both repeater ports are high due to V_{FS}. The delay capacitor, C_D, is fully charged, driving the inverter output low to maintain the transceiver in receive mode.
2. Then a low bit on bus 1, driving the output of RX_1 low, rapidly discharges C_D and enables driver DR_2.
3. When the bus voltage turns positive (V_{Bus} > 200 mV), the output of RX_1 turns high, which drives DR_2's output high and slowly charges C_D via R_D. The minimum time constant ($R_D \times C_D$) must be so calculated that at the maximum supply voltage, $V_{CC(max)}$, and the minimum positive inverter input threshold, $V_{TH+(min)}$, the delay time, t_D, exceeds the maximum low-to-high propagation delay, $t_{PLH(max)}$, of the driver by, say, 30%. For example, given a capacitance of C_D = 100 pF, the required resistor value for R_D is

$$R_D = \left| \frac{1.3 \times t_{PLH(max)}}{C_D \times \ln\left(1 - V_{TH+(min)}/V_{CC(max)}\right)} \right|.$$

4. The driver enable time is extended by the delay time (t_D) versus the actual data-bit interval to establish a valid high signal on the bus. This is done prior to switching from transmit to receive mode in order to keep the receiver output continuously high. Because the propagation delays of receivers are shorter than those of drivers, it is impossible for the receiver to turn low, not even for a short instant. Once the driver is disabled, the external fail-safe resistors bias bus 2 to above 200 mV, which is seen by the active receiver as a defined high.
5. The differential output voltages on bus 2 are V_{OD} = V_{FS} > +200 mV during an idle bus, V_{OD} < 1.5 V for a low bit, and V_{OD} > 1.5 V for the time delay (t_D) at the beginning of a high bit. Afterwards, $V_{OD} = V_{FS}$ > +200 mV for the remainder of a high bit.

Again, $XCVR_{OUT}$ represents the receiver output state of a remote transceiver on bus 2. While legacy repeater designs typically were limited to data rates of 10 kbps, modern transceivers with shorter propagation delays allow for higher data rates of up to 100 kbps and more.

For simplicity, the repeater discussion has so far excluded the important aspect of galvanic isolation. However, in long-haul networks—the main application field of repeaters—large ground-potential differences (GPDs) between network nodes are common. These GPDs present themselves as large common-mode voltages across the transceiver inputs and can damage a device if not eliminated through galvanic isolation. When a transceiver's bus circuitry is isolated from its control circuitry, the bus system is floating and independent from a local node's ground potential.

Figure 2 shows the driver and receiver section of a bus node being isolated from the node's control circuitry. However, in the case of the repeater, dual isolation is required because the inner control logic must be isolated from bus 1 and bus 2. Furthermore, the two buses must be isolated from each other. A repeater circuit accomplishing this is shown in Figure 5, accompanied by its bill of material (BOM) in Table 1. The circuit uses two isolated RS-485 transceivers, each requiring a separate, isolated supply, V_{ISO}, derived from the central 3.3-V supply of the control section (Figure 6).

Conclusion

A repeater can be used as a bus extender or a stub extender. For a bus extender, a repeater builds the end of one bus and the beginning of another. This allows a fixed installation of fail-safe and termination resistors at both ports. When a repeater is used as an extender for long stubs, however, it can be located anywhere in the network. In this case the resistors at the port side connecting to the bus should be removed, while the resistors at the stub port can remain installed.

Reference

1. "Application Guidelines for TIA/EIA-485-A," TIA TSB-89, January 1, 2006. Available at www.global.ihs.com

Table 1. BOM for the repeater's signal path

DESIGNATOR	FUNCTION	DEVICE/VALUE	SUPPLIER
U1, U2	Isolated half-duplex transceiver	ISO15DW	Texas Instruments
U3	Dual Schmitt-trigger inverter	SN74LVC2G14DBV	
R_{PU}	Pull-up resistor	4.7 kΩ	Vishay
R_{FS}	Fail-safe resistor	348 Ω	
R_T	Termination resistor	120 Ω	
R_D	Delay resistor	10 kΩ	
C_S	Storage capacitor	10 µF	
C_B	Bypass capacitor	0.1 µF	
C_D	Delay capacitor	100 pF	
D_D	Discharge diode	1N4448	

Related Web sites

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Replace *partnumber* with ISO15, SN6501, or SN74LVC2G14

Figure 5. Dual isolated half-duplex repeater

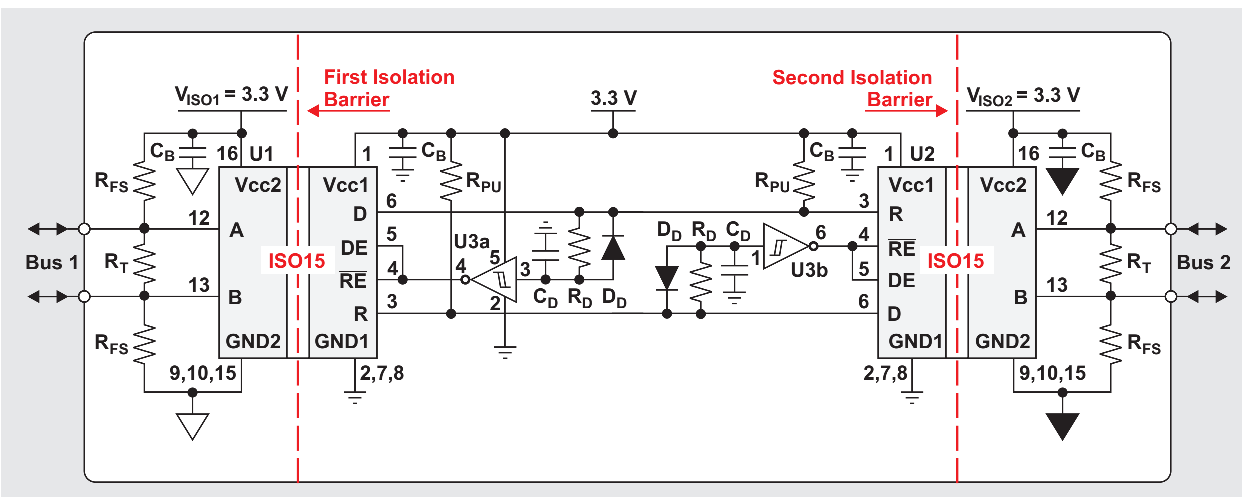
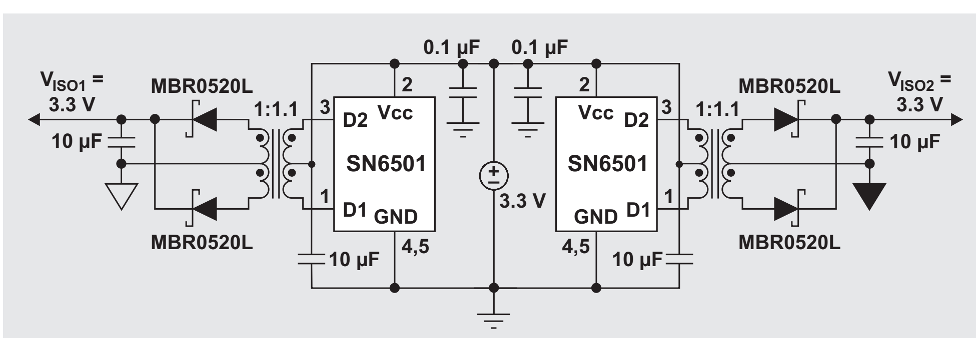


Figure 6. Design for dual isolated power supplies



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