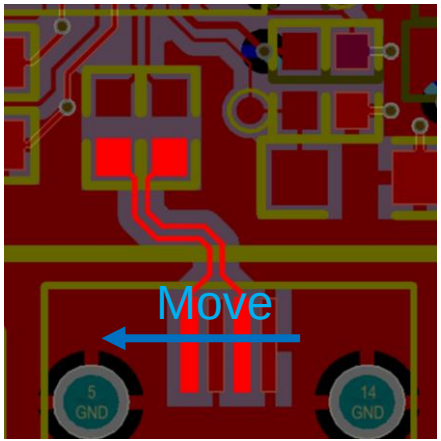
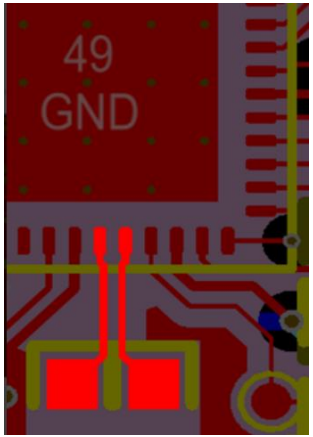
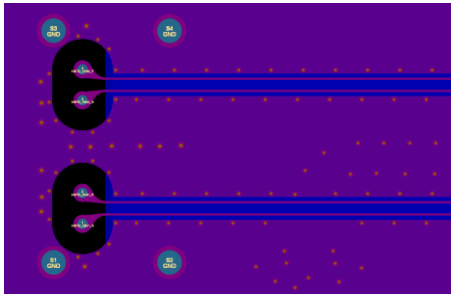
# 925 Review



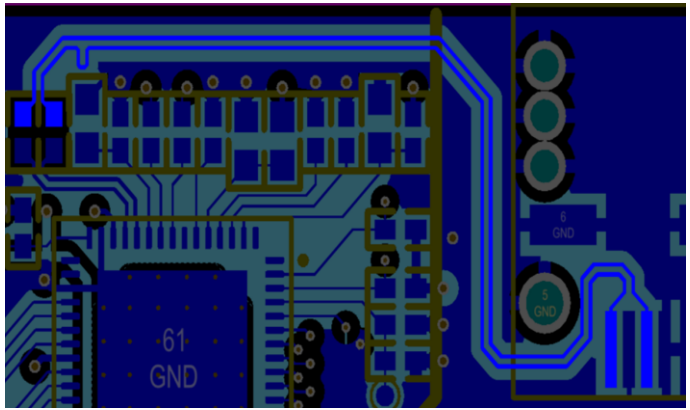



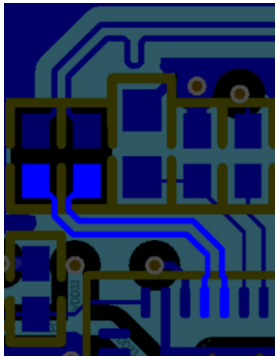



**Example of FPD Connector with GND stitching and straight routing along the High speed trace**

- Double check the thickness of the FPD traces in compare to the AC Caps Pads - Please ensure to use proper width to maintain 100 ohm impedance – Double check your differential path is meeting the 100 ohm impedance requirement based on trace width and PCB stack-up
- The highspeed trace width needs to be consistent with the AC Caps pad widths - We typically recommend to use 0402 or 0201 sized caps to minimize the pad size in order to ensure the parasitic capacitance can be controlled
- If there is room on PCB to move the connector to the left to have a straight line for the FPD signal that would provide a better signal path in layout
- Routing is normally restricted to 45-degree or right angle turns with typical layout so if there is a way to straighten those data lines that would be most optimal option

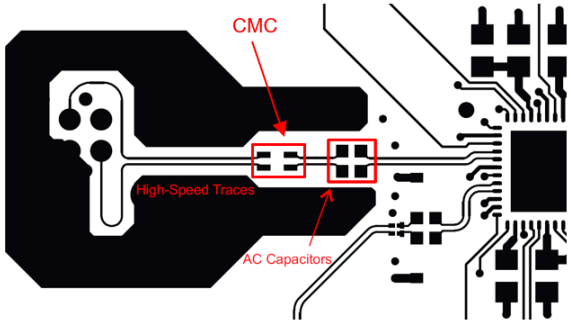
# 926 RIN Traces



- If no physical space limitations – it's best to have the AC caps closer to the pins, and make the traces thicker to ensure proper impedance between the contact of the AC cap pad and the FPD trace
- Minimize the overall length of the FPD trace as much as possible to avoid any cross-talk issues
- Avoid sharp turns in routing FPD signal path
- Typically straight lines are preferred in routing FPD traces
- Differential FPD signal routing commonly uses an optional CMC along the data path – Please refer to 925/926 EVM user guide for mode detail – This is optional for your design

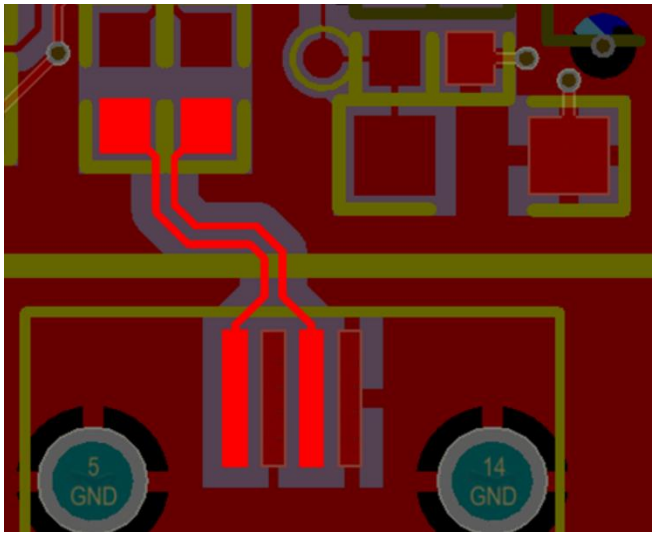
| | | | | | | |
|---|---|---|---|---|---|---|
| 1 | L1 | Z = 90 ohm | L/HDC-0805 | CHOKE COIL COMMON MODE 280MA SMD | Murata | DLW21SN900HQ2L |

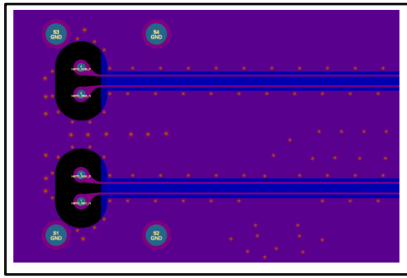



Example of a CMC

# FPD-Link Ux925 IC

- What layer is the FPD connector on? If 925 IC is on the top layer, the connector should be on the bottom layer to reduce stub



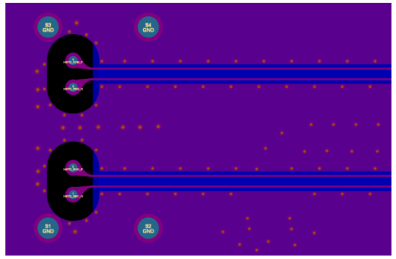



Example of FPD Connector with GND stitching along the High speed trace.

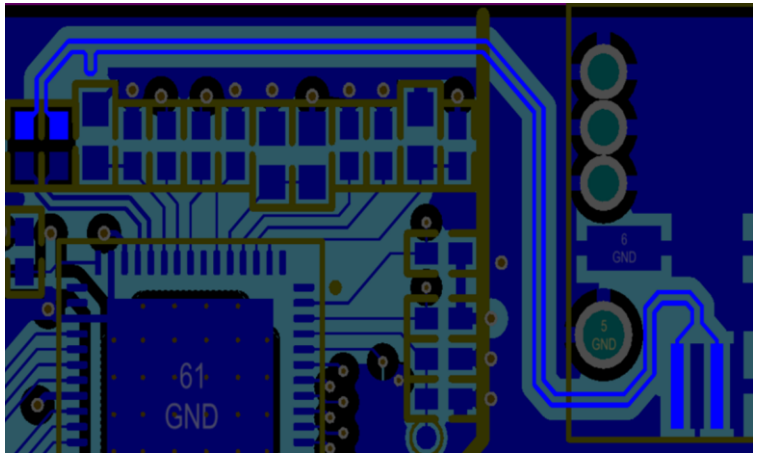
Is GND stitching available around the FPD lanes as shown in this example. It might be your software not having this toggled on but I don’t see GND stitching along the high speed paths

# FPD-Link Ux926 IC

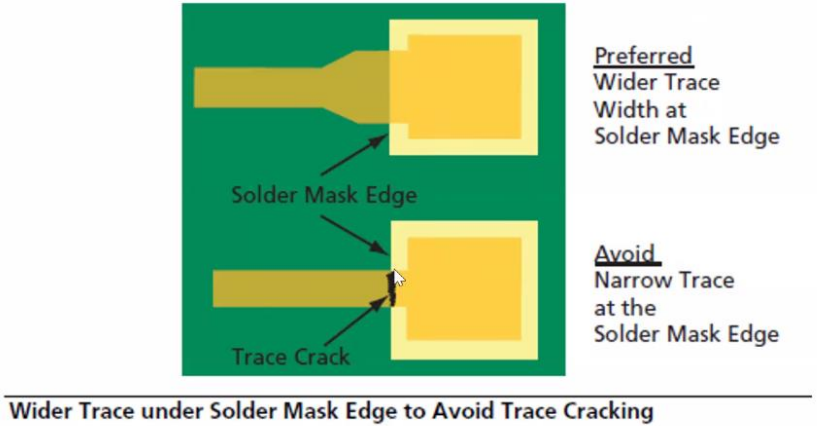
- What layer is the FPD connector on? If 926 IC is on the bottom layer, the connector should be on the top layer to reduce stub
- Is GND stitching available around the FPD lanes as shown in this example
- It might be your software not having this toggled on but I don't see GND stitching along the high speed paths
- Ensure your Serpentine routing meets the length matching requirements for the FPD signal



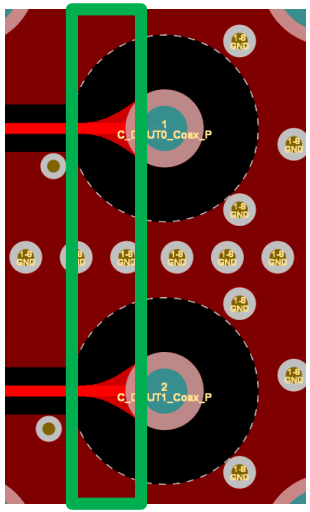
Example of FPD Connector with GND stitching along the High speed trace.



# General Connector Recommendation




Wider Trace under Solder Mask Edge to Avoid Trace Cracking




Customer is recommended to use winder trace at the connecter entry point

# General Feedback

- Try to avoid power polygons that are parallel to each other in separate planes, but not separated by a GND plane. This can cause coupling which can lead to excess noise

- Example of via stub (for connector feedback in previous slides):

**Figure 10-11. Example of Via Stub**

In Figure 10-12, the device is placed on the top layer as well as on a top-mount through-hole component. The differential signal traces, therefore, must use bottom trace routing to avoid the via stub. If the top trace routing restricts the top layer routing, the connector can be flipped and placed on the opposite side of the connector.

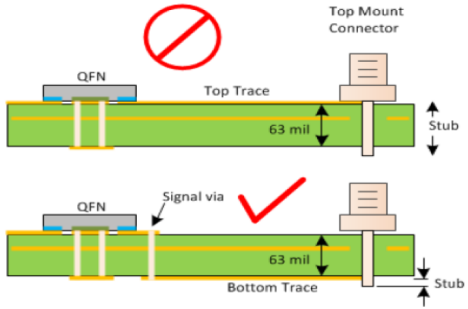



**Figure 10-12. Example of Voided Via Stub**

# Important notice and disclaimer

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.