ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Function	Description	Setting	
							Hex	Binary
0	0x00	I2C Device ID	[7:1]	RW	Device ID	7–bit address of Deserializer Note: Read-only unless bit 0 is set	3B	01110110
			0	RW	ID Setting	I2C ID Setting **0: Device ID is from IDx pin** 1: Register I2C Device ID overrides IDx pin	0	
1	0x01	Reset	[7:3]			Reserved		00000100
			2	RW	BC Enable	Back Channel Enable 0: Disable **1: Enable**	0	
			1	RW	Digital RESET1	Reset the entire digital block including registers. This bit is self-clearing. **0: Normal operation (default)** 1: Reset	0	
			0	RW	Digital RESET1	Reset the entire digital block except registers. This bit is self-clearing **0: Normal operation (default)** 1: Reset	0	
2	0x02	General	7	RW	OEN	LVCMOS Output Enable. Self-clearing on loss of LOCK **0: Disable, Tristate Outputs (default)** 1: Enable	0x00	00000000
			6	RW	OEN/OSS_ SEL Override	Output Enable and Output Sleep State Select override **0: Disable over-write (default)** 1: Enable over-write		
			5	RW	Auto Clock Enable	OSC Clock Output. Enable On loss of lock, OSC clock is output onto TxCLK± **0: Disable (default)** 1: Enable		
			4	RW	OSS_SEL	Output Sleep State Select. Enable Select to control output state during lock low period **0: Disable, Tri-State Outputs (default)** 1: Enable		
			3	RW	BKWD Override	Backwards Compatibility Mode Override **0: Use MODE_SEL pin (default)** 1: Use register bit to set BKWD mode		
			2	RW	BKWD Mode	Backwards Compatibility Mode Select **0: Backwards Compatibility Mode disabled (default)** 1: Backwards Compatibility Mode enabled		
			1	RW	LFMODE Override	Low Frequency Mode Override **0: Use LFMODE pin (default)** 1: User register bit to set LFMODE		
			0	RW	LFMODE	Low Frequency Mode **0: 15 MHz ≤ PCLK ≤ 85 MHz (default)** 1: 5 MHz ≤ PCLK < 15 MHz		
3	0x03	General Configuration 1	7			Reserved	0xF0	11110000
			6	RW	Back channel CRC Generator Enable	Back Channel CRC Generator Enable 0: Disable **1: Enable (default)**		
			5	RW	Failsafe	Outputs Failsafe Mode. Determines the pull direction for undriven LVCMOS inputs 0: Pullup **1: Pulldown (default)**		
			4	RW	Filter	HS, VS, DE two clock filter. When enabled, pulses less than two full PCLK cycles on the DE, HS, and VS inputs will be rejected 0: Filtering disable **1: Filtering enable (default)**		
			3	RW	I2C Pass-Through	I2C Pass-Through Mode Read/Write transactions matching any entry in the DeviceAlias registers will be passed through to the remote serializer I2C interface. **0: Pass-Through Disabled (default)** 1: Pass-Through Enabled		
			2	RW	Auto ACK	Automatically Acknowledge I2C transactions independent of the forward channel Lock state. **0: Disable (default)** 1: Enable		
			1	RW	DE Gate	Gate RGB data with DE signal. In DS90UH928, RGB data is gated with DE in order to allow packetized audio and block unencrypted data. In DS90UB928 or in Backward Compatibility mode, RGB data is not gated with DE by default. However, to enable packetized audio in DS90UB928, this bit must be set. This bit has no effect in DS90UH928		

					RGB	**0: Pass RGB data independent of DE in Backward Compatibility mode or interfacing to DS90UB925 or DS90UB927** 1: Gate RGB data with DE in Backward Compatibility mode or interfacing to DS90UB925 or DS90UB927		
			0			Reserved		
4	0x04	BCC Watchdog	[7:1]	RW	BCC Watchdog Timer	BCC Watchdog Timer The watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time. This field sets the Bidirectional Control Channel Watchdog Timeout value in units of 2 ms. This field should not be set to 0.	0xFE	11111110
			0	RW	BCC Watchdog Disable	Disable Bidirectional Control Channel Watchdog Timer **0: Enable (default)** 1: Disable		
5	0x05	I2C Control 1	7	RW	I2C Pass- All	I2C Pass-Through All Transactions. Pass all local I2C transactions to the remote serializer. **0: Disable (default)** 1: Enable	0x1E	00011110
			[6:4]	RW	I2C SDA Hold	Internal I2C SDA Hold Time. This field configures the amount of internal hold time is provided for the SDA input relative to the SCL input. Units are 50 ns.		
			[3:0]	RW	I2C Filter Depth	I2C Glitch Filter Depth. This field configures the maximum width of glitch pulses on the SCL and SDA inputs that will be rejected. Units are 5 ns.		
6	0x06	I2C Control 2	7	RW	Forward Channel Sequence Error	Control Channel Sequence Error Detected Indicates a sequence error has been detected in forward control channel. It this bit is set, an error may have occurred in the control channel operation.	0x00	00000000
			6	RW	Clear Sequence Error	Clears the Sequence Error Detect bit This bit is not self-clearing.		
			5			Reserved		
			[4:3]	RW	SDA Output Delay	SDA Output Delay This field configures output delay on the SDA output. Setting this value will increase output delay in units of 50ns. Nominal output delay values for SCL to SDA are: **00: 250 ns (default)** 01: 300 ns 10: 350 ns 11: 400 ns		
			2	RW	Local Write Disable	Disable Remote Writes to Local Registers through Serializer (Does not affect remote access to I2C slaves) **0: Remote write to local device registers (default)** 1: Stop remote write to local device registers		
			1	RW	I2C Bus Timer Speedup	Speed up I2C Bus Watchdog Timer **0: Timer expires after approximately 1 s (default)** 1: Timer expires after approximately 50 µs		
			0	RW	I2C Bus Timer Disable	Disable I2C Bus Watchdog Timer. When the I2C Watchdog Timer may be used to detect when the I2C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signaling occurs for approximately 1 second, the I2C bus is assumed to be free. If SDA is low and no signaling occurs, the device will attempt to		
7	0x07	Remote ID	[7:1]	R	Remote ID	Remote Serializer ID RW if bit 0 is set	0x00	00000000
			0	RW	Freeze Device ID	Freeze Serializer Device ID **0: Auto-load Serializer Device ID (default)** 1: Prevent auto-loading of Serializer Device ID from the remote device. The ID will be frozen at the value written.		
8	0x08	Slave ID[0]	[7:1]	RW	Slave Device ID0	7-bit Remote Slave Device ID 0 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID[0], the transaction will be re-mapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.	0x00	00000000
			0			Reserved		

9	0x09	Slave ID[1]	[7:1]	RW	Slave Device ID1	7-bit Remote Slave Device ID1 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID[1], the transaction will be re-mapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.	0x00	00000000
			0			Reserved		
10	0x0A	Slave ID[2]	[7:1]	RW	Slave Device ID2	7-bit Remote Slave Device ID2 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID[2], the transaction will be re-mapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.	0x00	00000000
			0			Reserved		
11	0x0B	Slave ID[3]	[7:1]	RW	Slave Device ID3	7-bit Remote Slave Device ID3 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID[3], the transaction will be re-mapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.	0x00	00000000
			0			Reserved		
12	0x0C	Slave ID[4]	[7:1]	RW	Slave Device ID4	7-bit Remote Slave Device ID4 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID[4], the transaction will be re-mapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.	0x00	00000000
			0			Reserved		
13	0x0D	Slave ID[5]	[7:1]	RW	Slave Device ID5	7-bit Remote Slave Device ID5 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID[5], the transaction will be re-mapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.	0x00	00000000
			0			Reserved		
14	0x0E	Slave ID[6]	[7:1]	RW	Slave Device ID6	7-bit Remote Slave Device ID6 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID[6], the transaction will be re-mapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.	0x00	00000000
			0			Reserved		
15	0x0F	Slave ID[7]	[7:1]	RW	Slave Device ID7	7-bit Remote Slave Device ID 7 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID[7], the transaction will be re-mapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.	0x00	00000000
			0			Reserved		
16	0x10	Slave Alias[0]	[7:1]	RW	Slave Device Alias 0	7-bit Remote Slave Alias 0 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID[0], the transaction will be re-mapped to the ID address before passing the transaction across the Bidirectional Control Channel to the Serializer.	0x00	00000000
			0			Reserved		
17	0x11	Slave Alias[1]	[7:1]	RW	Slave Device Alias 1	7-bit Remote Slave Alias 1 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID[1], the transaction will be re-mapped to the ID address before passing the transaction across the Bidirectional Control Channel to the Serializer.	0x00	00000000
			0			Reserved		
18	0x12	Slave Alias[2]	[7:1]	RW	Slave Device Alias 2	7-bit Remote Slave Alias 2 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID[2], the transaction will be re-mapped to the ID address before passing the transaction across the Bidirectional Control Channel to the Serializer.	0x00	00000000
			0			Reserved		

19	0x13	Slave Alias[3]	[7:1]	RW	Slave Device Alias 3	7-bit Remote Slave Alias 3 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID[3], the transaction will be re-mapped to the ID address before passing the transaction across the Bidirectional Control Channel to the Serializer.	0x00	00000000
			0			Reserved		
20	0x14	Slave Alias[4]	[7:1]	RW	Slave Device Alias 4	7-bit Remote Slave Alias 4 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID[4], the transaction will be re-mapped to the ID address before passing the transaction across the Bidirectional Control Channel to the Serializer.	0x00	00000000
			0			Reserved		
21	0x15	Slave Alias[5]	[7:1]	RW	Slave Device Alias 5	7-bit Remote Slave Alias 5 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID[5], the transaction will be re-mapped to the ID address before passing the transaction across the Bidirectional Control Channel to the Serializer.	0x00	00000000
			0			Reserved		
22	0x16	Slave Alias[6]	[7:1]	RW	Slave Device Alias 6	7-bit Remote Slave Alias 6 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID[6], the transaction will be re-mapped to the ID address before passing the transaction across the Bidirectional Control Channel to the Serializer.	0x00	00000000
			0			Reserved		
23	0x17	Slave Alias[7]	[7:1]	RW	Slave Device Alias 7	7-bit Remote Slave Alias 7 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID[7], the transaction will be re-mapped to the ID address before passing the transaction across the Bidirectional Control Channel to the Serializer.	0x00	00000000
			0			Reserved		
24	0x18	Mailbox[0]	[7:0]	RW	Mailbox Register 0	Mailbox Register 0 This register may be used to temporarily store temporary data, such as status or multi-master arbitration	0x00	00000000
25	0x19	Mailbox[1]	[7:0]	RW	Mailbox Register 1	Mailbox Register 1 This register may be used to temporarily store temporary data, such as status or multi-master arbitration	0x01	00000001
27	0x1B	Frequency Counter	[7:0]	RW	Frequency Count	Frequency Counter control A write to this register will enable a frequency counter to count the number of pixel clock during a specified time interval. The time interval is equal to the value written multiplied by the oscillator clock period (nominally 50 ns). A read of the register returns the number of pixel clock edges seen during the enabled interval. The frequency counter will saturate at 0xff if it reaches the maximum value. The frequency counter will provide a rough estimate of the pixel clock period. If the pixel clock frequency is known, the frequency counter may be used to determine the actual oscillator clock frequency.	0x00	00000000
28	0x1C	General Status	[7:4]			Reserved	0x00	00000000
			3	R	I2S Locked	I2S Lock Status **0: I2S PLL controller not locked (default)** 1: I2S PLL controller locked to input I2S clock		
			2	R	CRC Error	CRC Error Detected **0: No CRC errors detected** 1: CRC errors detected		
			1			Reserved		
			0	R	LOCK	Deserializer CDR and PLL Locked to recovered clock frequency **0: Deserializer not Locked (default)** 1: Deserializer Locked to recovered clock		
			[7:4]	R	Revision ID	Device Revision ID: 0010: Production Device		
			3	RW	GPIO0 Output Value	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled		

					Value	is disabled. 0: Output LOW (default) **1: Output HIGH**		
29	0x1D	GPIO0 Configuration	2	RW	GPIO0 Remote Enable	Remote GPIO Control **0: Disable GPIO control from remote device (default)** 1: Enable GPIO control from remote device. The GPIO pin will be an output, and the value is received from the remote device.	0x2B	00101011
			1	RW	GPIO0 Direction	Local GPIO Direction 0: Output (default) **1: Input**		
			0	RW	GPIO0 Enable	GPIO Function Enable 0: Enable normal operation (default) **1: Enable GPIO operation**		
30	0x1E	GPIO1 and GPIO2 Configuration	7	RW	GPIO2 Output Value	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled. **0: Output LOW (default)** 1: Output HIGH	0x5B	01011011
			6	RW	GPIO2 Remote Enable	Remote GPIO Control 0: Disable GPIO control from remote device (default) **1: Enable GPIO control from remote device. The GPIO pin will be an output, and the value is received from the remote device.**		
			5	RW	GPIO2 Direction	Local GPIO Direction **0: Output (default)** 1: Input		
			4	RW	GPIO2 Enable	GPIO Function Enable 0: Enable normal operation (default) **1: Enable GPIO operation**		
			3	RW	GPIO1 Output Value	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled. 0: Output LOW (default) **1: Output HIGH**		
			2	RW	GPIO1 Remote Enable	Remote GPIO Control **0: Disable GPIO control from remote device (default)** 1: Enable GPIO control from remote device. The GPIO pin will be an output, and the value is received from the remote device.		
			1	RW	GPIO1 Direction	Local GPIO Direction 0: Output (default) **1: Input**		
			0	RW	GPIO1 Enable	GPIO Function Enable 0: Enable normal operation (default) **1: Enable GPIO operation**		
31	0x1F	GPIO3 Configuration	[7:4]			Reserved	0x0D	00001101
			3	RW	GPIO3 Output Value	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled. 0: Output LOW (default) **1: Output HIGH**		
			2	RW	GPIO3 Remote Enable	Remote GPIO Control 0: Disable GPIO control from remote device (default) **1: Enable GPIO control from remote device. The GPIO pin will be an output, and the value is received from the remote device.**		
			1	RW	GPIO3 Direction	Local GPIO Direction **0: Output (default)** 1: Input		
			0	RW	GPIO3 Enable	GPIO Function Enable 0: Enable normal operation (default) **1: Enable GPIO operation**		
			7	RW	GPIO_REG6 Output Value	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, and the local GPIO direction is Output. **0: Output LOW (default)** 1: Output HIGH		
			6			Reserved		
			5	RW	GPIO_REG6 Direction	Local GPIO Direction **0: Output (default)** 1: Input		
					GPIO_REG6	GPIO Function Enable		

32	0x20	GPIO_REG5 and GPIO_REG6 Configuration	4	RW	GPIO_REG6 Enable	0: Enable normal operation (default) **1: Enable GPIO operation**	0x1B	00011011
			3	RW	GPIO_REG5 Output Value	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, and the local GPIO direction is Output. 0: Output LOW (default) **1: Output HIGH**		
			2			Reserved		
			1	RW	GPIO_REG5 Direction	Local GPIO Direction 0: Output (default) **1: Input**		
			0	RW	GPIO_REG5 Enable	GPIO Function Enable 0: Enable normal operation (default) **1: Enable GPIO operation**		
33	0x21	GPIO_REG7 and GPIO_REG8 Configuration	7	RW	GPIO_REG8 Output Value	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, and the local GPIO direction is Output. 0: Output LOW (default) **1: Output HIGH**	0x91	10010001
			6			Reserved		
			5	RW	GPIO_REG8 Direction	Local GPIO Direction **0: Output (default)** 1: Input		
			4	RW	GPIO_REG8 Enable	GPIO Function Enable 0: Enable normal operation (default) **1: Enable GPIO operation**		
			3	RW	GPIO_REG7 Output Value	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, and the local GPIO direction is Output. **0: Output LOW (default)** 1: Output HIGH		
			2			Reserved		
			1	RW	GPIO_REG7 Direction	Local GPIO Direction **0: Output (default)** 1: Input		
			0	RW	GPO_REG7 Enable	GPIO Function Enable 0: Enable normal operation (default) **1: Enable GPIO operation**		
34	0x22	Data Path Control	7	RW	Override FC Configuration	Override Configuration Loaded by Forward Channel 0: Allow forward channel loading of this register (default) **1: Disable loading of this register from the forward channel, keeping locally written values intact** Bits [6:0] are RW if this bit is set	0x00	00000000
			6			Reserved		
			5	RW	DE Polarity	This bit indicates the polarity of the DE (Data Enable) signal. **0: DE is positive (active high, idle low) (default)** 1: DE is inverted (active low, idle high)		
			4	RW	I2S Repeater Regen	Regenerate I2S Data From Repeater I2S Pins **0: Output packetized audio on RGB video output pins. (default)** 1: Repeater regenerates I2S from I2S pins		
			3	RW	I2S Channel B Enable Override	I2S Channel B Override **0: Set I2S Channel B Disabled (default)** 1: Set I2S Channel B Enable from register		
			2	RW	18-bit Video Select	Video Color Depth Mode **0: Select 24-bit video mode (default)** 1: Select 18-bit video mode		
			1	RW	I2S Transport Select	Select I2S Transport Mode **0: Enable I2S Data Island Transport (default)** 1: Enable I2S Data Forward Channel Frame Transport		
			0	RW	I2S Channel B Enable	I2S Channel B Enable **0: I2S Channel B disabled (default)** 1: Enable I2S Channel B		
			7			Reserved		
			[6:4]			Reserved		
			3	R	LFMODE Status	Low Frequency Mode (LFMODE) pin status **0: 15 MHz ≤ TxCLKOUT ≤ 85 MHz (default)**		

						1: 5 MHz ≤ TxCLKOUT < 15 MHz		
35	0x23	Rx Mode Status	2	R	REPEAT Status	Repeater Mode (REPEAT) pin Status **0: Non-repeater (default)** 1: Repeater	0x10	00010000
			1	R	BKWD Status	Backward Compatible Mode (BKWD) Status **0: Compatible to DS90UB925Q-Q1/DS90UB927Q-Q1 (default)** 1: Backward compatible to DS90UR905/7Q		
			0	R	I2S Channel B Status	I2S Channel B Mode (I2S_DB) Status **0: I2S_DB inactive (default)** 1: I2S_DB active		
36	0x24	BIST Control	[7:4]			Reserved	0x08	00001000
			3	RW	BIST Pin Config	BIST Pin Configuration 0: BIST enabled from register **1: BIST enabled from pin (default)**		
			[2:1]	RW	OSC Clock Source	Internal OSC clock select for Functional Mode or BIST. Functional Mode when PCLK is not present and 0x03[1]=1. **00: 33 MHz Oscillator (default)** 01: 33 MHz Oscillator Note: In LFMODE=1, the internal oscillator is 12.5 MHz		
			0	RW	BIST Enable	BIST Control **0: Disabled (default)** 1: Enabled		
37	0x25	BIST Error	[7:0]	R	BIST Error Count	Errors Detected During BIST Records the number (up to 255) of forward-channel errors detected during BIST. The value stored in this register is only valid after BIST terminates (BISTEN = 0). Resets on PDB = 0 or start of another BIST (BISTEN = 1).	0x00	00000000
38	0x26	SCL High Time	[7:0]	RW	SCL High Time	I2C Master SCL High Time This field configures the high pulse width of the SCL output when the deserializer is the Master on the local I2C bus. Units are 50 ns for the nominal oscillator clock frequency.	0x83	10000011
39	0x27	SCL Low Time	[7:0]	RW	SCL Low Time	I2C SCL Low Time This field configures the low pulse width of the SCL output when the deserializer is the Master on the local I2C bus. This value is also used as the SDA setup time by the I2C Slave for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 50 ns for the nominal oscillator clock frequency.	0x84	10000100
40	0x28	Data Path Control 2	7	RW	Block I2S Auto Config	Override Forward Channel Configuration 0: Enable forward-channel loading of this register **1: Disable loading of this register from the forward channel, keeping local values intact**	0x84	10000100
			[6:4]			Reserved		
			3	RW	Aux I2S Enable	Auxiliary I2S Channel Enable **0: Normal GPIO[1:0] operation** 1: Enable Aux I2S channel on GPIO1 (AUX word select) and GPIO0 (AUX data)		
			2	RW	I2S Disable	Disable All I2S Outputs 0: I2S Outputs Enabled (default) **1: I2S Outputs Disabled**		
			1			Reserved		
			0	RW	I2S Surround	Enable 5.1- or 7.1-channel I2S audio transport **0: 2-channel or 4-channel I2S audio is enabled as configured in register or MODE_SEL (default)** 1: 5.1- or 7.1-channel audio is enabled Note that I2S Data Island Transport is the only option for surround audio. Also note that in a repeater, this bit may be overridden by the in-band I2S mode detection.		
			7	RW	Timing Mode Select	Select Display Timing Mode **0: DE only Mode (default)** 1: Sync Mode (VS,HS)		
			6	RW	HS Polarity	Horizontal Sync Polarity Select **0: Active High (default)** 1: Active Low		
			5	RW	VS Polarity	Vertical Sync Polarity Select **0: Active High (default)**		

						1: Active Low		
41	0x29	FRC Control	4	RW	DE Polarity	Data Enable Sync Polarity Select **0: Active High (default)** 1: Active Low	0x00	00000000
			3	RW	FRC2 Enable	FRC2 Enable **0: FRC2 disable (default)** 1: FRC2 enable		
			2	RW	FRC1 Enable	FRC1 Enable **0: FRC1 disable (default)** 1: FRC1 enable		
			1	RW	Hi-FRC2 Enable	Hi-FRC2 Enable **0: Hi-FRC2 enable (default)** 1: Hi-FRC2 disable		
			0	RW	Hi-FRC1 Enable	Hi-FRC1 Enable **0: Hi-FRC1 enable (default)** 1: Hi-FRC1 disable		
42	0x2A	White Balance Control	[7:6]	RW	Page Setting	Control/LUT Setting Page Select **00: Configuration Registers (default)** 01: Red LUT 10: Green LUT 11: Blue LUT	0x00	00000000
			5	RW	White Balance Enable	White Balance Enable **0: White Balance Disabled (default)** 1: White Balance Enabled		
			4	RW	LUT Reload Enable	Enable LUT Reload **0: Reload Disable (default)** 1: Reload Enable		
			[3:0]			Reserved		
43	0x2B	I2S Control	7	RW	I2S PLL Override	Override I2S PLL **0: PLL override disabled (default)** 1: PLL override enabled	0x00	00000000
			6	RW	I2S PLL Enable	Enable I2S PLL **0: I2S PLL is on for I2S data jitter cleaning (default)** 1: I2S PLL is off. No jitter cleaning		
			[5:1]			Reserved		
			0	RW	I2S Clock Edge	I2S Clock Edge Select **0: I2S Data is strobed on the Falling Clock Edge(default)** 1: I2S Data is strobed on the Rising Clock Edge		
53	0x35	AEQ Control	7			Reserved	0x00	00000000
			6	RW	AEQ Restart	Restart AEQ adaptation from initial (Floor) values **0: Normal operation (default)** 1: Restart AEQ adaptation Note: This bit is not self-clearing. It must be set, then reset.		
			5	RW	LCBL Override	Override LCBL Mode Set by MODE_SEL **0: LCBL controlled by MODE_SEL pin** 1: LCBL controlled by register		
			4	RW	LCBL	Set LCBL Mode **0: LCBL Mode disabled** 1: LCBL Mode enabled. AEQ Floor value is controlled from Adaptive EQ MIN/MAX register		
			[3:0]			Reserved		
57	0x39	PG Internal Clock Enable	[7:2]			Reserved	0x10	00000010
			1	RW	PG INT CLK	Enable Pattern Generator Internal Clock This bit must be set to use the Pattern Generator Internal Clock Generation 0: Pattern Generator with external PCLK **1: Pattern Generator with internal PCLK** See TI Application Note ( ) for details		
			0			Reserved		
58	0x3A	I2S DIVSEL	7	RW	MCLK Div Override	Override MCLK Divider Setting **0: No override for MCLK divider (default)** 1: Override divider select for MCLK	0x00	00000000
			[6:4]	RW	MCLK Div	See Table 4		
			[3:0]			Reserved		
59	0x3B	Adaptive EQ Status	[7:6]			Reserved	0x00	00000000
			[5:0]		EQ Status	Equalizer Status Current equalizer level set by AEQ or Override Register		
65	0x41	Link Error Count	[7:5]			Reserved	0x03	00000011
			4	RW	Link Error Count Enable	Enable serial link data integrity error count 1: Enable error count **0: Disable**		
			[3:0]	RW	Link Error Count Threshold	Link error count threshold. Counter is pixel clock based. CLK0, CLK1, and DCA are monitored for link errors, if error count is enabled Deserializer loose lock once error count reaches threshold if disabled Deserializer loose lock with one error.		

68	0x44	Adaptive Equalizer Bypass	[7:5]	RW	EQ Stage 1 Select Value	EQ Stage 1 select value. Used if adaptive EQ is bypassed. Used if adaptive EQ is bypassed.	0x60	01100000
			4			Reserved		
			[3:1]	RW	EQ Stage 2 Select Value	EQ Stage 2 select value. Used if adaptive EQ is bypassed Used if adaptive EQ is bypassed.		
			0	RW	Adaptive EQ Bypass	Bypass Adaptive EQ Overrides Adaptive EQ search and sets the EQ to the static value configured in this register **0: Enable adaptive EQ (default)** 1: Disable adaptive EQ (to write EQ select values)		
69	0x45	Adaptive EQ MIN/MAX	[7:4]	RW		Reserved	0x88	10001000
			[3:0]	RW	Adaptive EQ Bypass	Adaptive Equalizer Floor Value Sets the AEQ floor value when Long Cable Mode (LCBL) is enabled by register or MODE_SEL		
73	0x49	Map Select	7	R	MAPSEL Pin Status	Returns Status of MAPSEL pin	0x00	00000000
			6	RW	MAPSEL Override	Map Select (MAPSEL) Setting Override **0: MAPSEL set from pin** 1: MAPSEL set from register		
			5	RW	MAPSEL	Map Select (MAPSEL) Setting **0: LSBs on TxOUT3±** 1: MSBs on TxOUT3±		
			[4:0]			Reserved		
75	0x4B	LVDS Setting	[7:2]			Reserved	0x08	00001000
			[1:0]	RW	LVDS VOD Control	**00: 400 mV differential (default)** 01: 600 mV differential		
86	0x56	Loop-Through Driver	[7:4]			Reserved	0x08	00001000
			3	RW	Loop-Through Driver Enable	Enable CML Loop-Through Driver (CMLOUTP/CMLOUTN) 0: Enable **1: Disable (default)**		
			[2:0]			Reserved		
100	0x64	Pattern Generator Control	[7:4]	RW	Pattern Generator Select	Fixed Pattern Select Selects the pattern to output when in Fixed Pattern Mode. Scaled patterns are evenly distributed across the horizontal or vertical active regions. This field is ignored when Auto-Scrolling Mode is enabled. xxxx: normal/inverted 0000: Checkerboard 0001: White/Black (default) 0010: Black/White 0011: Red/Cyan 0100: Green/Magenta 0101: Blue/Yellow 0110: Horizontal Black-White/White-Black 0111: Horizontal Black-Red/White-Cyan 1000: Horizontal Black-Green/White-Magenta 1001: Horizontal Black-Blue/White-Yellow 1010: Vertical Black-White/White— Black 1011: Vertically Scaled Black to Red/White to Cyan 1100: Vertical Black-Green/White-Magenta 1101: Vertical Black-Blue/White-Yellow **1110: Custom color (or its inversion) configured in PGRS, PGGS, PGBS registers** 1111: VCOM See TI App Note AN-2198 ().	0xE1	11100001
			3			***Reserved***		
			2	RW	Color Bars Pattern	Enable Color Bars Pattern **0: Color Bars disabled (default)** 1: Color Bars enabled Overrides the selection from bits [7:4]		
			1	RW	VCOM Pattern Reverse	Reverse order of color bands in VCOM pattern **0: Color sequence from top left is (YCBR) (default)** 1: Color sequence from top left is (RBCY)		
			0	RW	Pattern Generator Enable	Pattern Generator Enable 0: Disable Pattern Generator (default) **1: Enable Pattern Generator** See TI App Note AN-2198 ().		
			7			Reserved		
			6	RW	Checkerboard Scale	Scale Checkerboard Patterns: **0: Normal operation (each square is 1x1 pixel) (default)** 1: Scale checkered patterns (VCOM and checkerboard) by 8 (each square is 8x8 pixels) Setting this bit gives better visibility of the checkered patterns.		
			5	RW	Custom Checkerboa	Use Custom Checkerboard Color **0: Use white and black in the Checkerboard pattern(default)**		

					rd	1: Use the Custom Color and black in the Checkerboard pattern		
101	0x65	Pattern Generator Configuration	4	RW	PG 18–bit Mode	18-bit Mode Select: **0: Enable 24-bit pattern generation. Scaled patterns use 256 levels of brightness. (default)** 1: Enable 18-bit color pattern generation. Scaled patterns will have 64 levels of brightness and the R, G, and B outputs use the six most significant color bits.	0x00	00000000
			3	RW	External Clock	Select External Clock Source: 0: Selects the internal divided clock when using internal timing (default) 1: Selects the external pixel clock when using internal timing. This bit has no effect in external timing mode (PATGEN_TSEL = 0).		
			2	RW	Timing Select	Timing Select Control: **0: the Pattern Generator uses external video timing from the pixel clock, Data Enable, Horizontal Sync, and Vertical Sync signals. (default)** 1: The Pattern Generator creates its own video timing as configured in the Pattern Generator Total Frame Size, Active Frame Size. Horizontal Sync Width, Vertical Sync Width, Horizontal Back Porch, Vertical Back Porch, and Sync Configuration registers		
			1	RW	Color Invert	Enable Inverted Color Patterns: 0: Do not invert the color output. (default) 1: Invert the color output.		
			0	RW	Auto Scroll	Auto Scroll Enable: 0: The Pattern Generator retains the current pattern. (default) 1: The Pattern Generator will automatically move to the next enabled pattern after the number of frames specified in the Pattern Generator Frame Time (PGFT) register. See TI App Note AN-2198 ().		
102	0x66	PGIA	[7:0]	RW	PG Indirect Address	This 8-bit field sets the indirect address for accesses to indirectly-mapped registers. It should be written prior to reading or writing the Pattern Generator Indirect Data register. See TI App Note AN-2198 ().	0x00	00000000
103	0x67	PGID	[7:0]	RW	PG Indirect Data	When writing to indirect registers, this register contains the data to be written. When reading from indirect registers, this register contains the read back value. See TI App Note AN-2198 ().	0x00	00000000
110	0x6E	GPI Pin Status 1	7	R	GPI7 Pin Status	GPI7 Pin Status. Readable when REG_GPIO7 is set as an input.	0x00	00000000
			6	R	GPI6 Pin Status	GPI6 Pin Status. Readable when REG_GPIO6 is set as an input.		
			5	R	GPI5 Pin Status	GPI5 Pin Status. Readable when REG_GPIO5 is set as an input.		
			4			Reserved		
			3	R	GPI3 Pin Status	GPI3 Pin Status. Readable when GPIO3 is set as an input.		
			2	R	GPI2 Pin Status	GPI2 Pin Status. Readable when GPIO2 is set as an input.		
			1	R	GPI1 Pin Status	GPI1 Pin Status. Readable when GPIO1 is set as an input.		
			0	R	GPI0 Pin Status	GPI0 Pin Status. Readable when GPIO0 is set as an input.		
111	0x6F	GPI Pin Status 2	[7:1]			Reserved	0x00	00000000
			0	R	GPI8 Pin Status	GPI8 Pin Status. Readable when REG_GPIO8 is set as an input.		
240	0xF0	RX ID	[7:0]	R	ID0	First byte ID code, ‘_’	0x5F	01011111
241	0xF1		[7:0]	R	ID1	Second byte of ID code, ‘U’	0x55	01010101
242	0xF2		[7:0]	R	ID2	Third byte of ID code. 'B'	0x42	01000010
243	0xF3		[7:0]	R	ID3	Forth byte of ID code: ‘9’	0x39	00111001
244	0xF4		[7:0]	R	ID4	Fifth byte of ID code: “2”	0x32	00110010
245	0xF5		[7:0]	R	ID5	Sixth byte of ID code: “8”	0x38	00111000