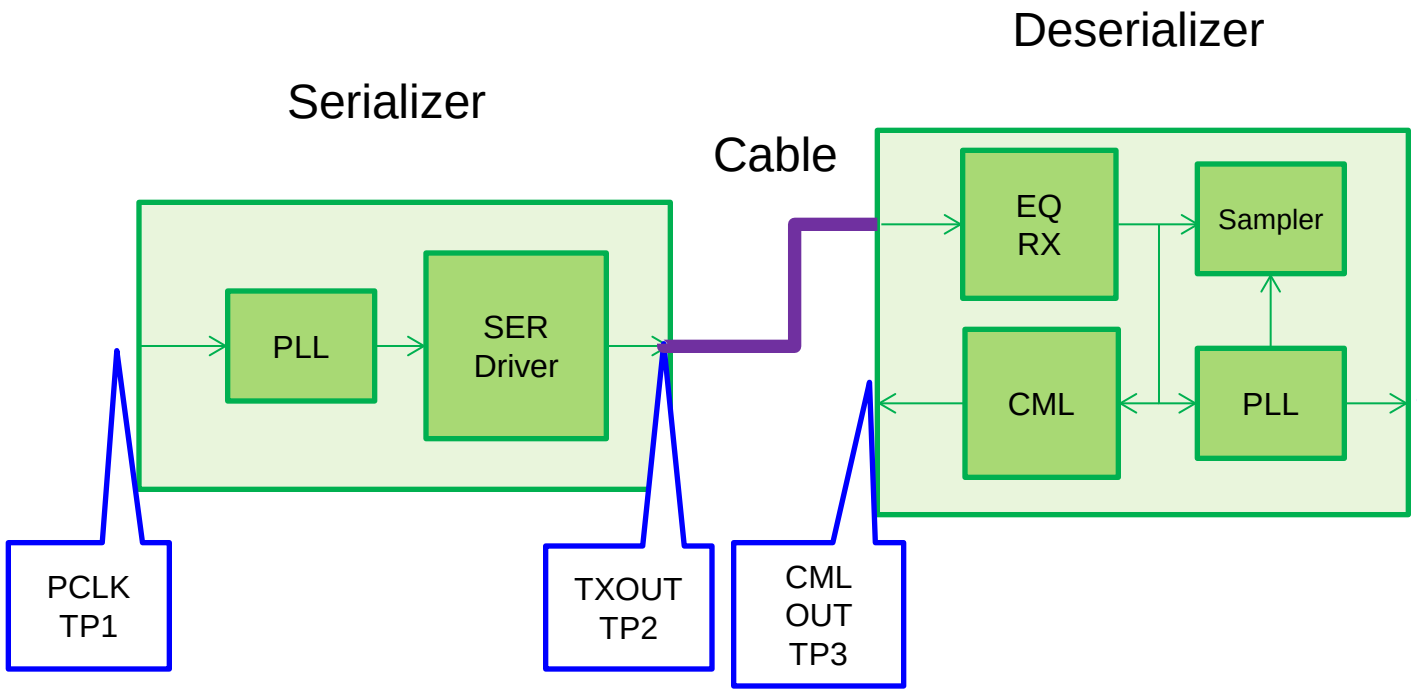
Jitter Measurement Method

September 2016

Rev. 6

Quick Overview



TP1: t_{IJIT} (PCLK input jitter)

Input jitter measurement on PCLK, t_{IJIT}, is measured under the following conditions:

a) Use TJ@BER with Target BER = 10 (BER = 1E - 10)

b) Set Clock Recover using Custom PLL with loop BW at f/15, where f is the PCLK frequency and damping of 2

c) Set Low Pass @ f/20, where f is the PCLK frequency.

UI:

92x

* ***1UI = 1 / (PCLK*35) and refers to the high speed serial stream.***

913A/914A

* ***12bLF: 1UI = 1 / (PCLK*28) and refers to the high speed serial stream.***
* ***12bHF: 1UI = 1 / (PCLK*28*2/3) and refers to the high speed serial stream.***
* ***10bHF: 1UI = 1 / (PCLK*28*1/2) and refers to the high speed serial stream.***

TP2: t_{TJIT} (TXOUT Total Jitter)

On the high speed serial stream output DOUT-, DOUT+, measure under the following conditions:

a) Configure device in serial test pattern mode : Set register 2C = 60h
b) Set Clock recover using custom PLL with Loop BW at f/15, where f is the PCLK frequency
c) Use TJ@BER with Target BER = 10 (BER = 1E - 10)
d) Configure to measure DDJ@BER

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TP3: Ew (CMLOUT Eye Opening)

CMLOUT Eye Opening can be defined by t_{BIT} (1UI) – TJ@BER:

a) Enable CMLOUT: Set Register 0x3F[4] = 0'b
b) Set Clock recover using custom PLL with Loop BW at f/15, where f is the PCLK frequency
c) Use TJ@BER with Target BER = 10 (BER = 1E - 10)

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DPOJET Jitter Measurement

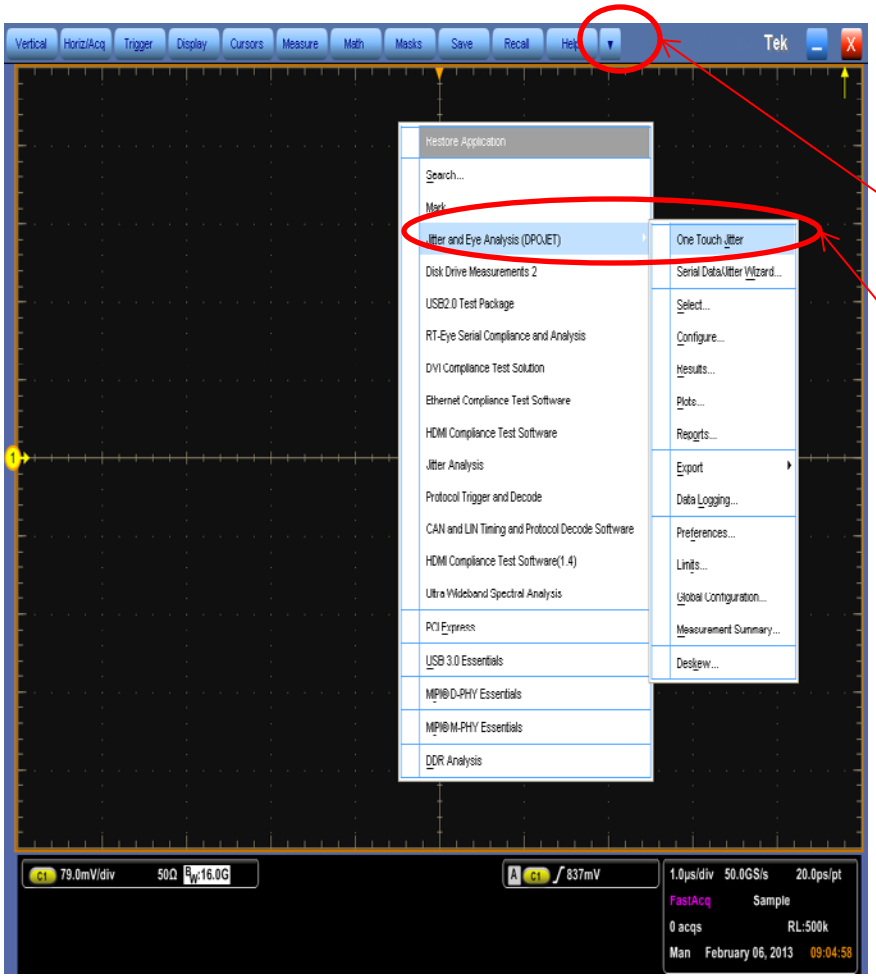
Jitter Measurement Guidance

- These guidelines are based on the use of DPOJET
- Goal is to provide guidance to configure the DPOJET settings recommended for measurement of the DS90UH925 input and output jitter
- The images show are for the purpose of illustrating the DPOJET tool configuration process. This is not meant to reflect actual or expected application or device measurements.

LOCK?

- Check LOCK status before starting jitter measurement.
- How?
  - LOCK pin LED
  - LOCK @ General Status Register

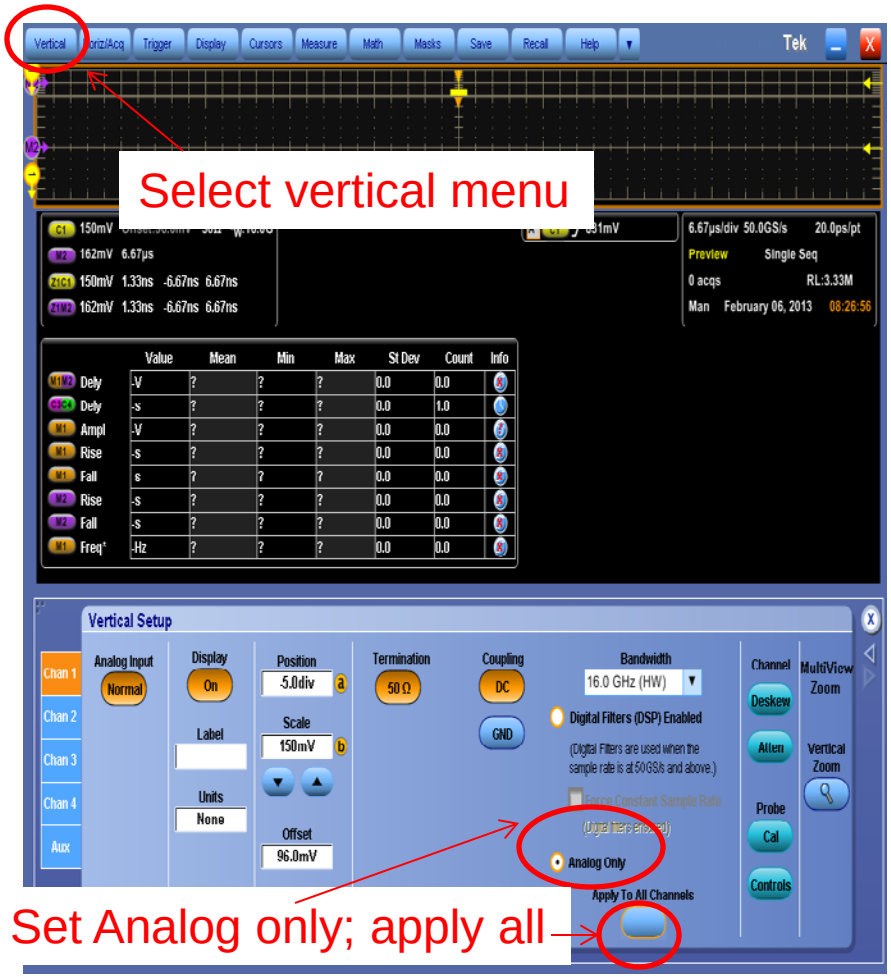
Enable Tool



Select drop-down menu

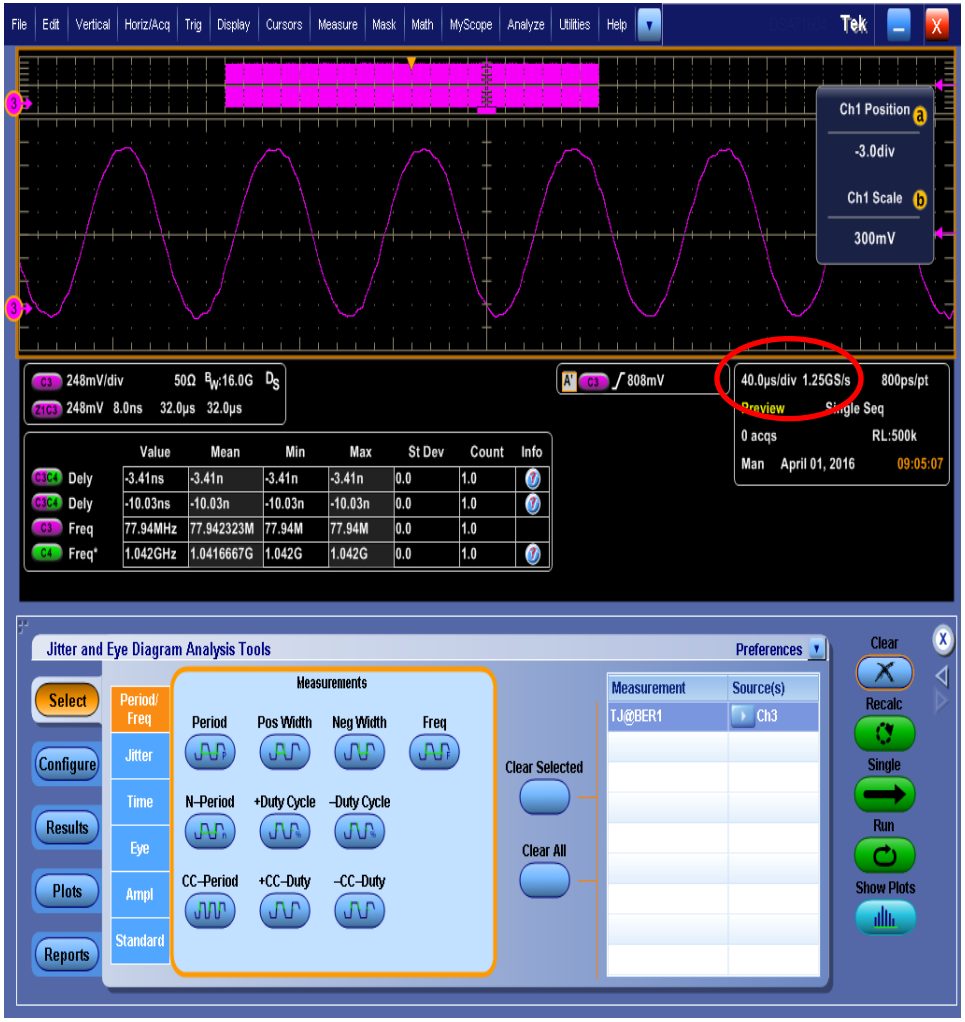
Choose DPOJET & One Touch Jitter

Select “Analog Measurement”

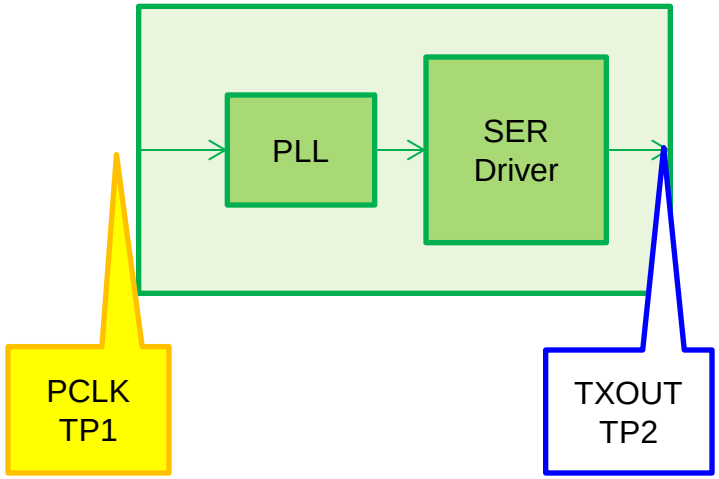


Manually select the analog measurement mode to avoid errors. (This may be set incorrectly with default settings)

Proper Set Scale



Using horizontal scale and resolution knob to set 40uS/div



TP1: T_{IJIT} (PCLK INPUT JITTER)

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Input jitter measurement on PCLK, t_{IJIT}, is measured under the following conditions:

a) Use TJ@BER with Target BER = 10 (BER = 1E - 10)

b) Set Clock Recover using Custom PLL with loop BW at f/15, where f is the PCLK frequency and damping of 2

c) Set Low Pass @ f/20, where f is the PCLK frequency.

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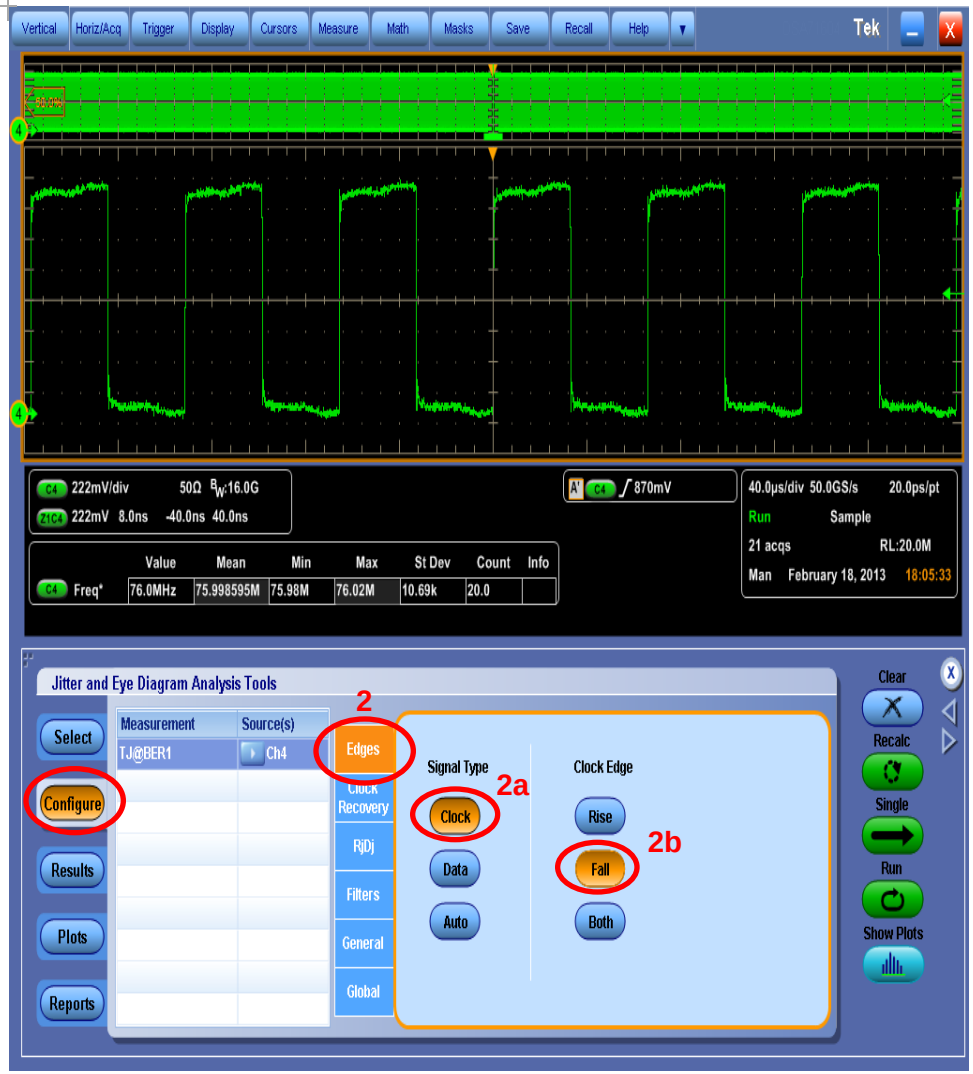
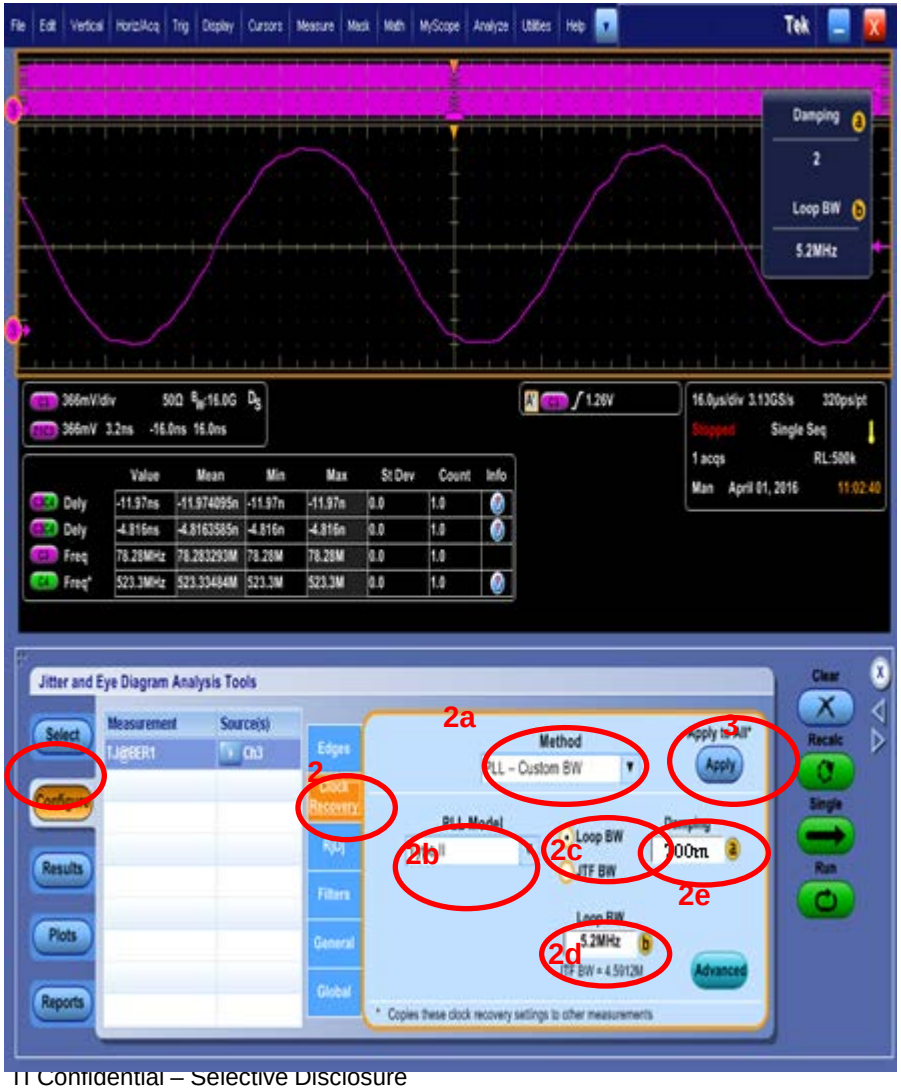
PCLK Input Jitter Configure Edge



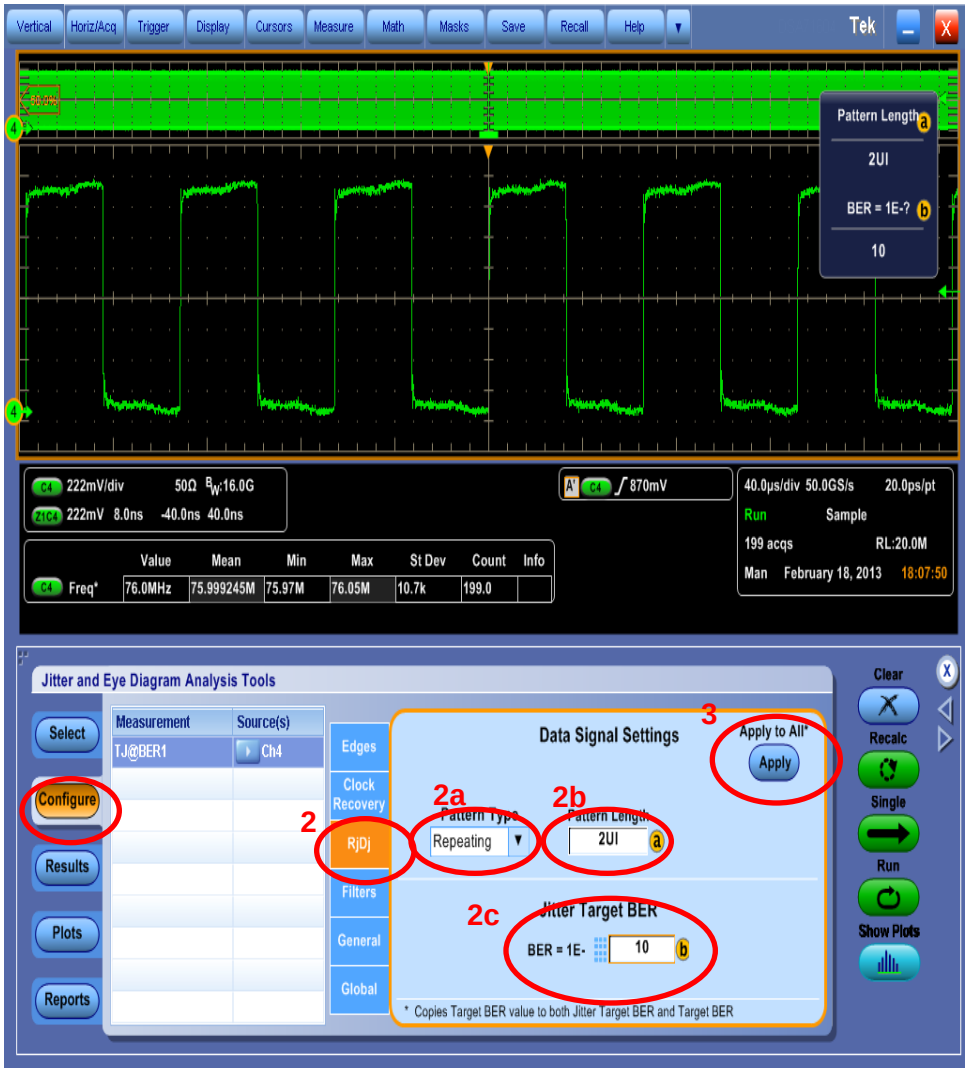
1. Go to **Configure** menu
2. Select **Edges**
    a. Signal Type = **Clock**
    b. Clock Edge = **Fall (if using rising edge, change to Rise)**

PCLK Input Jitter
Configure Clock Recover



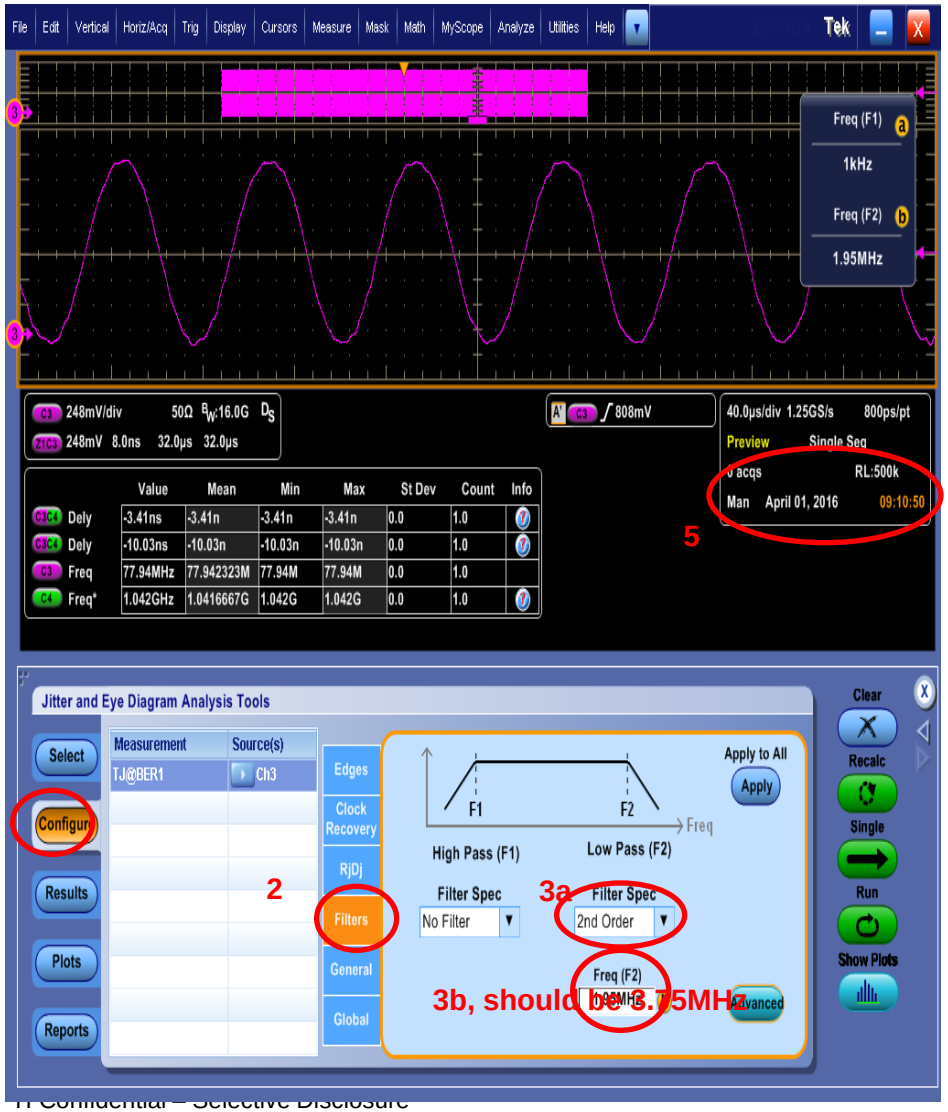
1. Go to **Configure** menu
2. Select **Clock Recover**
   - 2a. Method = **PLL Custom BW**
   - 2b. PLL Type = **Type II**
   - 2c. Chose **Loop BW**
   - 2d. Loop BW = **f/15**
     - for exaple, pclk=78MHz
       - f/15 = 5.2MHz
   - 2e. Damping = **2**
3. **Apply to All**

PCLK Input Jitter Configure RjDj



1. Go to **Configure** menu
2. Select **RjDj**
   a. Pattern = **Repeating**
   b. Window Length = **2**UI
   c. Jitter Target BER = 1E-**10**
3. **Apply to All**

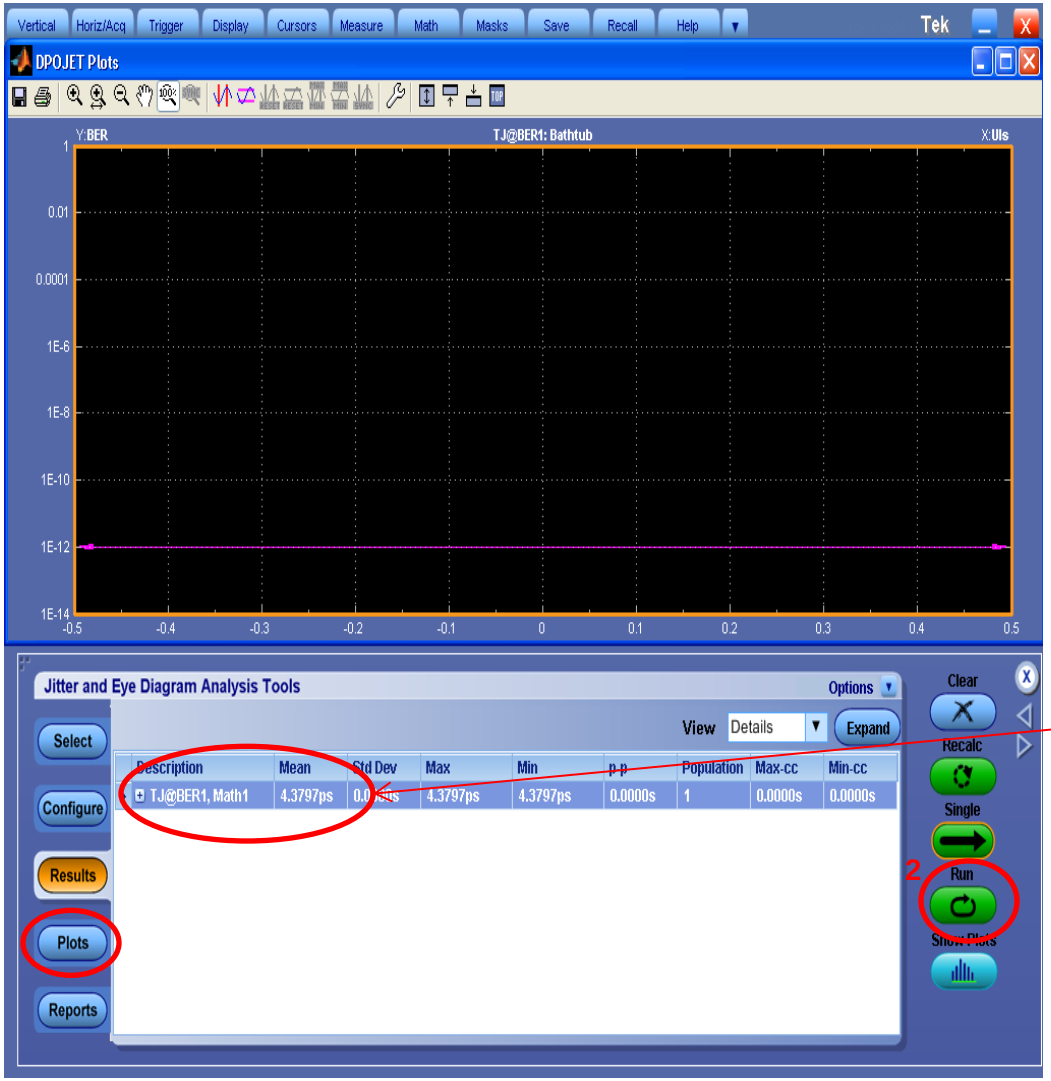
PCLK Input Jitter Configure Filter



1. Go to **Configure** menu
2. Select **Filters**
3. Configure the Low Pass filter to f/20
   a. Use drop-down Low Pass (F2) Filter Spec to select "**2rd Order**"
   b. Set Freq (F2) to **f/20**
      Example: PCLK = 75MHz
      f/20= 3.75MHz

4. Apply to All

PCLK Input Jitter Results

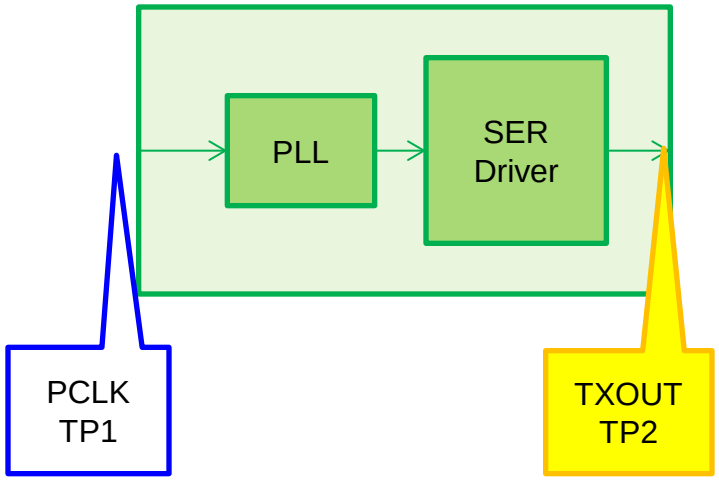


1. Go to **Results**

2, Click “**Single**” to capture measurement

3, click on “**Run**” to get distribution of jitter

Measurement results will be reported in this format



TP2: TX OUTPUT JITTER

TP2: t_{TJIT} (TXOUT Total Jitter)

On the high speed serial stream output DOUT-, DOUT+, measure under the following conditions:

a) Configure device in serial test pattern mode : Set register 2C = 60h
b) Set Clock recover using custom PLL with Loop BW at f/15, where f is the PCLK frequency
c) Use TJ@BER with Target BER = 10 (BER = 1E - 10)
d) Configure to measure DDJ@BER

UI:

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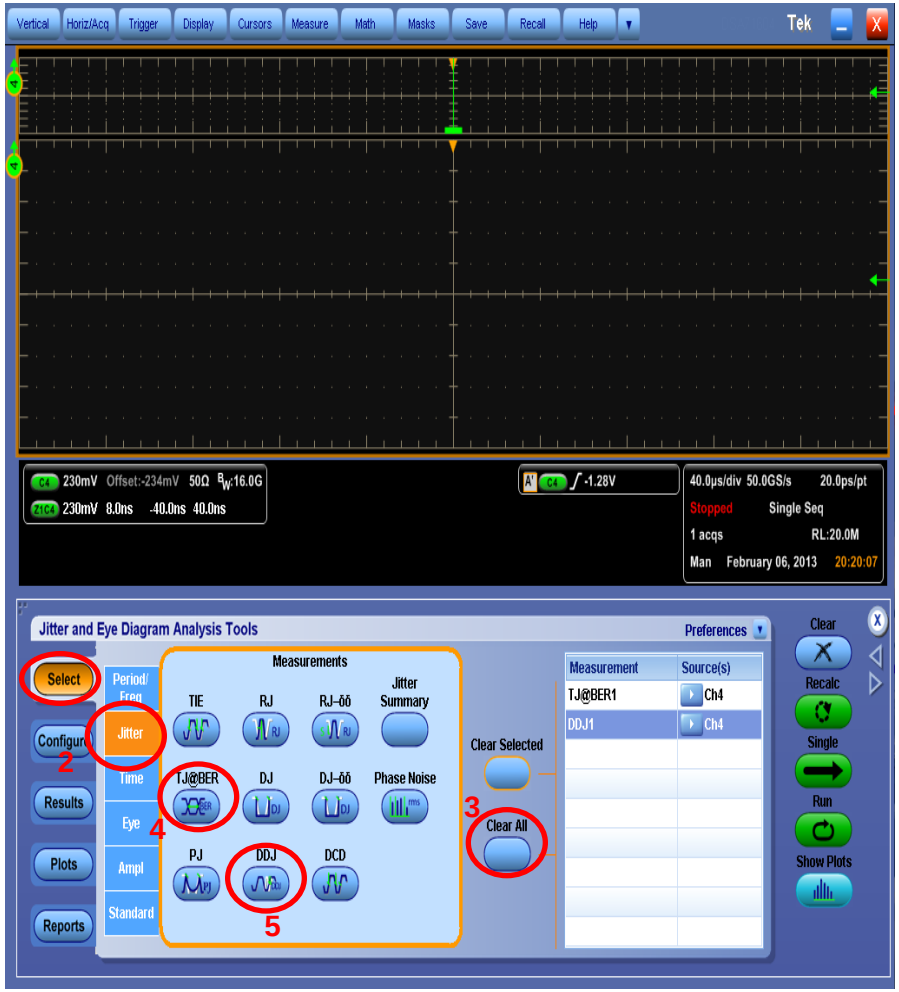
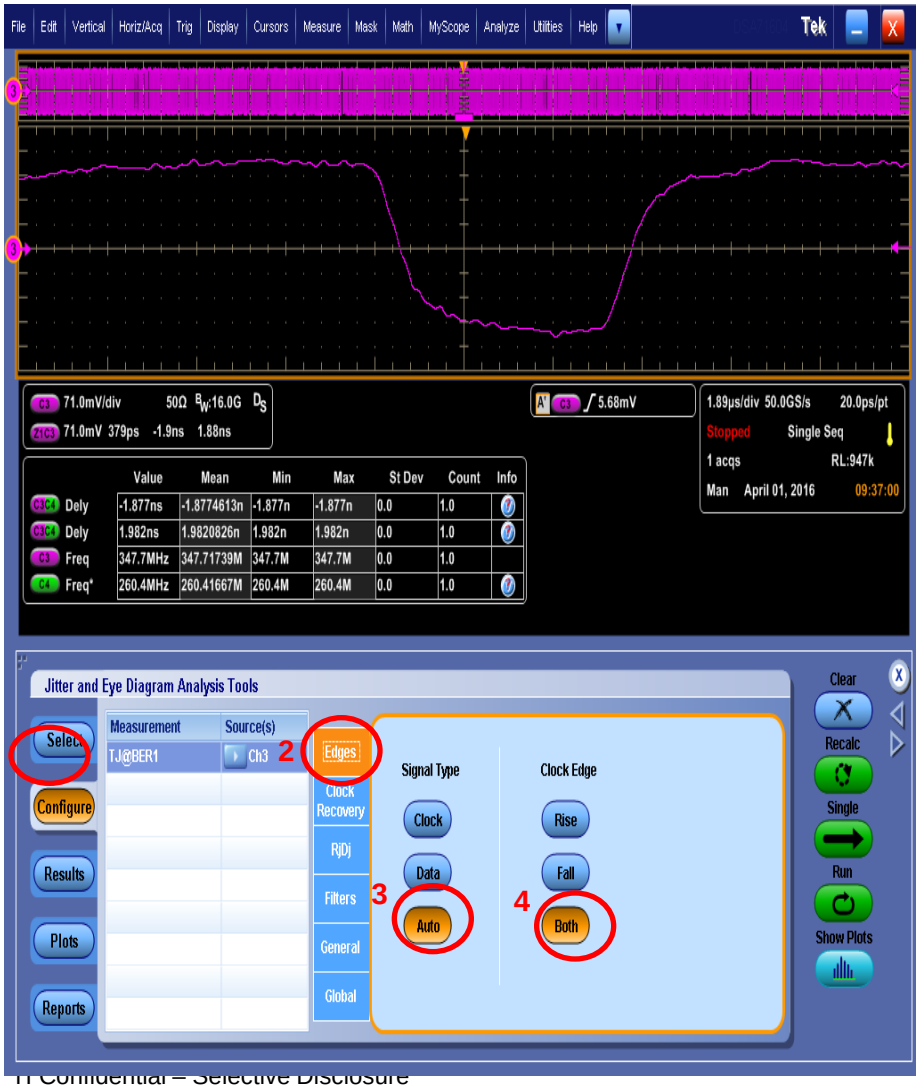
Tx Output Jitter
Select Jitter Measurement



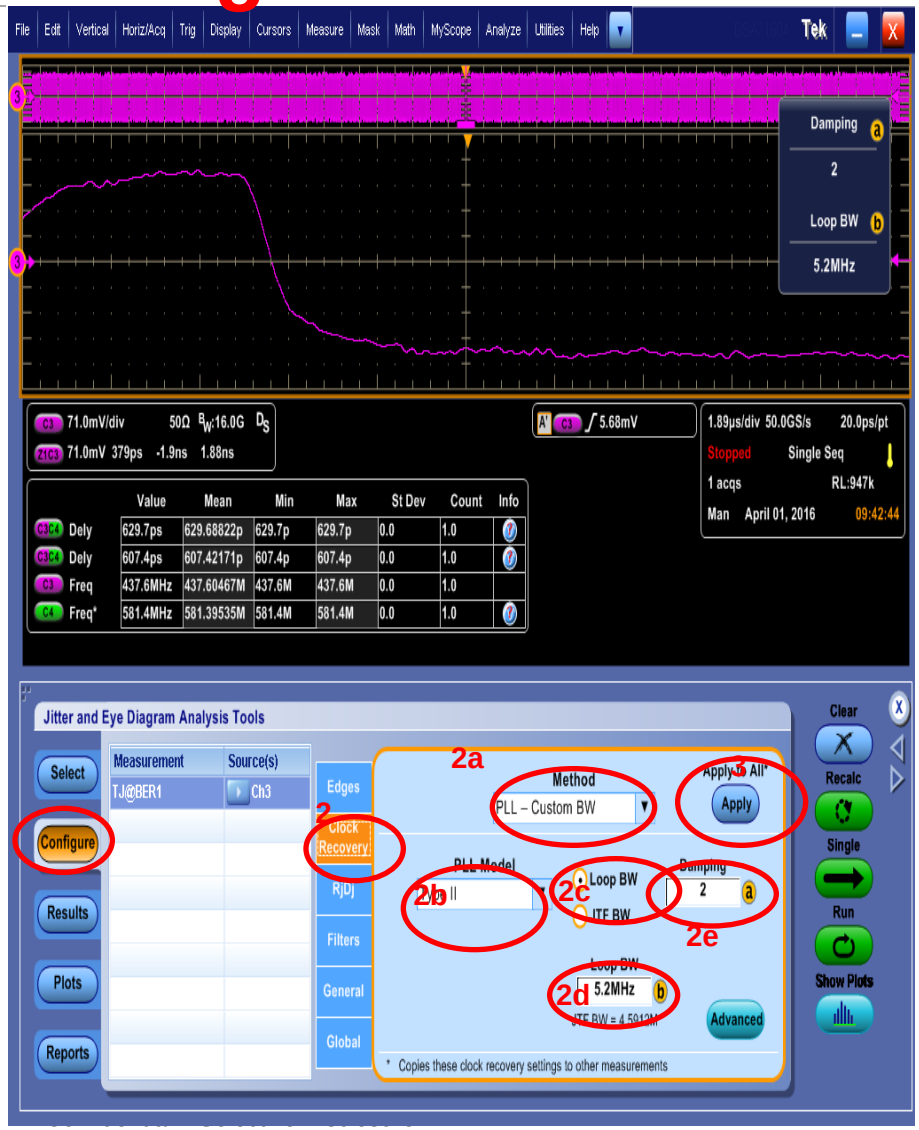
1. Go to jitter **Select** menu
2. Select **Jitter**
3. **Clear All**
4. Select **TJ@BER**
5. Select **DDJ**

Tx Output Jitter Configure Edges



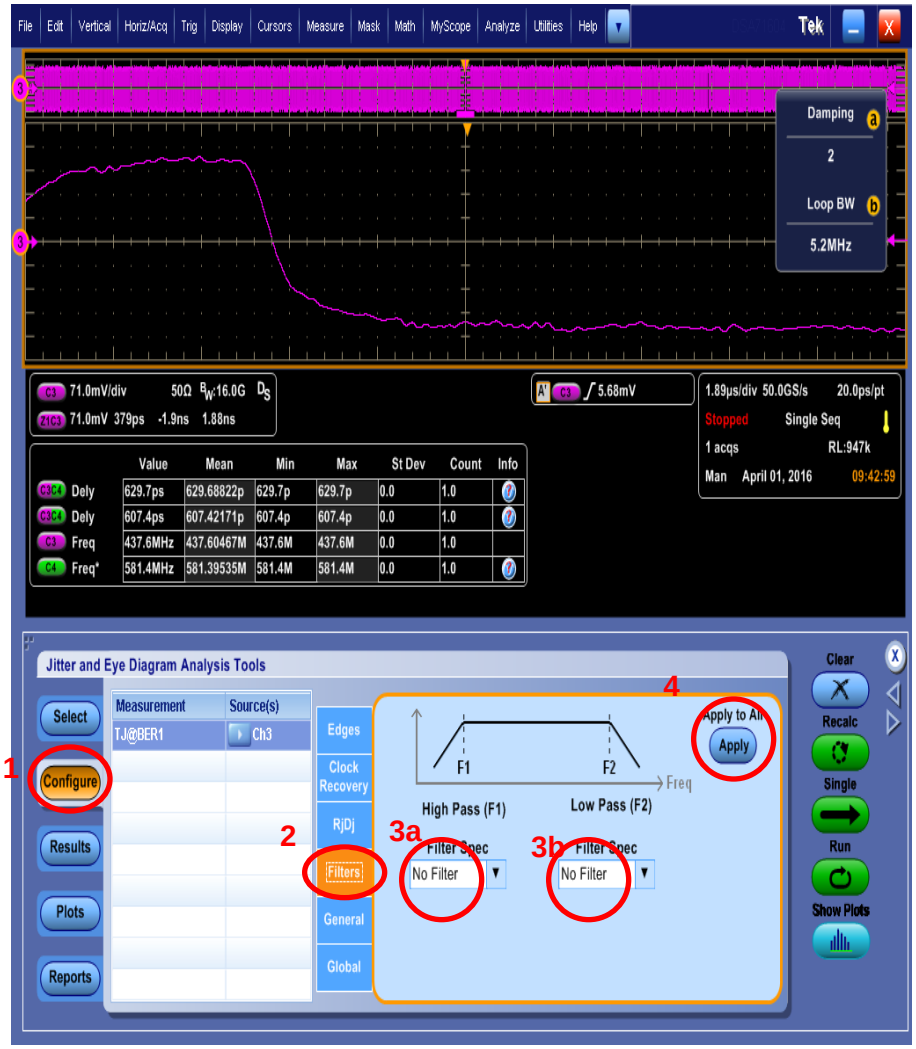
1. Go to **Configure** menu
2. Select **Edges**
3. Select **Auto**
4. Select **Both (some SW dose not have this option)**

Tx Output Jitter
Configure Clock Recover



1. Go to **Configure** menu
2. Select **Clock Recover**
   - 2a. Method = **PLL Custom BW**
   - 2b. PLL Type = **Type II**
   - 2c. Chose **Loop BW**
   - 2d. Loop BW = **f/15**
     - for exaple, pclk=78MHz
       - f/15 = 5.2MHz
   - 2e. Damping = **2**
3. **Apply to All**

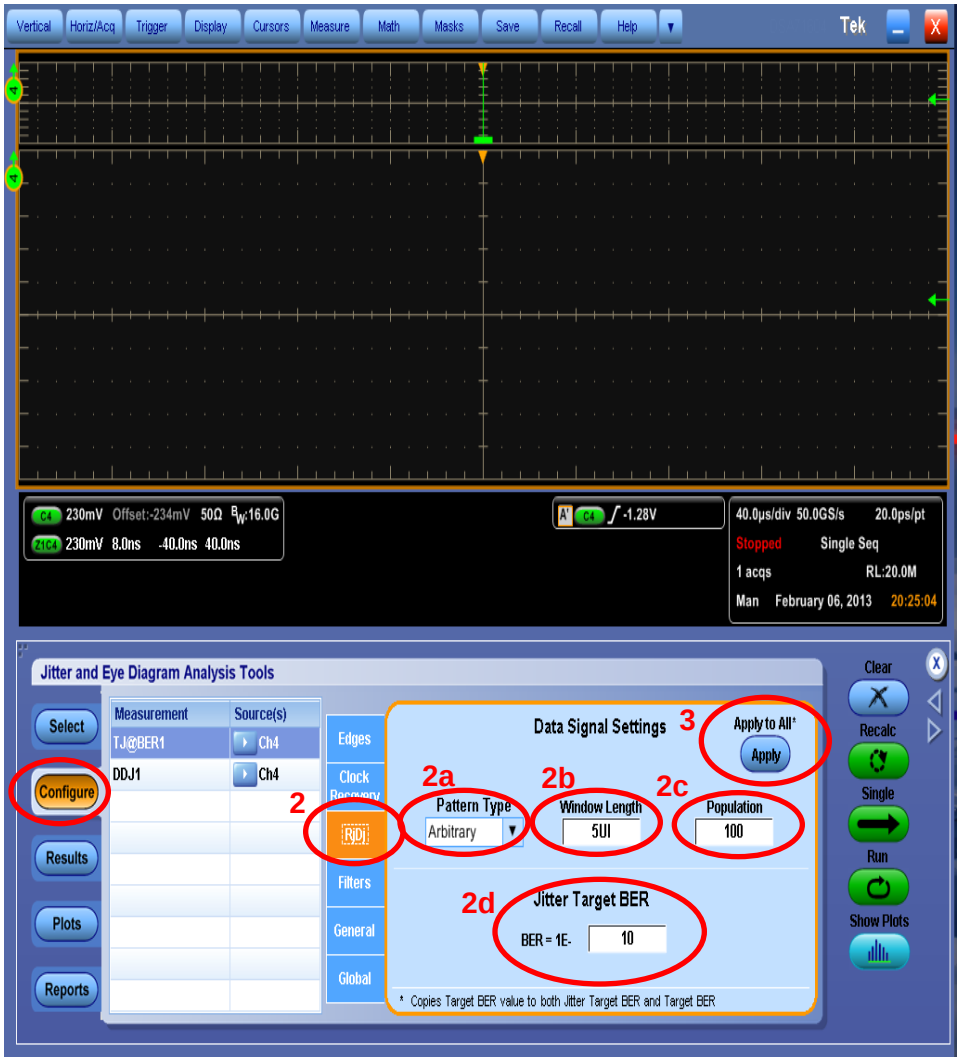
Tx Output Jitter Configure Filter



1. Go to **Configure** menu
2. Select **Filters**
3. Chose **No Filter** for both High Pass and Low Pass

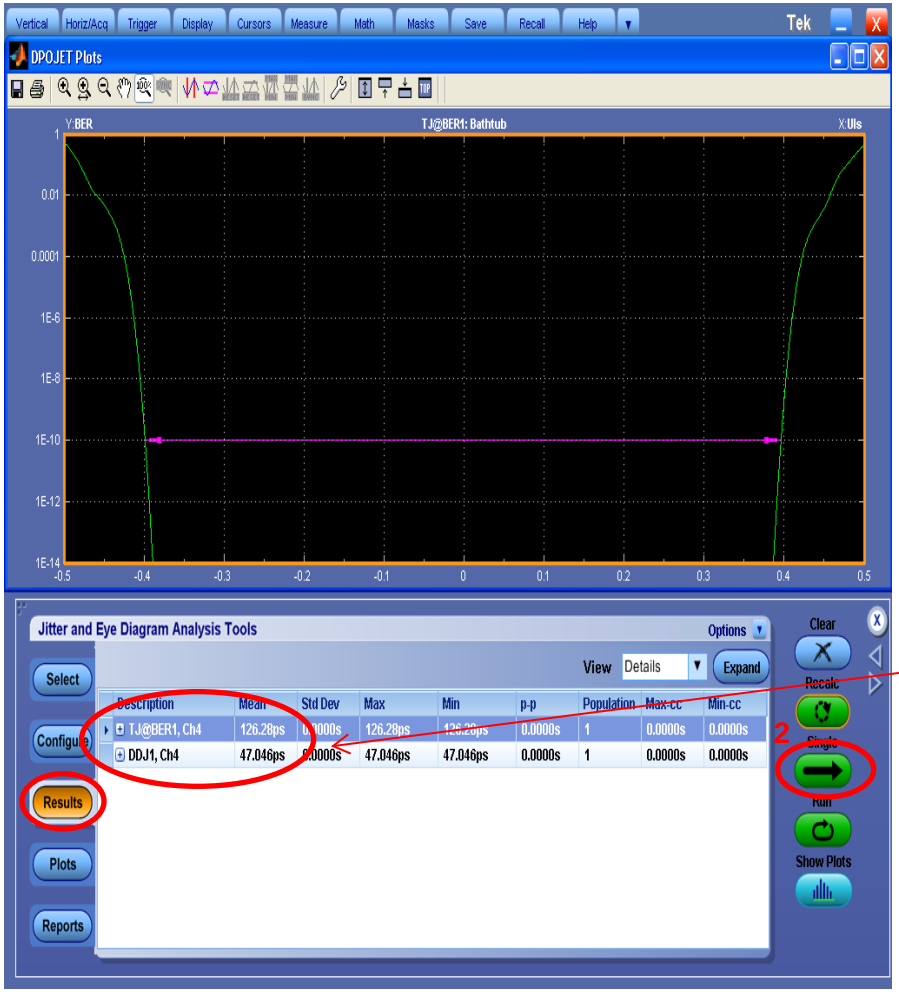
4. **Apply to All**

Tx Output Jitter Configure RjDj



1. Go to **Configure** menu
2. Select **RjDj**
    a. Pattern = **Arbitrary**
    b. Window Length = **5**
    c. Population = **100**
    d. Jitter Target BER = 1E-**10**
3. **Apply to All**

Tx Output Jitter Results

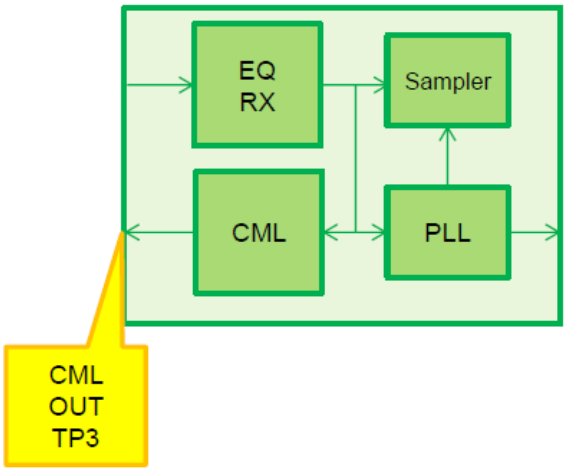


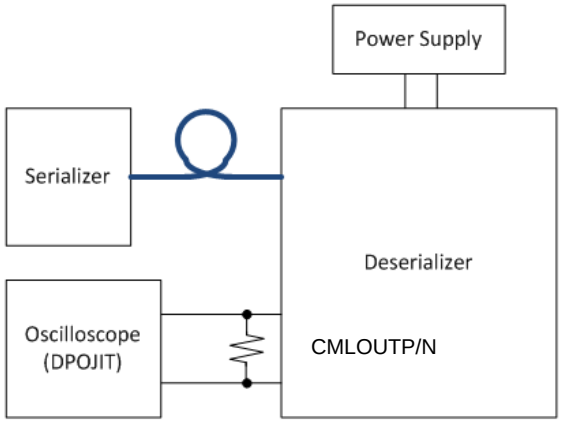
1. Click "**Single**" to capture measurement

2. Go to **Results**

3. click on "**Run**" to get distribution of jitter

Measurement results will be reported in this format





TP3: CMLOUT OUTPUT JITTER

TP3: Ew (CMLOUT Eye Opening)

CMLOUT Eye Opening can be defined by t_{BIT} (1UI) – TJ@BER:

a) Enable CMLOUT: Set Register 0x3F[4] = 0'b
b) Set Clock recover using custom PLL with Loop BW at f/15, where f is the PCLK frequency
c) Use TJ@BER with Target BER = 10 (BER = 1E - 10)

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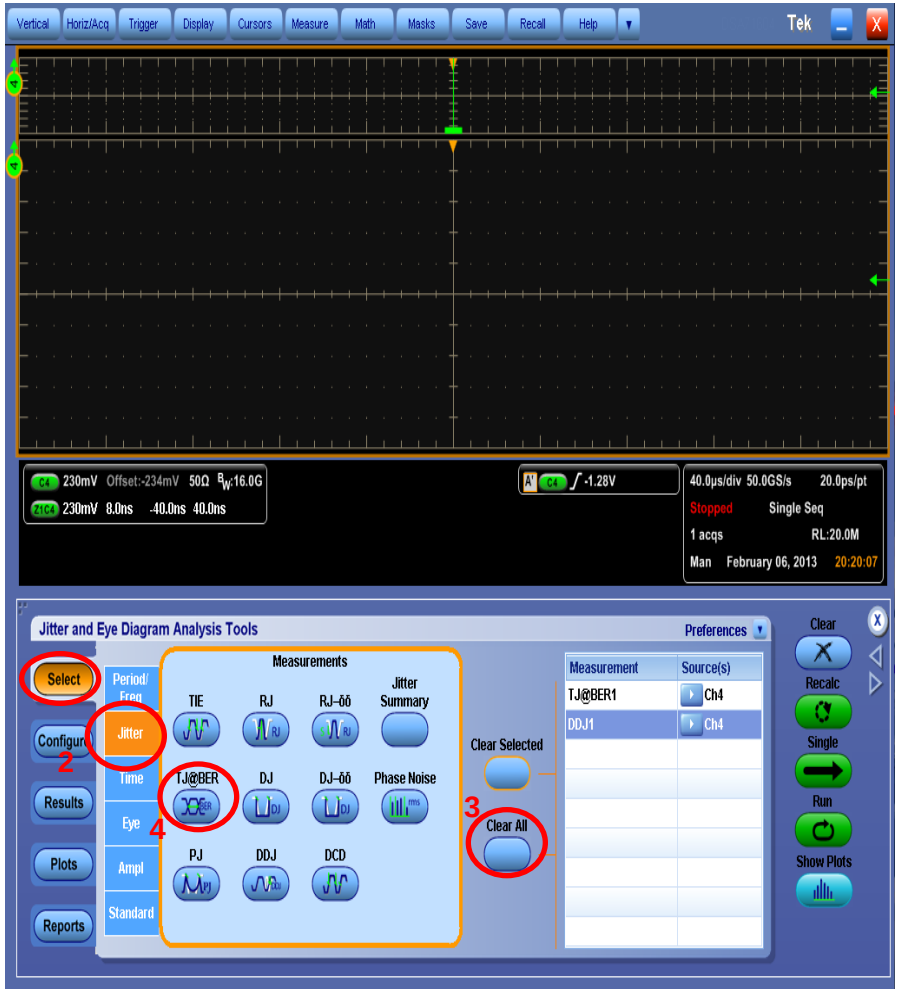
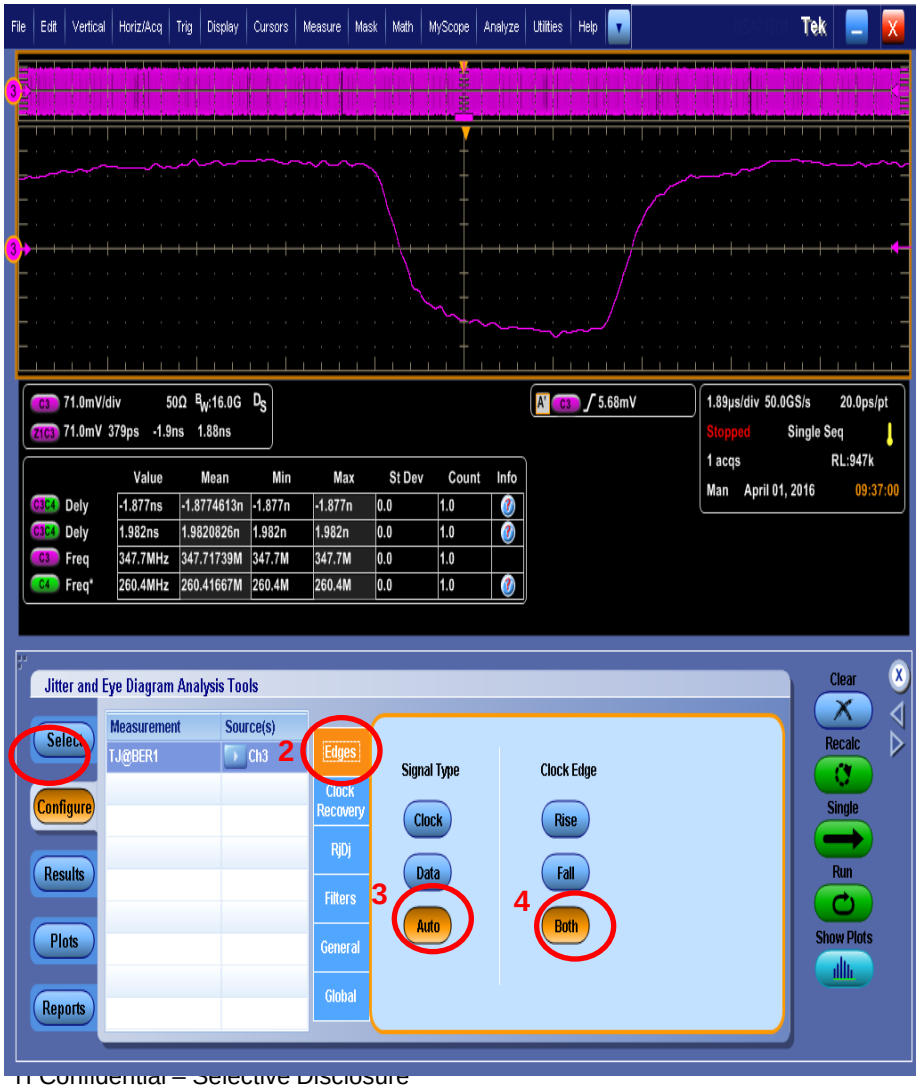
CMLOUT Output Jitter
Select Jitter Measurement



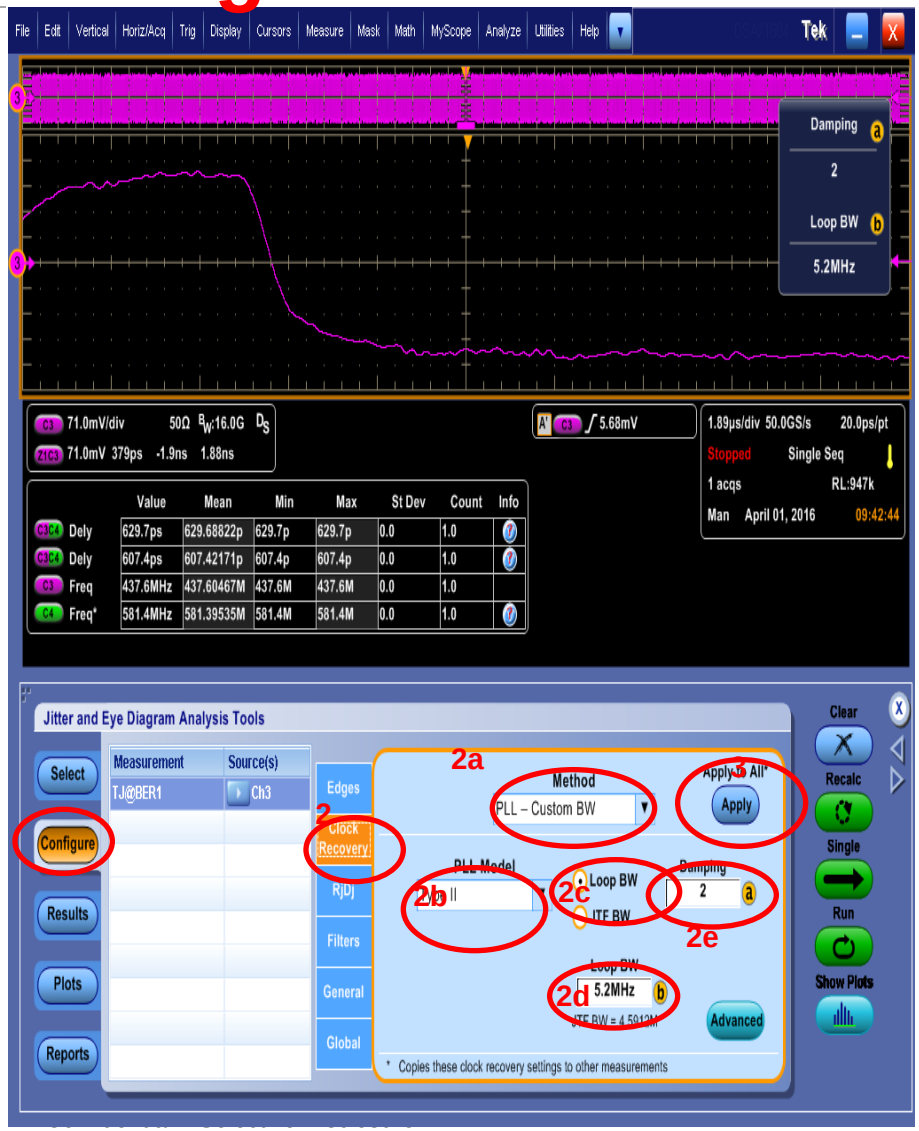
1. Go to jitter **Select** menu
2. Select **Jitter**
3. **Clear All**
4. Select **TJ@BER**

CMLOUT Output Jitter Configure Edges



1. Go to **Configure** menu
2. Select **Edges**
3. Select **Auto**
4. Select **Both (some SW dose not have this option)**

CMLOUT Output Jitter Configure Clock Recover



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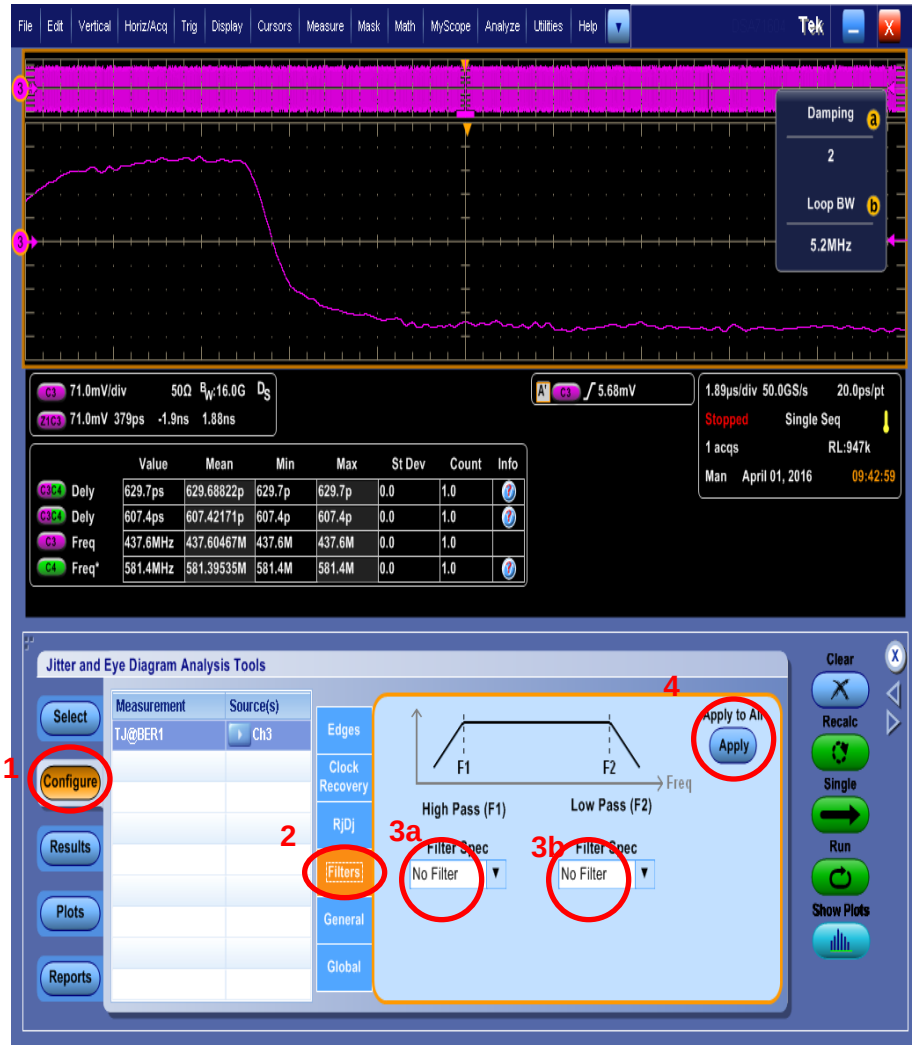
       - f/15 = 5.2MHz
   - 2e. Damping = **2**
3. **Apply to All**

CMLOUT Output Jitter Configure Filter



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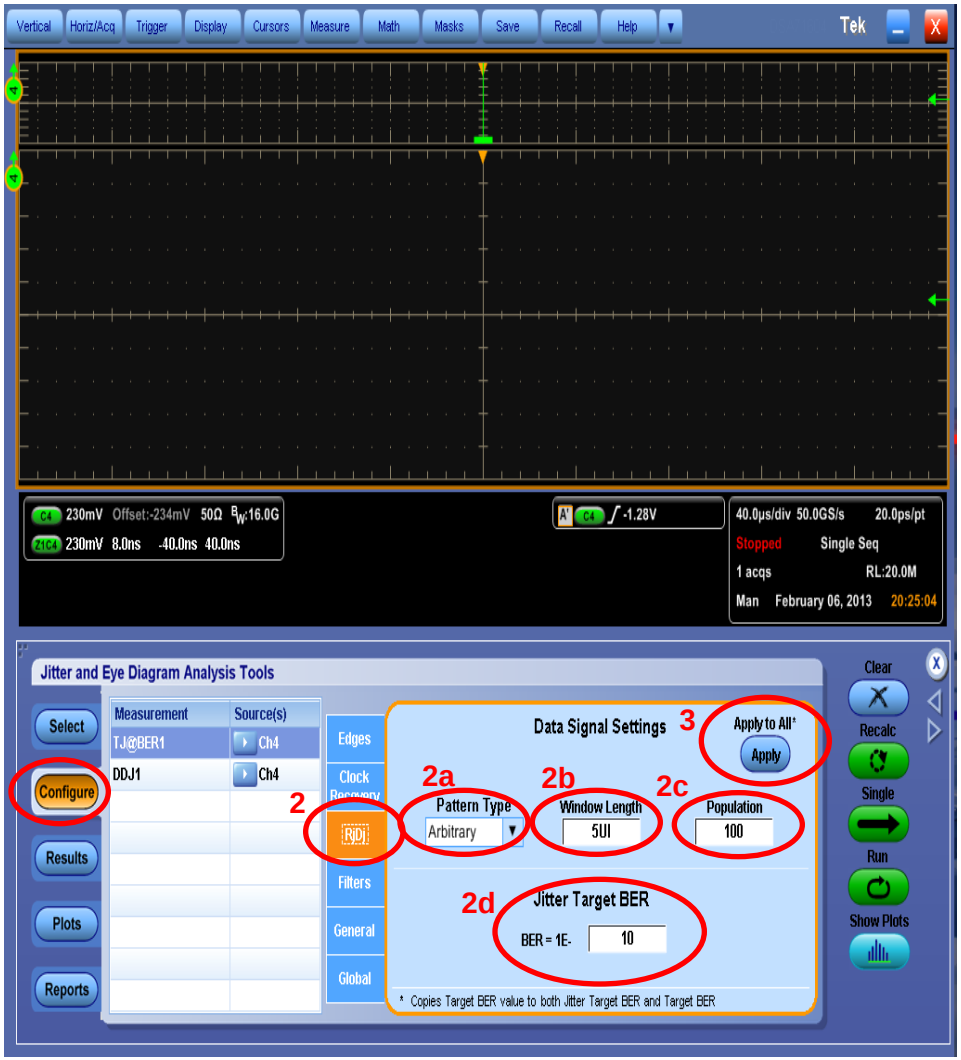
2. Select **Filters**
3. Chose **No Filter** for both High Pass and Low Pass

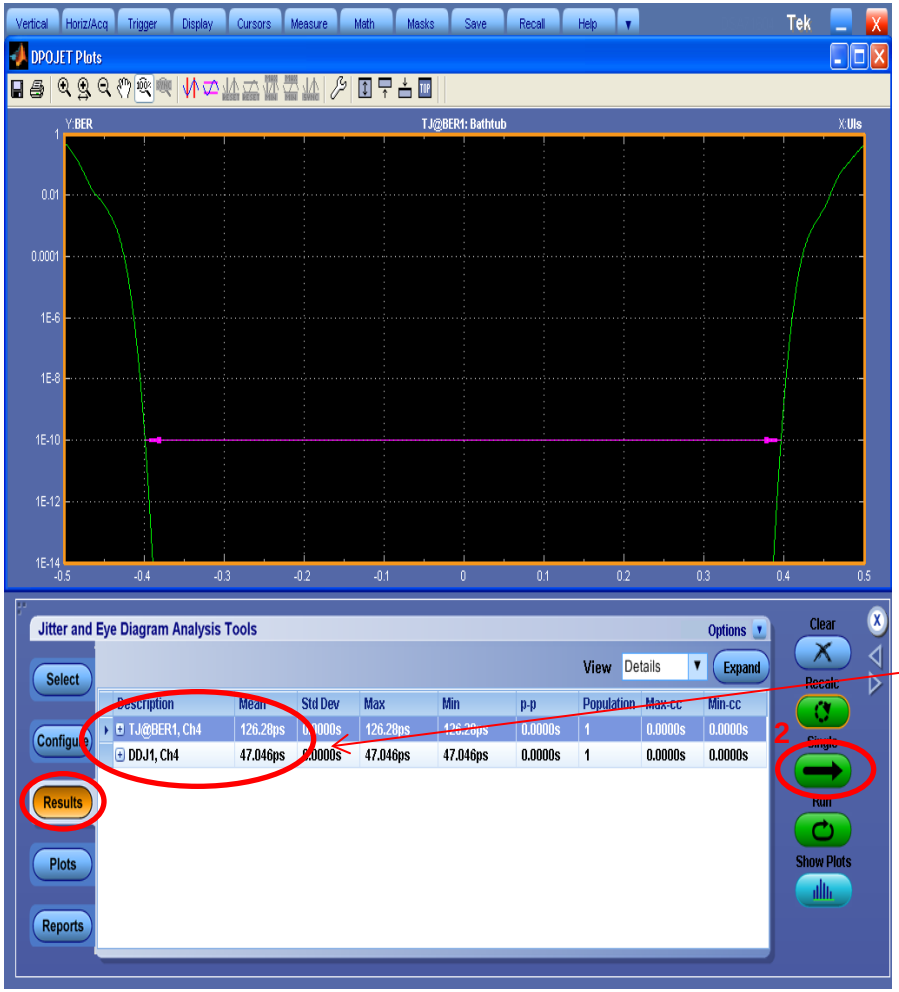
4. **Apply to All**

CMLOUT Output Jitter Configure RjDj



1. Go to **Configure** menu
2. Select **RjDj**
    a. Pattern = **Arbitrary**
    b. Window Length = **5**
    c. Population = **100**
    d. Jitter Target BER = 1E-**10**
3. **Apply to All**

CMLOUT Output Jitter Results



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