INNOLUX 群創光電

PRODUCT SPECIFICATION

Doc. Number:

■ Tentative Specification
☐ Preliminary Specification
☐ Approval Specification

MODEL NO.: P173ZZZ
SUFFIX:BZ1 Rev.A1

V2 PCBa

Customer:

APPROVED BY **SIGNATURE**
Name / Title

(Please return 1 copy for your confirmation with your signature and comments.)

Approved By	Checked By	Prepared By
OWEN.HUNG	MINGHUEI.WANG	Peichun.yao

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REVISION HISTORY

Version	Date	Page	Description
1.0	2021.03.31	P5 P31	修正尺寸
1.1	2021.04.19	all	

PRODUCT SPECIFICATION

1. GENERAL DESCRIPTION

1.1 OVERVIEW

P173ZZZ-BZ1 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 UHD, 3840(H) x2160(V) screen and with LED backlight driving circuit. All input signals are eDP(Embedded DisplayPort) interface compatible.

1.2 GENERAL SPECIFICATIONS

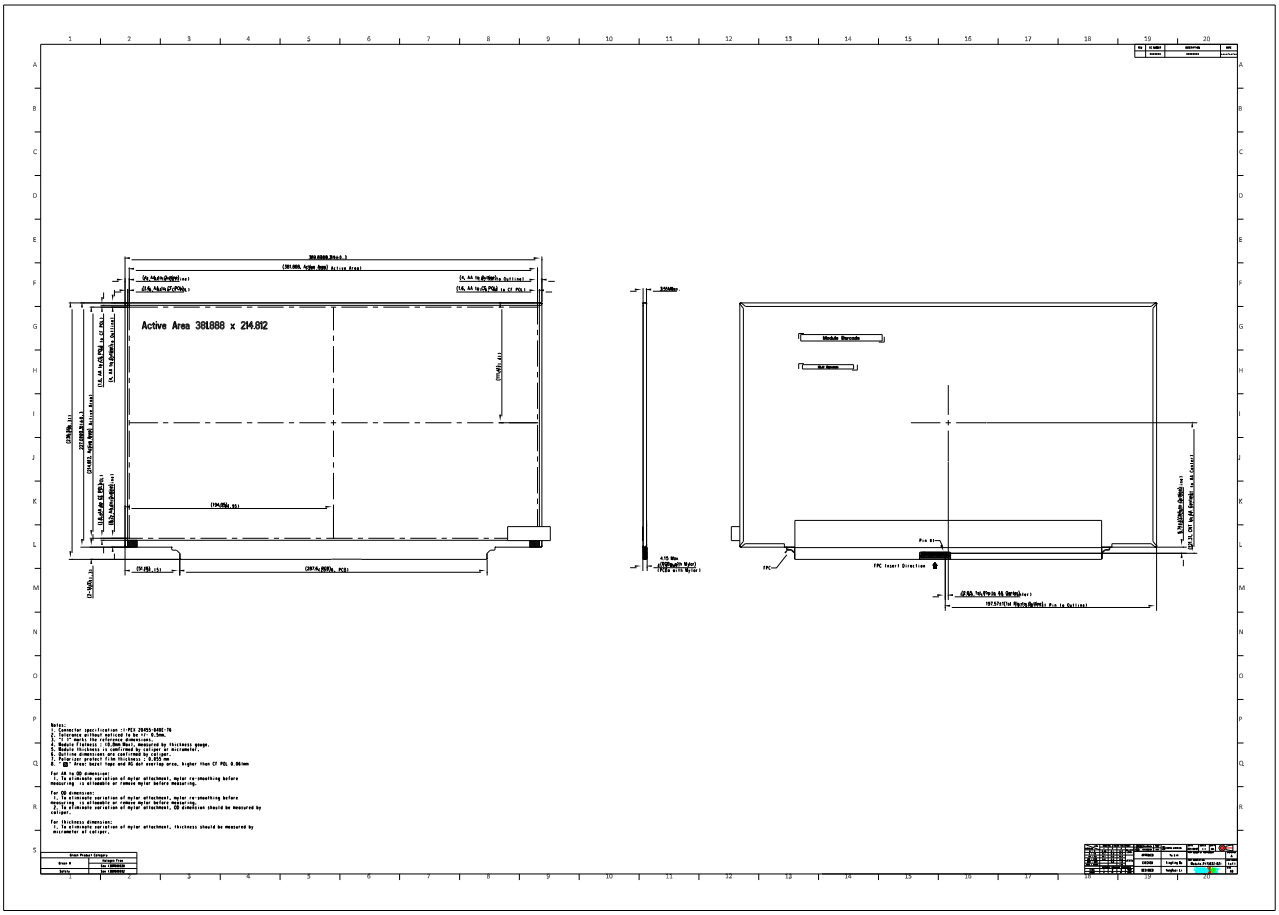
Item	Specification	Unit	Note
Screen Size	17.3" (diagonal)	inch	-
Driver Element	LTPS TFT active matrix	-	-
Pixel Number	3840x R.G.B. x 2160	pixel	-
Pixel Pitch	0.09945(H) x 0.09945(V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Contrast Ratio	100,000:1 typ (HDR on)		-
Response Time [ms]	25 (typ)	[ms]	
Transmissive mode	Normally black	-	-
Surface Treatment	AG	-	-
Luminance, White	1180(Typ).	nits	-
ElectricalInterface	eDP1.4		
GlassThickness(LCM)	0.3	mm	
Power Consumption (include LED driver efficiency)	Total 23W (Max.) @ cell 2.8 W (Max.) ,1180nit (Full on)	W	(1)

Note (1) The specified power consumption (with converter efficiency) is under the conditions at LCD_VCC =3.3V, fv = 60Hz, LED_VCCS = 12V and Ta = 25 ± 2 ºC, whereas **Mosaic8*4** pattern is displayed.

2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	389.59	389.89	390.19	mm	(1)(2)
	Vertical (V,w/o PCBa)	226.71	227.01	227.31	mm	
	Vertical (V,w/i PCBa)	-	238.31	-	mm	
	Thickness (T, w/o PCBa)	-	3.29	3.5	mm	
	Thickness (T, PCBa)	-	3.88	4.15	mm	
Active Area	Horizontal	-	381.888	-	mm	
	Vertical	-	214.812	-	mm	
Weight		-	495	520	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.



Note (2) Dimensions are measured by caliper.

module_p173zzz-bz1_v2_plc_20210407.pd

2.1 CONNECTOR TYPE

Please refer appendix outline drawing for detail design.

Connector Part No.:IPEX-20455-040E-76

3. ABSOLUTE MAXIMUM RATINGS

3.1 ELECTRICAL ABSOLUTE RATINGS

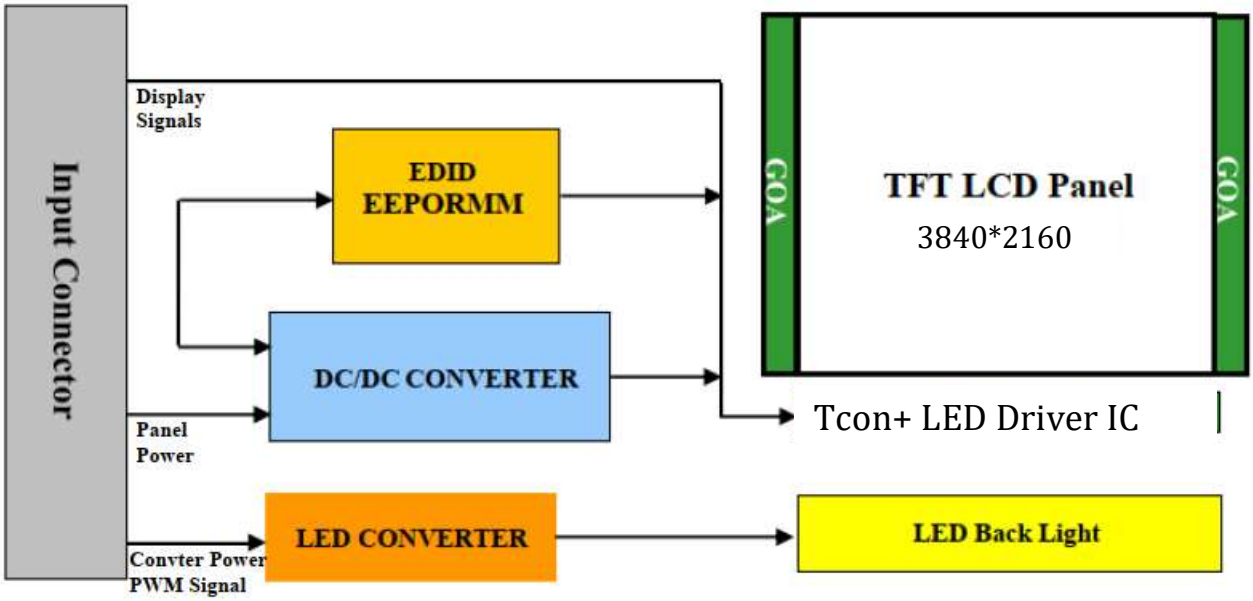
3.1.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	LCD_VCC	3.0	3.6	V	(1)
Converter Input Voltage	LED_VCCS	12	21	V	(1)
Converter Control Signal Voltage	LED_EN	3.1	3.5	V	3.3V +/-5%
Converter Control Signal Voltage	LED_PWM	3.1	3.5	V	3.3V +/-5%

Note (1) Stresses beyond those listed in above “ELECTRICAL ABSOLUTE RATINGS” may cause permanent damage to the device. Normal operation should be restricted to the conditions described in “ELECTRICAL CHARACTERISTICS”.

4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM



4.2. INTERFACE CONNECTIONS

PIN ASSIGNMENT

Pin	Symbol	Description	Remark
1	NC	No connection	
2	GND	Ground	
3	RX3N	eDP differential data3 input (Negative)	
4	RX3P	eDP differential data3 input (Positive)	
5	GND	Ground	
6	RX2N	eDP differential data2 input (Negative)	
7	RX2P	eDP differential data2 input (Positive)	
8	GND	Ground	
9	RX1N	eDP differential data1 input (Negative)	
10	RX1P	eDP differential data1 input (Positive)	
11	GND	Ground	
12	RX0N	eDP differential data0 input (Negative)	
13	RX0P	eDP differential data0 input (Positive)	
14	GND	Ground	
15	AUX_P	True Signal Auxiliary Channel	
16	AUX_N	Complement Signal Auxiliary Channel	
17	GND	Ground	
18	VCCS_3V3	3.3V input	
19	VCCS_3V3	3.3V input	
20	VCCS_3V3	3.3V input	
21	VCCS_3V3	3.3V input	
22	AGING	Aging test	
23	GND	Ground	
24	GND	Ground	

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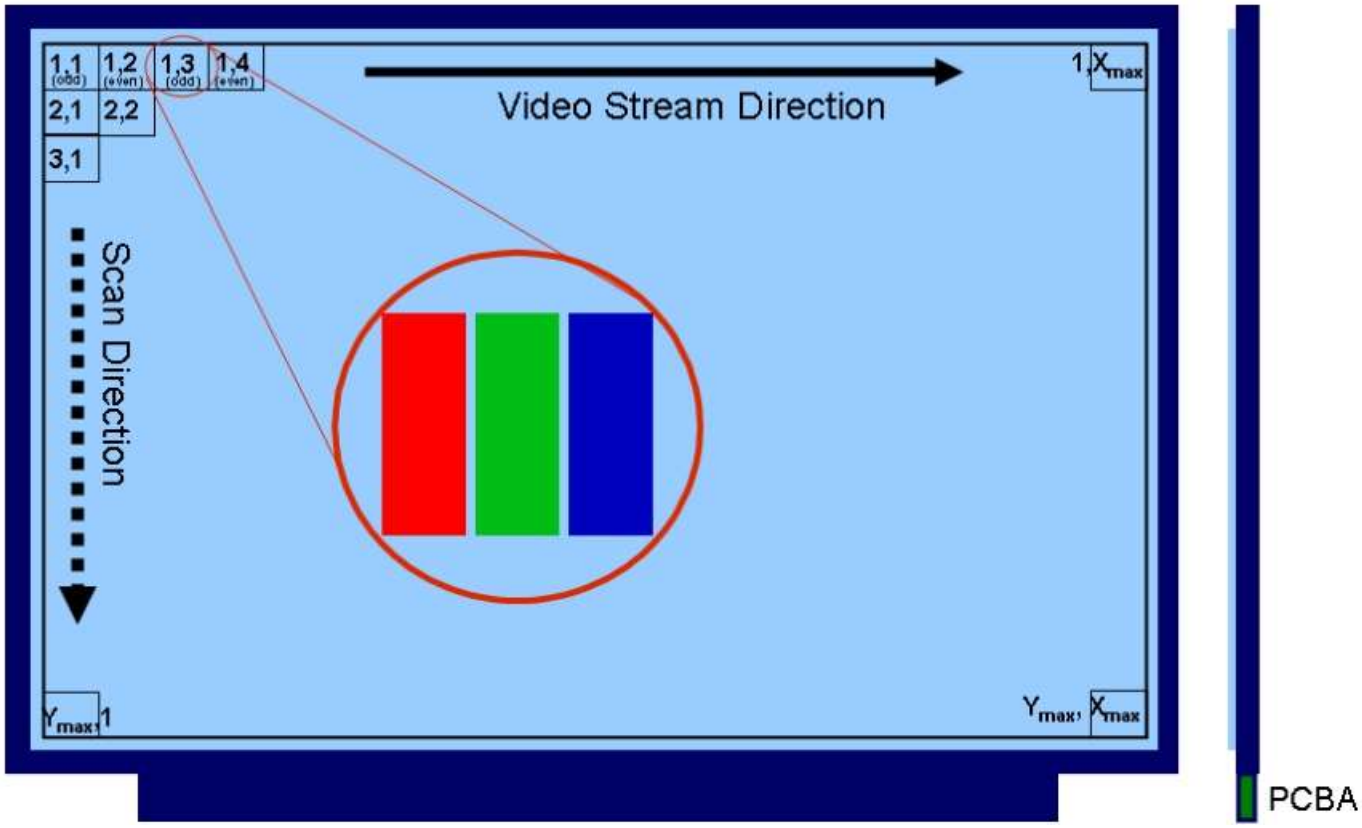
V	GND	Ground	
26	GND	Ground	
27	HPD	HPD signal pin	
28	GND	Ground	
29	GND	Ground	
30	GND	Ground	
31	GND	Ground	
32	LED_EN	LED On / Off	
33	NC	No connection	
34	NC	No connection	
35	NC	No connection	
36	BL_VCCS	Backlight_VCCS input	
37	BL_VCCS	Backlight_VCCS input	
38	BL_VCCS	Backlight_VCCS input	
39	BL_VCCS	Backlight_VCCS input	
40	NC	No connection	

Note (1) The first pixel is odd as shown in the following figure.



Note (2) The setting of BIST function are as follows.

Pin	Enable	Disable
BIST_EN	Hi	Lo or Open

Hi = High level, Lo = Low level.

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELETRONICS SPECIFICATION

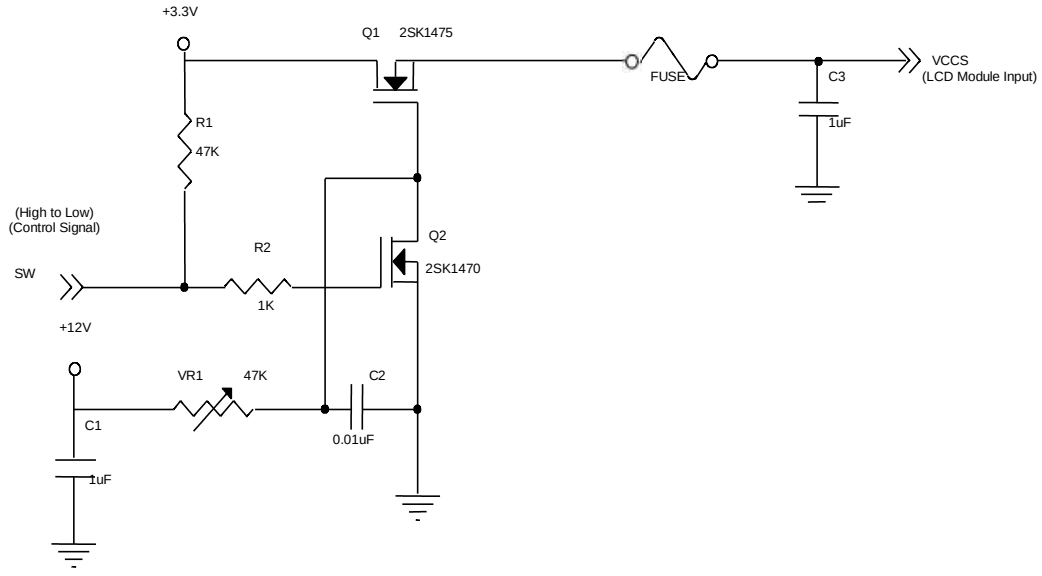
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		LCD_VCC	3.0	3.3	3.6	V	(1)
Ripple Voltage		V_{RP}	-	-	100	mV	(1)
Inrush Current		I_{RUSH}	-	-	1.8	A	(1),(2)
Power Supply Current	Mosaic 8*6	Icc	0.65	-	0.85	mA	(3)a
	Black		0.63	-	0.83	mA	(3)
	(HeavyPattern)		0.93	-	1.13	mA	
HPD output voltage			2.25	-	3.6	V	
HPD Impedance		R_{HPD}	-	100K	-	ohm	(4)
HPD	High Level		2.25	-	-	V	(5)
	Low Level		0	-	0.7	V	(5)

Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

Note (2) I_{RUSH}: the maximum current when LCD_VCC is rising

I_{IS}: the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.



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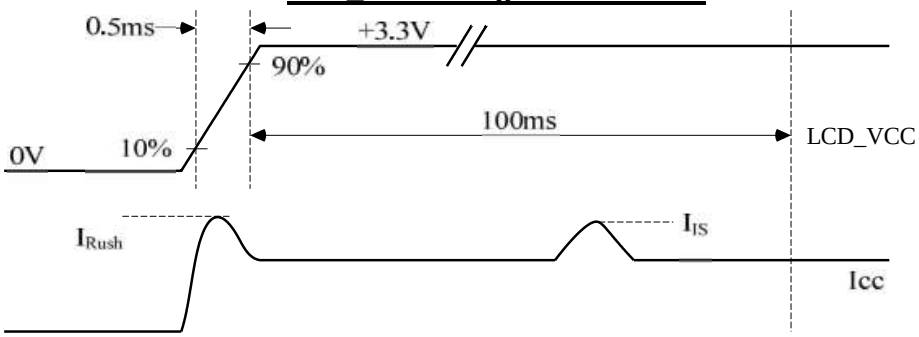
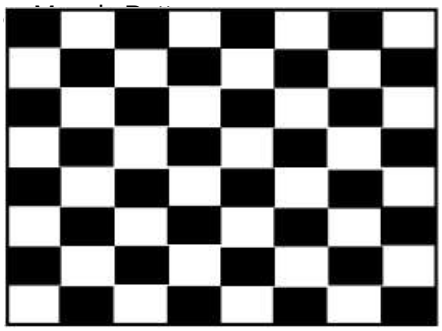
LCD_VCC rising time is 0.5ms



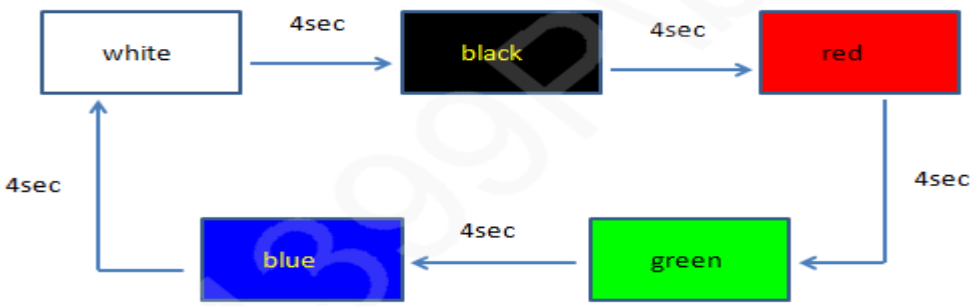
Note (3) The specified power supply current is under the conditions at LCD_VCC = 3.3 V, Ta = 25 ± 2 ºC, DC Current and f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.



Note (4) The specified signals have equivalent impedances pull down to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. Please refer to Note (4) of 4.3.2 LED CONVERTER SPECIFICATION to obtain more information.

Note (5) When a source detects a low-going HPD pulse, it must be regarded as a HPD event. Thus, the source must read the link / sink status field or receiver capability field of the DPCD and take corrective action.

Note (6) LCD panel self-test (BIST mode) pattern are shown as below image. Each pattern displays 2 sec and recurring.



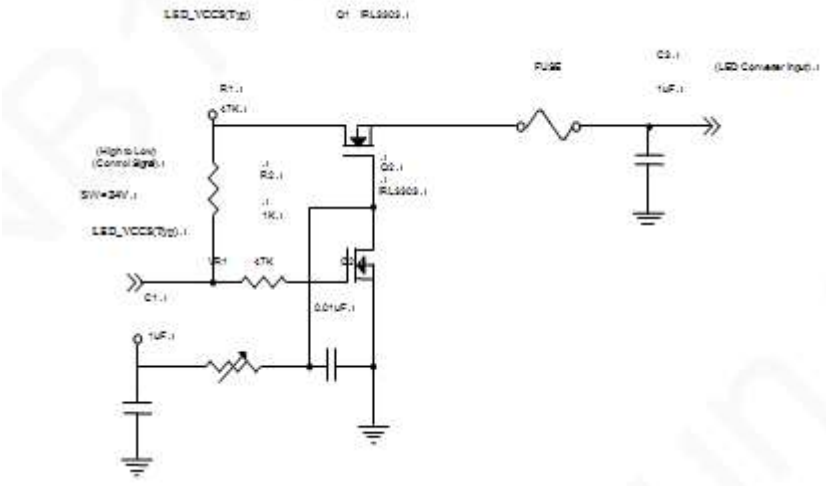
4.3.2 LED CONVERTER SPECIFICATION

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Input Power Supply Voltage		LED_VCCS	12	-	21	V	
Converter Input Power Supply Current		ILED_VCCS	0.75	-	1.15	A	
Converter Inrush Current		ILEDRUSH	-	-	2.8	A	(1)
Input Voltage (LED_EN)	High Level	VIH	1.26	-	2.1	V	(4)
	Low Level	VIL	0	-	0.54	V	(4)
LED_EN Impedance		RLED_EN	-	400	-	ohm	(4)
Input Voltage (LED_PWM)	High Level	VIH	0.81	-	1.35	V	
	Low Level	VIL	0.36	-	0.72	V	
PWM Resolution			7	-	12	bits	

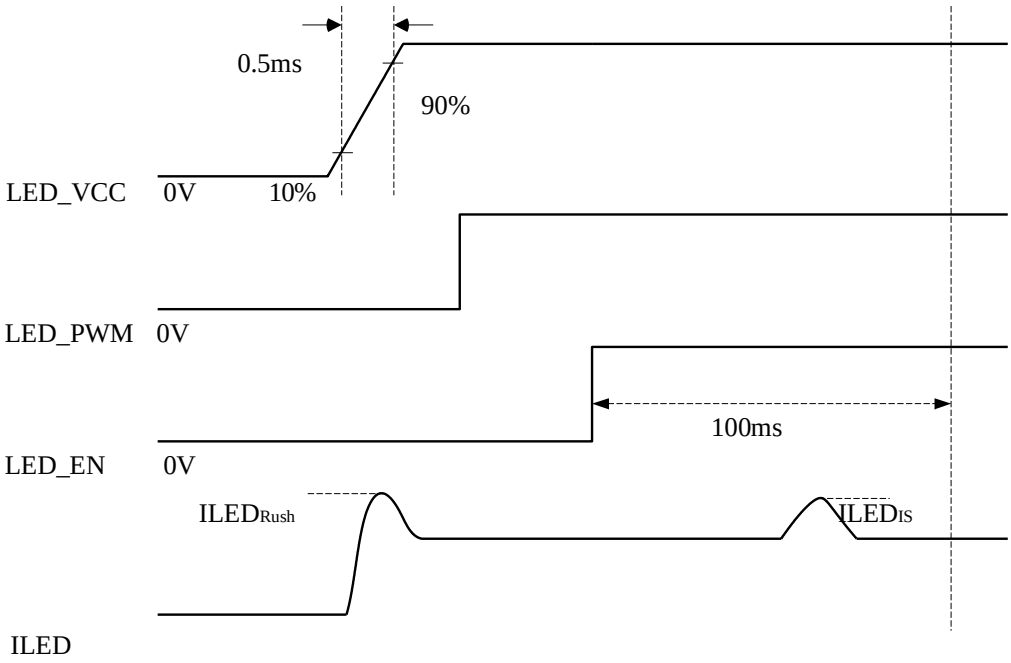
Note (1) $I_{LED_{RUSH}}$: the maximum current when LED_VCCS is rising,

$I_{LED_{IS}}$: the maximum current of the first 100ms after power-on,

Measurement Conditions: Shown as the following figure. LED_VCCS = Typ, Ta = 25 ± 2 ºC, f_{PWM} = 200 Hz, Duty=100%.



VLED rising time is 0.5ms



Note (2) If PWM control frequency is applied in the range less than 1KHz, the "waterfall" phenomenon on the screen may be found. To avoid the issue, it's a suggestion that PWM control frequency should follow the criterion as below.

PWM control frequency f_{PWM} should be in the range

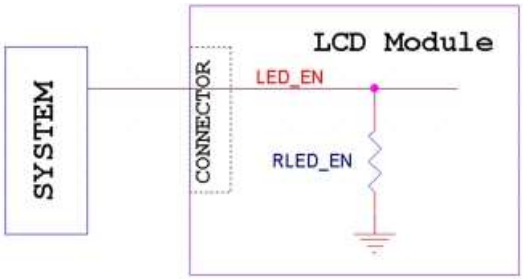
$$(N + 0.33) * f \leq f_{PWM} \leq (N + 0.66) * f$$

N : Integer $(N \geq 3)$

f : Frame rate

Note (3) The specified LED power supply current is under the conditions at "LED_VCCS = Typ.", Ta = 25 ± 2 ºC, f_{PWM} = 200 Hz, Duty=100%.

Note (4) The specified signals have equivalent impedances pull down to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. For example, the figure below describes the equivalent pull down impedance of LED_EN (If it exists). The rest pull down impedances of other signals (eg. HPD, PWM …) are in the same concept.



Note (5) If the cycle-to-cycle difference of PWM duty exceeds 0.1%, especially when the PWM duty is low, slight brightness change might be observed.

4.3.3 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
BLU Power Supply Voltage	V_L	5.2	5.6	6	V	
BLU Power Supply Current	I_L		3.393		A	
Power Consumption	P_L	17.64	19	20.36	W	
LED Life Time	L_{BL}	15000	-	-	Hrs	

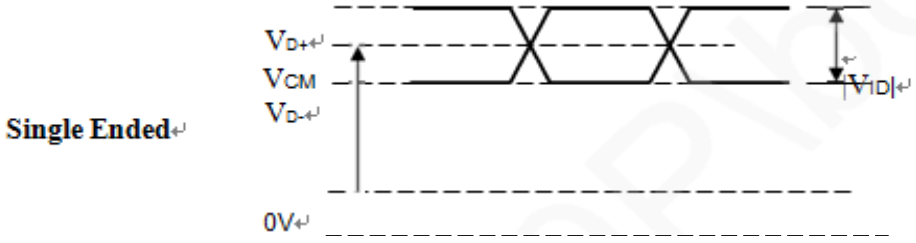
Note:
Parallel:2 strings
Series: 2 pcs
Partition:1440 area

4.4 DISPLAY PORT INPUT SIGNAL TIMING SPECIFICATIONS

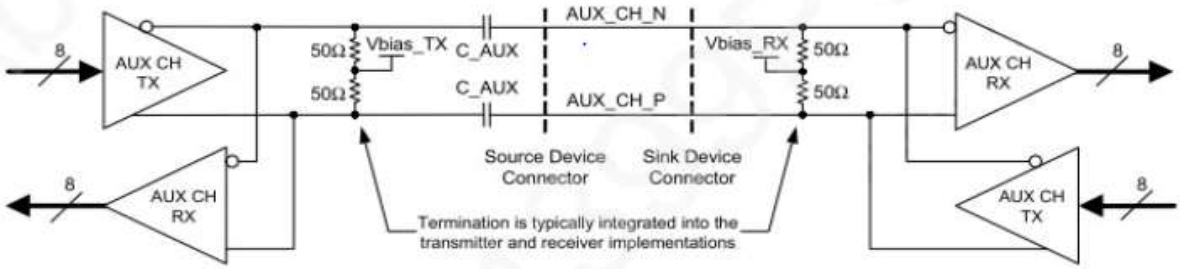
4.4.1 ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Differential Signal Common Mode Voltage(MainLink and AUX)	VCM	0.3		0.7	V	(1)(4)
AUX AC Coupling Capacitor	C_Aux_Source	75-		200-	nF	(2)

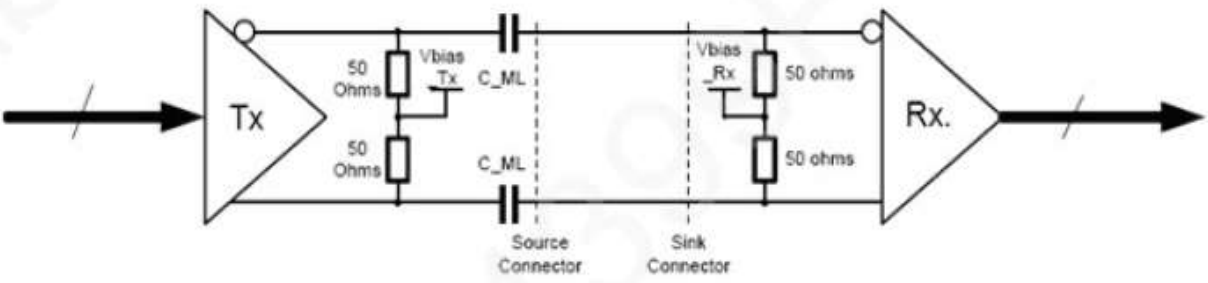
Note (1)Display port interface related AC coupled signals should follow VESA DisplayPort Standard Version1. Revision 1a and VESA Embedded DisplayPort™ Standard Version 1.2. There are many optional items described in eDP1.2. If some optional item is requested, please contact us.



(2) AUX CH consists of an AC-coupled, doubly-terminated differential pair. Manchester-II coding is used as the channel coding for AUX transaction over AUX CH. AUX CH provides a data rate of 1Mbps.



3) The Main-Link consists of one, two, or four AC-coupled, doubly terminated differential pairs. Eight link rates are supported (1.62/2.16/2.43/2.7/3.24/4.32/5.4/8.1 Gbps). All enabled lanes must be operating at the same link rate. There is no dedicated clock channel. The clock is extracted from the data stream itself that is encoded with ANSI 8b/10b coding rule.



4.4.2 eDP 1.4 Interface Data Format

Lane 0	Lane 1	Lane 2	Lane 3
R0-7:0	R1-7:0	R2-7:0	R3-7:0
G0-7:0	G1-7:0	G2-7:0	G3-7:0
B0-7:0	B1-7:0	B2-7:0	B3-7:0
R4-7:0	R5-7:0	R6-7:0	R7-7:0
G4-7:0	G5-7:0	G6-7:0	G7-7:0
B4-7:0	B5-7:0	B6-7:0	B7-7:0
R8-7:0	R9-7:0	R10-7:0	R11-7:0
G8-7:0	G9-7:0	G10-7:0	G11-7:0
B8-7:0	B9-7:0	B10-7:0	B11-7:0

8bit RGB to a 4-Lane Main-Link Mapping

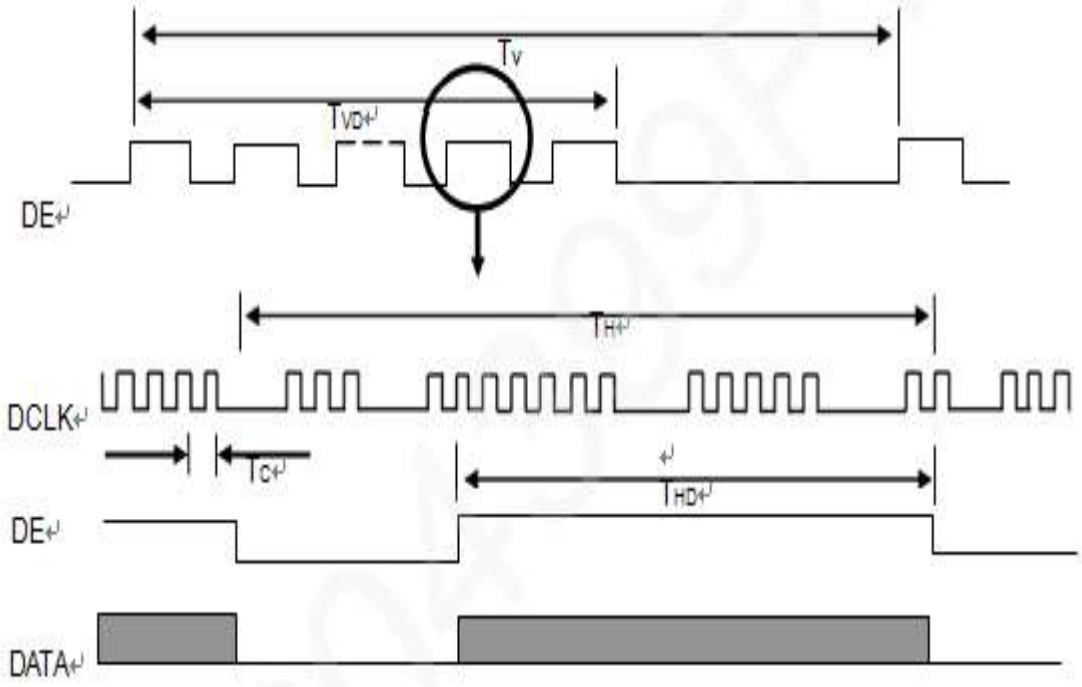
4.5 DISPLAY TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	-	1267.2	-	MHz	-
DE	Vertical Total Time	TV	-	2200	-	TH	-
	Vertical Active Display Period	TVD	-	2160	-	TH	-
	Vertical Active Blanking Period	TVB	-	40	-	TH	-
	Horizontal Total Time	TH	-	4000	-	Tc	-
	Horizontal Active Display Period	THD	-	3840	-	Tc	-
	Horizontal Active Blanking Period	THB	-	160	-	Tc	-

Note (1) The panel can operate at 60Hz normal mode and power saving mode, respectively. All reliability tests are based on specific timing of 60Hz refresh rate. We can only assure the panel's electrical function at power saving mode.

INPUT SIGNAL TIMING DIAGRAM



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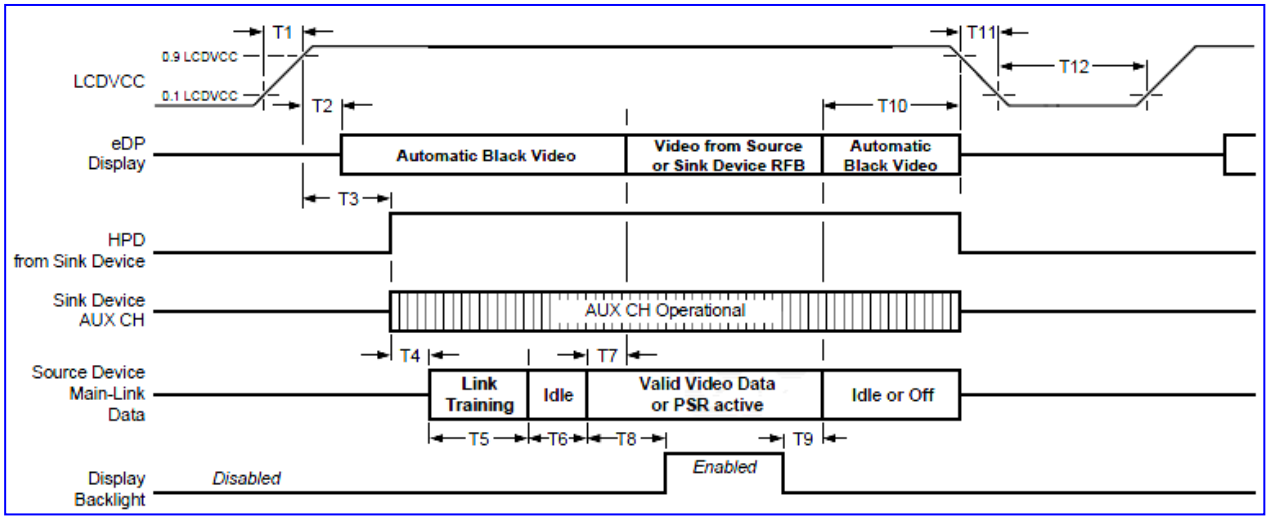
4.6 POWER ON/OFF SEQUENCE



Time Specifications

Parameter	Description	Reqd. By	Value		Unit	Notes
			Min	Max		
T1	Power rail rise time, 10% to 90%	Source Device	0.5	10	ms	-
T2	Delay from LCD,V_{CCS} to black video generation	Sink Device	0	200	ms	Automatic Black Video generation prevents display noise until valid video data is received from the Source device.[2,3]
T3	Delay from LCD,V_{CCS} to HPD high	Sink Device	0	200	ms	Sink device AUX CH must be operational upon HPD high .[4]
T4	Delay from HPD high to link training initialization	Source Device	0	-	ms	Allows for Source device to read Link capability and initialize
T5	Link training duration	Source Device	0	-	ms	Dependant on Source device link training protocol
T6	Link idle	Source Device	0	-	ms	Min Accounts for required BS-Idle pattern. Max allows for Source frame synchronization

Parameter	Description	Reqd. By	Value		Unit	Notes
			Min	Max		
T7	Delay from valid video data from Source to video on display	Sink Device	0	50	ms	Max value allows for the Sink device to validate video data and timing. At the end of T7, the Sink device will indicate that it detection valid video data, by setting the RECEIVE_PORT_0_STATUS bit of the STATUS bit of the SINK_STATUS register (DPCD Address 00205h, bit 0) to logic 1, and Sink device will no longer generate automatic Black Video
T8	Delay from valid video data from Source to backlight on	Source Device	80	-	ms	The Source device must assure display video is stable
T9	Delay from backlight disable to end of valid video data	Source Device	50	-	ms	The Source device must assure that the backlight is no longer illuminated. At the end of T9, the Sink device will indicate that it did not detect valid video data, by setting the RECEIVE _PORT_0_STATUS bit of the SINK_STATUS register (DPCD Address 00205h, bit 0;) to logic 0, and the Sink device will automatically display Black Video.[2,3]
T10	Delay from end of valid video data from Source to power off	Source Device	0	500	ms	
T11	V_{CCS} power rail fall time, 90% to 10%	Source Device	0.5	10	ms	-
T12	V_{CCS} Power off time	Source Device	500	-	ms	

Remark:

1. Please don't plug or unplug the interface cable when system is turned on.
2. The Sink device must include the ability to automatically and autonomously generate Black Video. The Sink device must automatically enable Black Video under the following conditions:
   - Upon LCDVCC power-on (within T2 max)
   - When the "No Video Stream Flag" (VB-ID Bit 3) is received from the Source device (at the end of T9)
3. The Sink device can implement the ability to disable the automatic Black Video function, as described in footnote "2",for system development and debugging purposes.
4. The Sink must support AUX Channel polling by the Source immediately following LCD VCC power-on without causing damage to the Sink device (the Source device can re-try if the Sink is not ready). The Sink device must be able to response to an AUX Channel transaction within the time specified within T3 max.

5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	oC
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	6	V
Input Signal	According to typical value in "4.3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I_L	2218	mA

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θx=0°, θY =0° Viewing Normal Angle	-	10_5	-	-	(2),(5), (7)
Response Time		T_R+T_F		-	25	-	ms	(3),(7)
Luminance of White		L			1180		cd/m^2	(4), (6),(7)
Color Chromaticity	Red	Rx		Typ –0.03	TBD	Typ +0.03	-	(1),(7)
		Ry			TBD		-	
	Green	Gx			TBD		-	
		Gy			TBD		-	
	Blue	Bx			TBD		-	
		By			TBD		-	
	White	Wx			0.313		-	
		Wy			0.329		-	
Color gamut		C.G		94.7	99.7	-	%	(8)
Viewing Angle	Horizontal	θ_{x+}	CR≥10	80	85	-	Deg.	(1),(5), (7)
		θ_{x-}		80	85	-		
	Vertical	θ_{Y+}		80	85	-		
		θ_{Y-}		80	85	-		
White Variation		δW_{5p}	θ_x=0°, θ_Y =0°	80	85	-	%	(5),(6), (7)
		δW_{13p}	θ_x=0°, θ_Y =0°	60	65	-	%	

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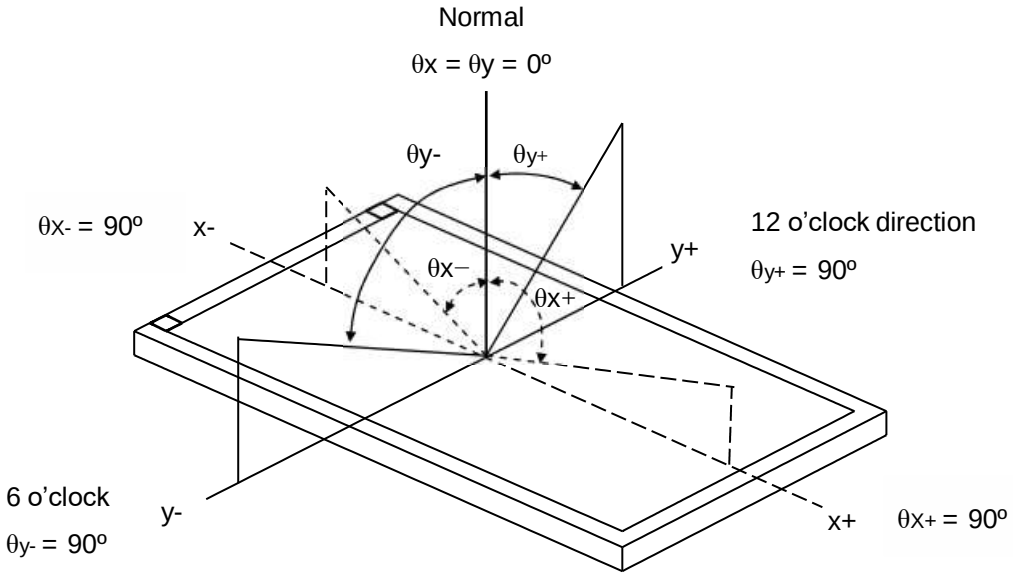
Note (1) Definition of Viewing Angle (θx, θy):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L255 / L0

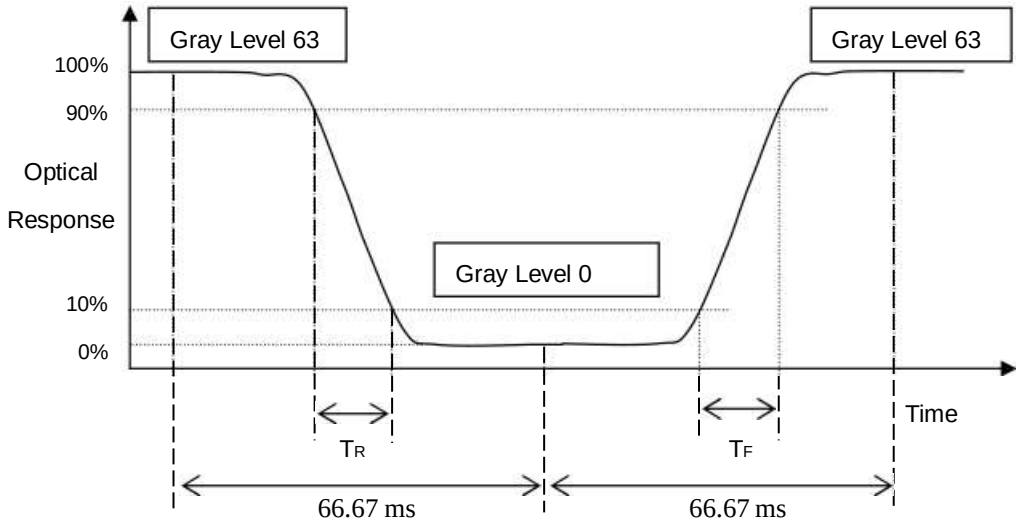
L63: Luminance of gray level255

L 0: Luminance of gray level 0

CR = CR (1)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (TR, TF):



Note (4) Definition of Average Luminance of White (L_{AVE}):

Measure the luminance of gray level 255 at 5 points

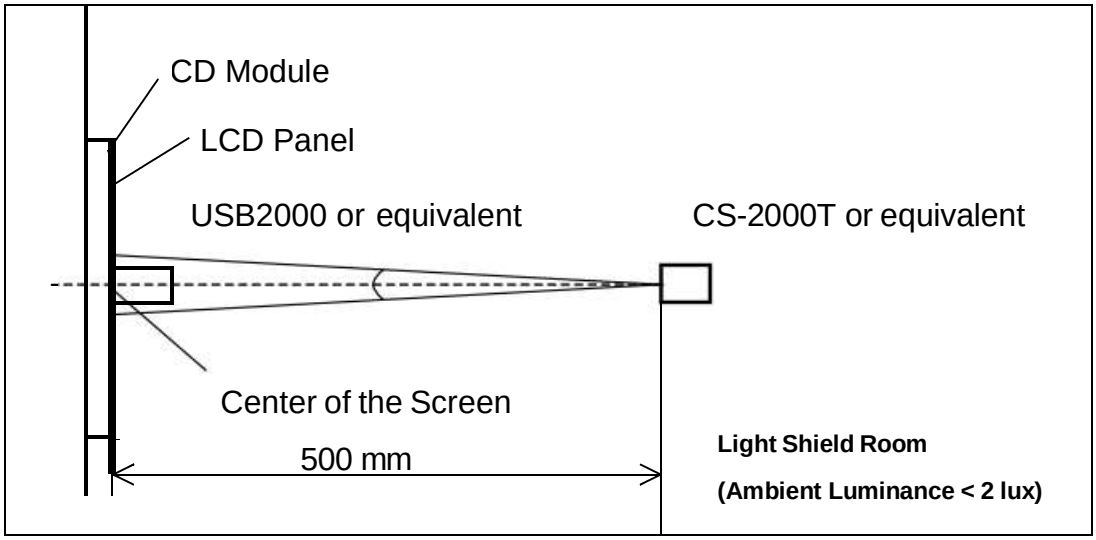
L_{AVE} = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (6)

PRODUCT SPECIFICATION

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.

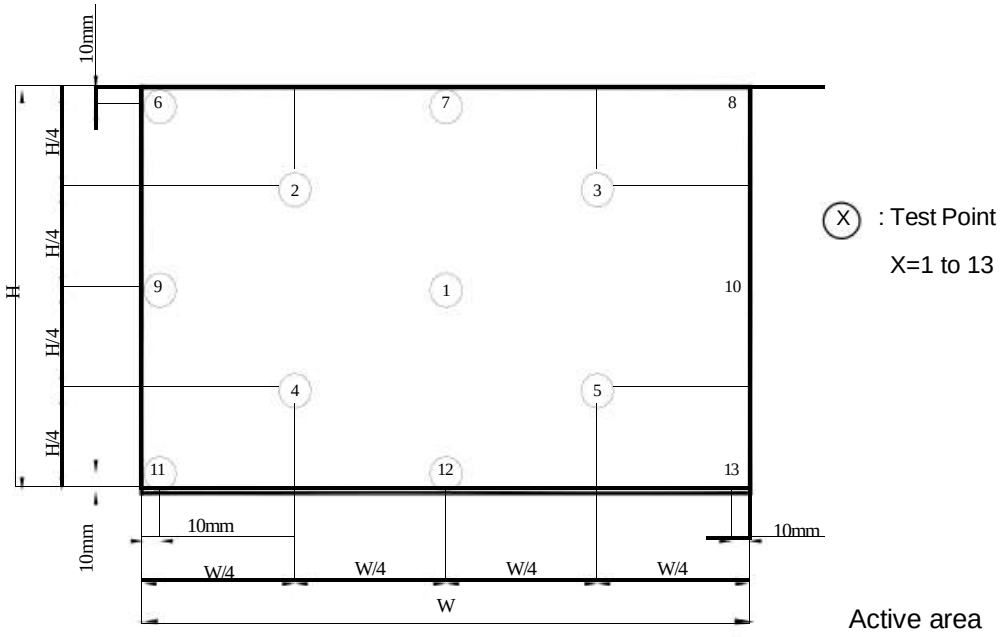


Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

δW_{5p} = {Minimum [L (1)~ L (5)] / Maximum [L (1)~ L (5)]}*100%

δW_{13p} = {Minimum [L (1)~ L (13)] / Maximum [L (1)~ L (13)]}*100%



Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

Note (8) Definition of color gamut (C.G%):

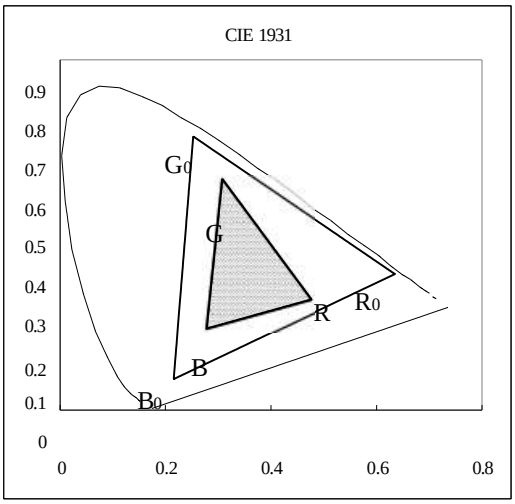
C.G%= ・R G B / ・R_0 G_0 B_0,*100%

R_0, G_0, B_0 : color coordinates of red, green, and blue defined by NTSC, respectively.

R, G, B : color coordinates of module on 255 gray levels of red, green, and blue, respectively.

R_0 G_0 B_0 : area of triangle defined by R_0, G_0, B_0

R G B: area of triangle defined by R, G, B



6. RELIABILITY TEST ITEM

Test Item	Test Condition	Note
High Temperature Storage Test	60ºC, 240 hours	(1) (2)
Low Temperature Storage Test	-20ºC, 240 hours	
Thermal Shock Storage Test	-25ºC, 0.5hour←→65℃, 0.5hour; 100cycles, 1hour/cycle	
Low Temperature Operation Test	0ºC, 240 hours	
High Temperature & High Humidity Operation Test	50ºC, RH 80%, 240hours	
ESD Test (Operation)	150pF, 330Ω, 1sec/cycle Condition 1 : Contact Discharge, ±8KV Condition 2 : Air Discharge, ±15KV	(1)
Shock (Non-Operating)	210G, 3ms, half sine wave,1 time for each direction of ±X,±Y,±Z	(1)(3)
Vibration (Non-Operating)	1.5G / 10-200-10Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z	(1)(3)

Note (1) criteria : Normal display image with no obvious non-uniformity and no line defect.

Note (2) Evaluation should be tested after storage at room temperature for more than two hour

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

7. PACKING

7.1 MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.

(a) Model Name: **P173ZZZ-BZ1**

(b) Revision: Rev. XX, for example: B1, B2 …etc.

(c) Serial ID: X X X X X X Y M D L N N N N

- Serial No.
- Product Line
- Year, Month, Date
- INNOLUX Internal Use
- Revision
- INNOLUX Internal Use

(d) Production Location: MADE IN XXXX.

(e) UL logo: XXXX especially stands for panel manufactured by INNOLUX satisfying UL requirement.
Marking as follows rule:
TW INX_D Factory =>GEMN
TW INX_C Factory =>
NB INX_NA Factory =>LEOO
NB INX_NB,NC Factory =>VIRO
NB INX_ND Factory =>COCKN
FS INX_A&B building=>CAPG

Serial ID includes the information as below:

(a) Manufactured Date: Year: 0~9, for 2010~2019

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

(b) Revision Code: cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

7.2 CARTON

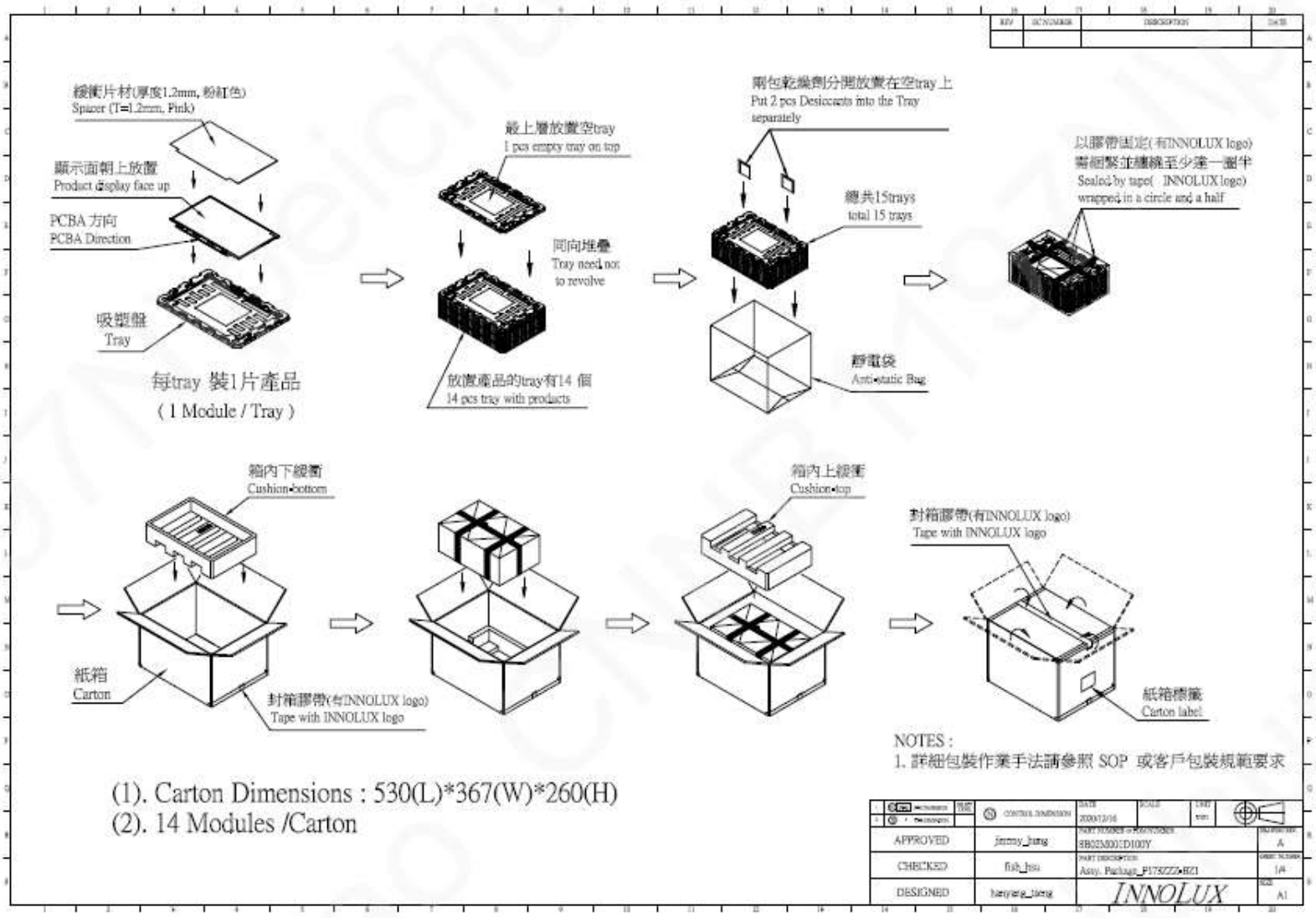


Figure. 7-2 Packing method

PRODUCT SPECIFICATION

7.3 PALLET

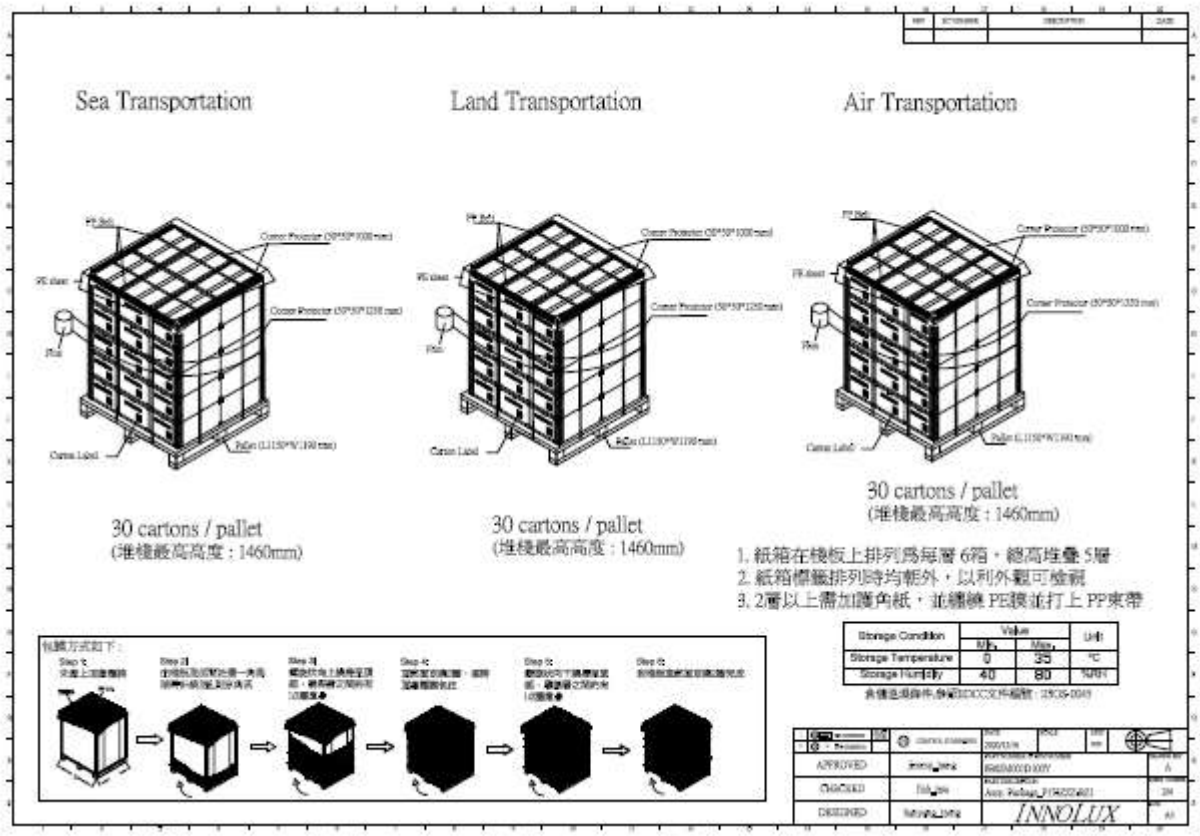


Figure. 7-3 Packing method

8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the LED wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

8.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

(3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

Appendix. EDID DATA STRUCTURE

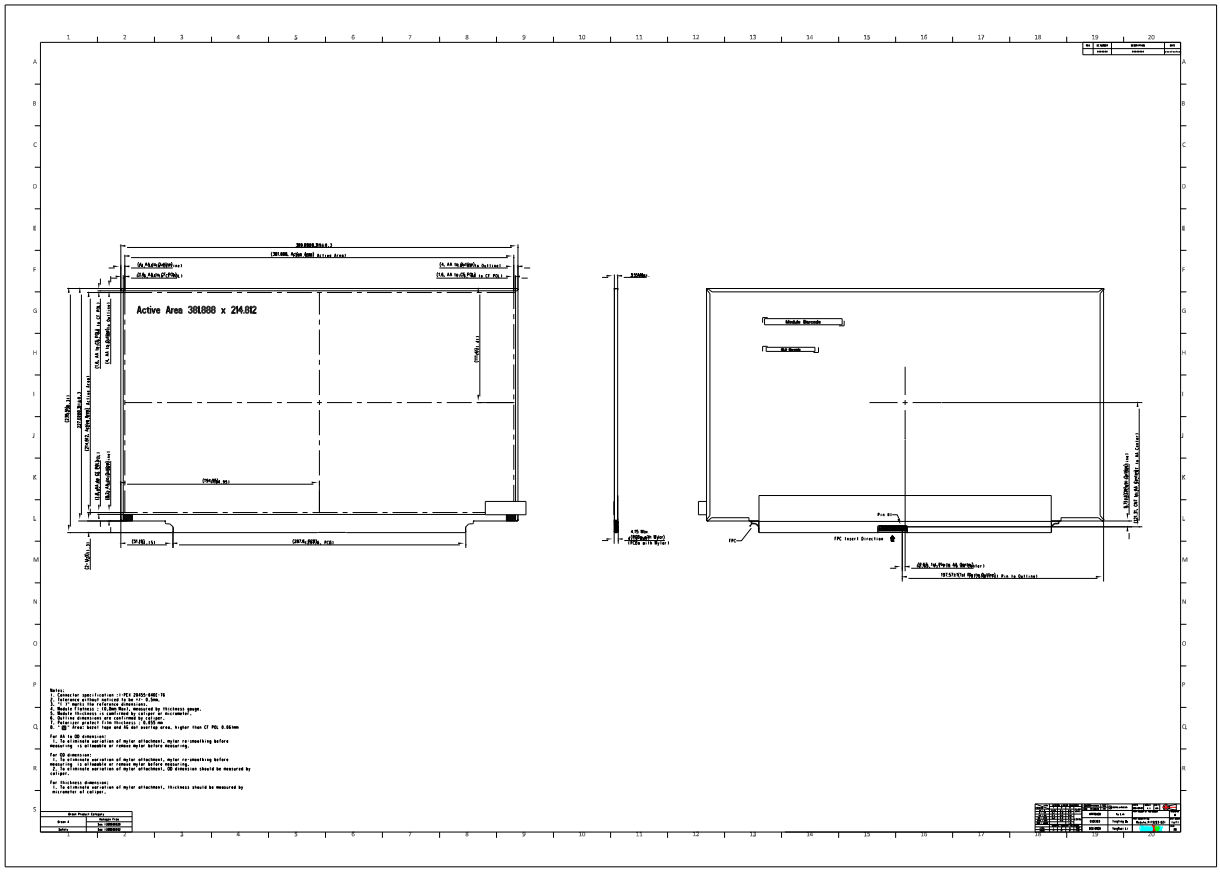
The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPDI standards.

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	00	Header	00	00000000
1	01	Header	FF	11111111
2	02	Header	FF	11111111
3	03	Header	FF	11111111
4	04	Header	FF	11111111
5	05	Header	FF	11111111
6	06	Header	FF	11111111
7	07	Header	00	00000000
8	08	EISA ID manufacturer name ("CMN")	0D	00110000
9	09	EISA ID manufacturer name	AE	10101110
10	0A	ID product code (LSB)	01	00000001
11	0B	ID product code (MSB)	AD	10101101
12	0C	ID S/N (fixed "0")	00	00000000
13	0D	ID S/N (fixed "0")	00	00000000
14	0E	ID S/N (fixed "0")	00	00000000
15	0F	ID S/N (fixed "0")	00	00000000
16	10	Week of manufacture (fixed week code)	2F	00101111
17	11	Year of manufacture (fixed year code)	1E	00011110
18	12	EDID structure version ("1")	01	00000001
19	13	EDID revision ("4")	04	00000100
20	14	Video I/P definition ("Digital")	B5	10110101
21	15	Active area horizontal (“27.9 cm“)	26	00100110
22	16	Active area vertical (“17.4cm“)	15	00010101
23	17	Display Gamma (Gamma = "2.2")	78	01111000
24	18	Feature support ("Active off, RGB Color")	02	00000010
25	19	Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0	4F	01001111
26	1A	Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0	B5	10110101
27	1B	Rx=0.644	AE	10101110
28	1C	Ry=0.324	4F	01001111
29	1D	Gx=0.306	3E	00111110
30	1E	Gy=0.609	B1	10110001
31	1F	Bx=0.153	27	00100111
32	20	By=0.063	0D	00001101
33	21	Wx=0.315	50	01010000
34	22	Wy=0.327	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	Manufacturer's reserved timings	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001

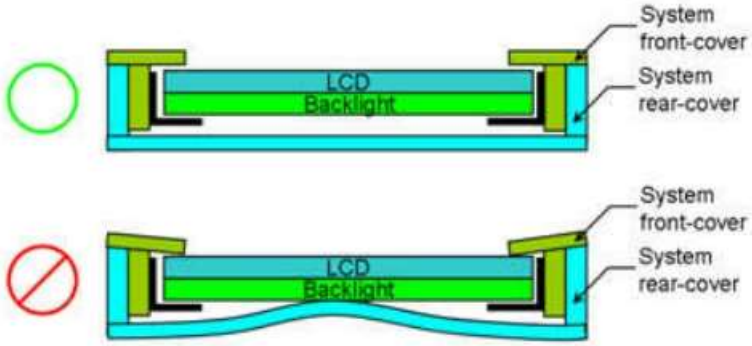
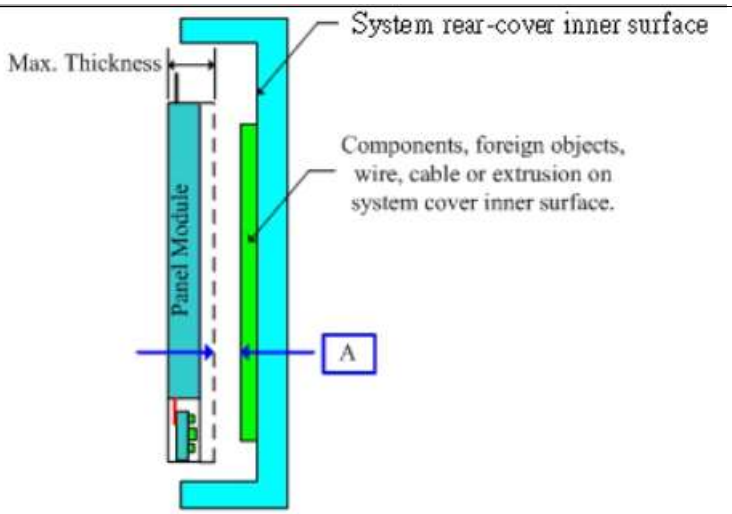
42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock ("180.77MHz")	4D	01001101
55	37	# 1 Pixel clock (hex LSB first)	D1	11010001
56	38	# 1 H active ("2160")	00	00000000
57	39	# 1 H blank ("44")	A0	10100000
58	3A	# 1 H active : H blank	F0	11110000
59	3B	# 1 V active ("1350")	70	01110000
60	3C	# 1 V blank ("17")	3E	00111110
61	3D	# 1 V active : V blank	80	10000000
62	3E	# 1 H sync offset ("16")	30	00110000
63	3F	# 1 H sync pulse width ("16")	20	00100000
64	40	# 1 V sync offset : V sync pulse width ("8 : 1")	35	00110101
65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width	00	00000000
66	42	# 1 H image size (“279 mm“)	7D	01111101
67	43	# 1 V image size (“174 mm“)	D6	11010110
68	44	# 1 H image size : V image size	10	00010000
69	45	# 1 H boarder ("0")	00	00000000
70	46	# 1 V boarder ("0")	00	00000000
71	47	# 1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives	18	00011000
72	48	Detailed timing description # 2	00	00000000
73	49	# 2 Flag	00	00000000
74	4A	# 2 Reserved	00	00000000
75	4B	# 2 ASCII string Model name	00	00000000
76	4C	# 2 Flag	00	00000000
77	4D	# 2 Character of Model name ("")	00	00000000
78	4E	# 2 Character of Model name ("")	00	00000000
79	4F	# 2 Character of Model name ("")	00	00000000
80	50	# 2 Character of Model name ("")	00	00000000
81	51	# 2 Character of Model name ("")	00	00000000
82	52	# 2 Character of Model name ("")	00	00000000
83	53	# 2 Character of Model name ("")	00	00000000
84	54	# 2 Character of Model name ("")	00	00000000
85	55	# 2 Character of Model name ("")	00	00000000
86	56	# 2 Character of Model name ("")	00	00000000
87	57	# 2 Character of Model name ("")	00	00000000

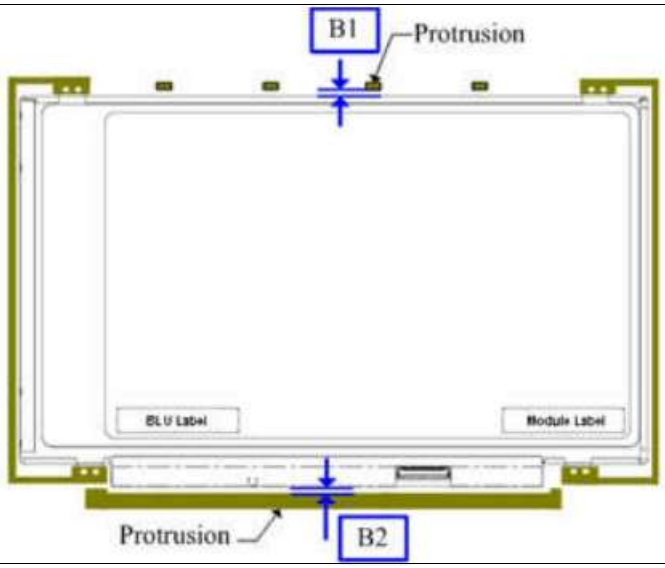
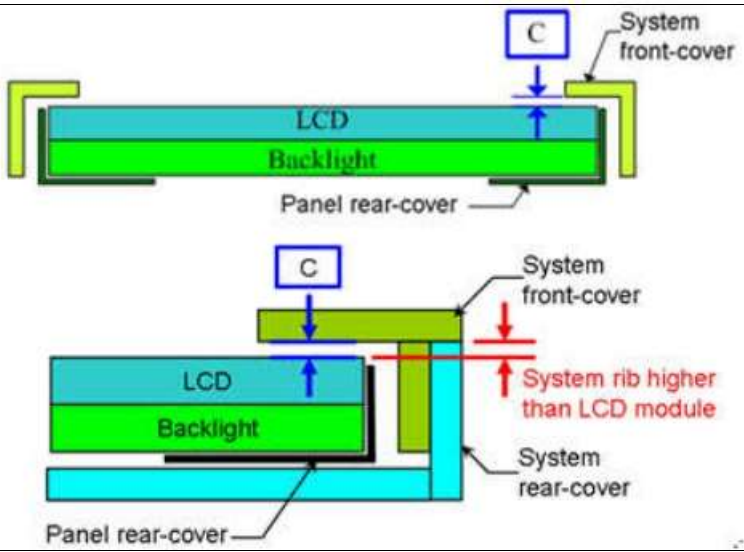
88	58	# 2 New line character indicates end of ASCII string	00	00000000
89	59	# 2 Padding with "Blank" character	00	00000000
90	5A	Detailed timing description # 3	00	00000000
91	5B	# 3 Flag	00	00000000
92	5C	# 3 Reserved	00	00000000
93	5D	# 3 ASCII string Vendor	00	00000000
94	5E	# 3 Flag	00	00000000
95	5F	# 3 Character of string ("")	00	00000000
96	60	# 3 Character of string ("")	00	00000000
97	61	# 3 Character of string ("")	00	00000000
98	62	# 3 New line character indicates end of ASCII string	00	00000000
99	63	# 3 Padding with "Blank" character	00	00000000
100	64	# 3 Padding with "Blank" character	00	00000000
101	65	# 3 Padding with "Blank" character	00	00000000
102	66	# 3 Padding with "Blank" character	00	00000000
103	67	# 3 Padding with "Blank" character	00	00000000
104	68	# 3 Padding with "Blank" character	00	00000000
105	69	# 3 Padding with "Blank" character	00	00000000
106	6A	# 3 Padding with "Blank" character	00	00000000
107	6B	# 3 Padding with "Blank" character	00	00000000
108	6C	Detailed timing description # 4	00	00000000
109	6D	# 4 Flag	00	00000000
110	6E	# 4 Reserved	00	00000000
111	6F	# 4 ASCII string Model Name	FE	11111110
112	70	# 4 Flag	00	00000000
113	71	# 4 1st character of name (“P”)	50	01010000
114	72	# 4 2nd character of name (“1”)	31	00110001
115	73	# 4 3rd character of name (“3”)	37	00110111
116	74	# 4 4th character of name (“0”)	33	00110011
117	75	# 4 5th character of name (“Z”)	5A	01011010
118	76	# 4 6th character of name (“F”)	5A	01011010
119	77	# 4 7th character of name (“Z”)	5A	01011010
120	78	# 4 8th character of name (“-”)	2D	00101101
121	79	# 4 9th character of name (“B”)	42	01000010
122	7A	# 4 10th character of name (“H”)	5A	01011010
123	7B	# 4 11th character of name (“2”)	31	00110001
124	7C	# 4 New line character indicates end of ASCII string	0A	00001010
125	7D	# 4 Padding with "Blank" character	20	00100000
126	7E	Extension flag	01	00000001
127	7F	Checksum	11	00010001

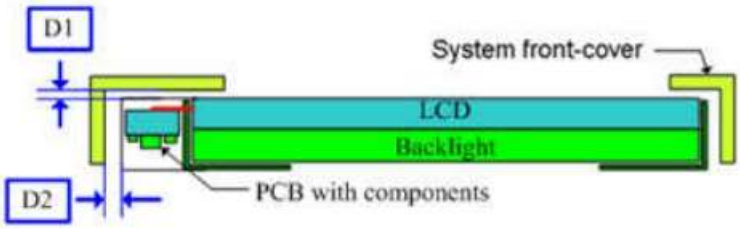
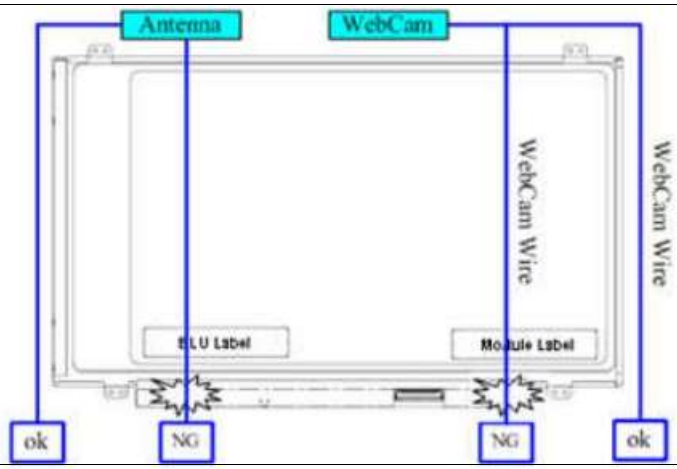
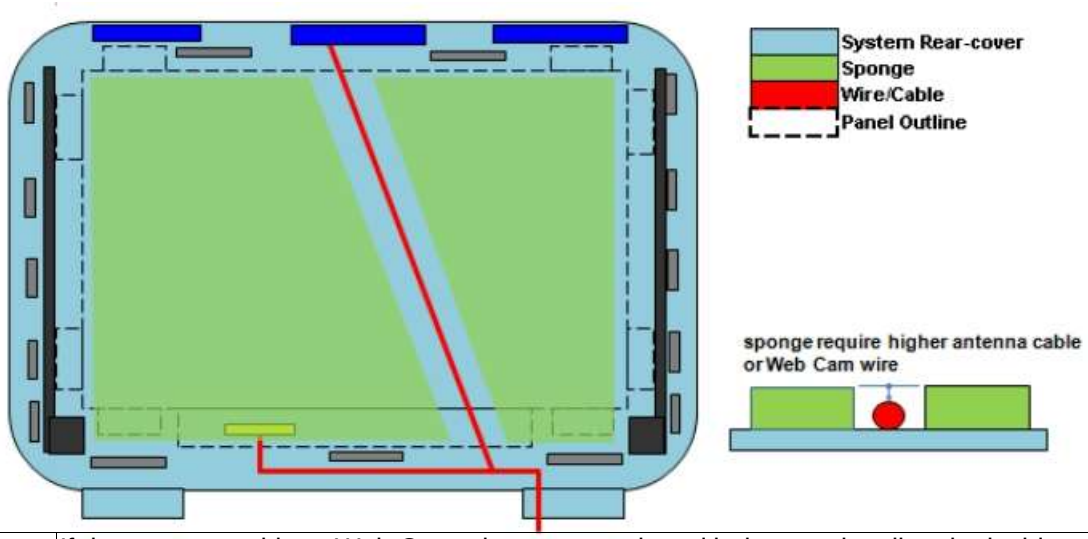
Appendix. OUTLINE DRAWING

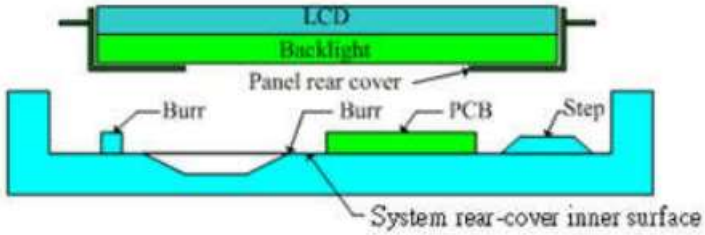
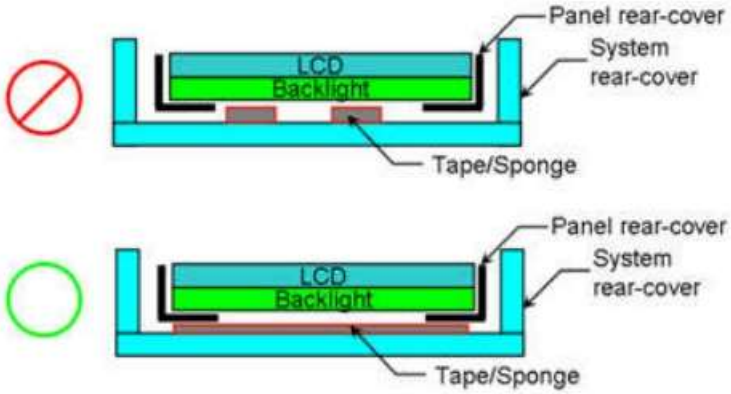
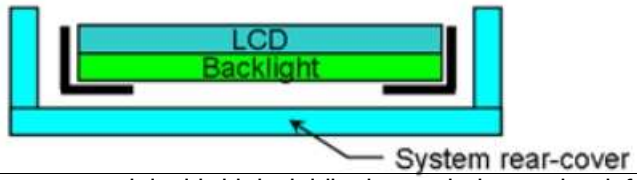
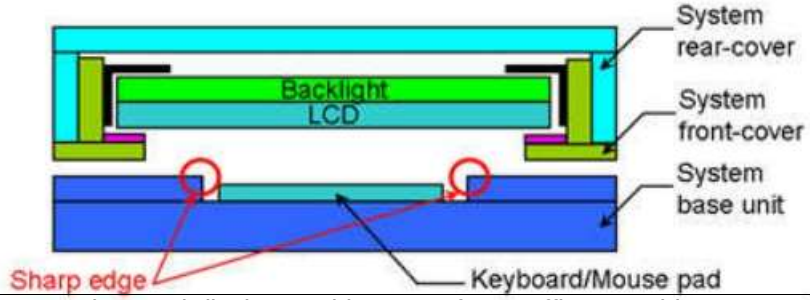


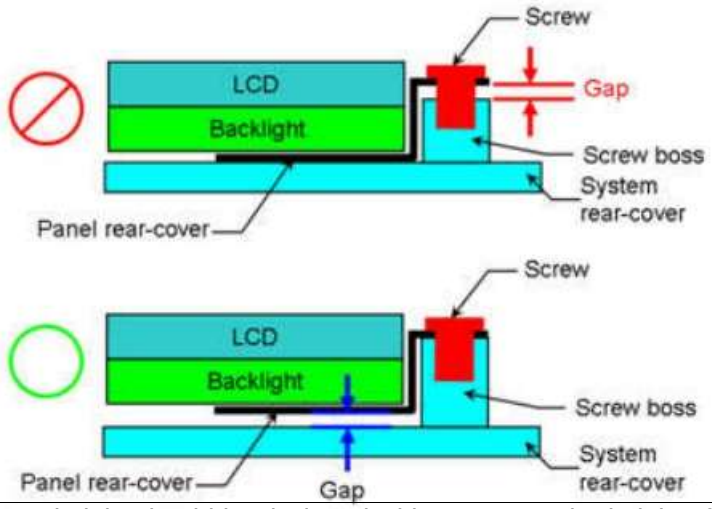
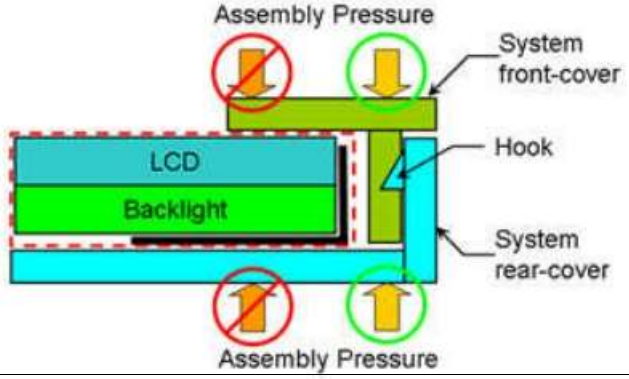
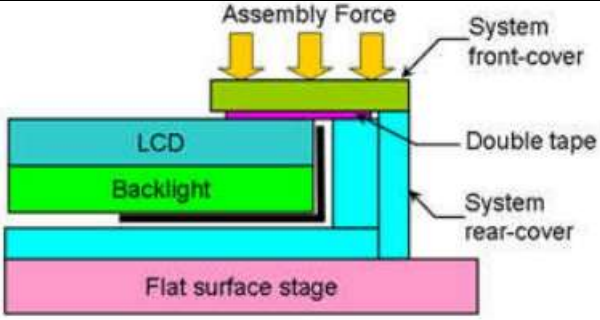
Appendix. SYSTEM COVER DESIGN GUIDANCE **Ver.7**

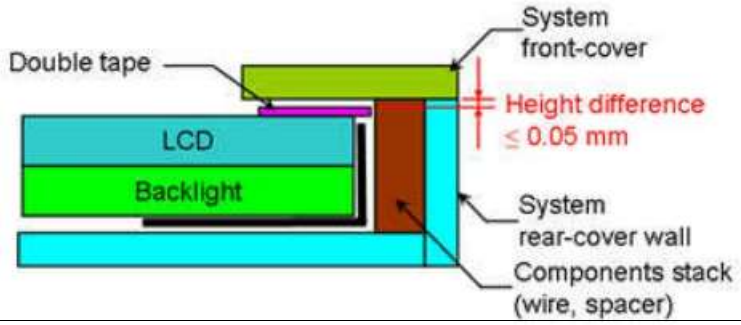
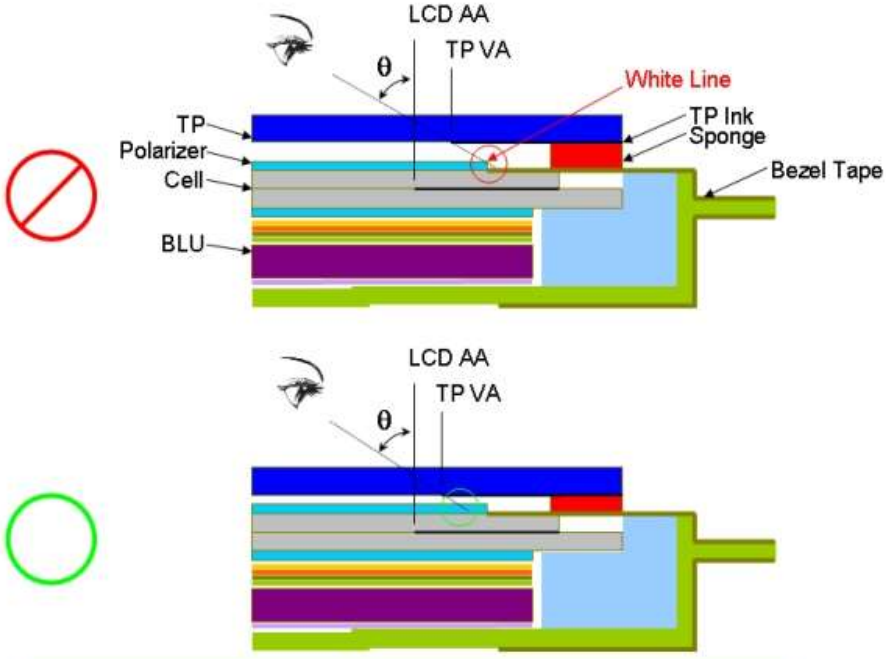
0.	**Permanent deformation of system cover after reliability test**
	
Definition	System cover including front and rear cover may deform during reliability test. Permanent deformation of system front and rear cover after reliability test should not interfere with panel. Because it may cause issues such as pooling, abnormal display, white spot, and also cell crack. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
1.	**Design gap A between panel & any components on system rear-cover**
	
Definition	Gap between panel's maximum thickness boundary & system's inner surface components such as wire, cable, extrusion is needed for preventing from backpack or pogo test fail. Because zero gap or interference may cause stress concentration. Issues such as pooling, abnormal display, white spot, and cell crack may occur. Maximum flatness of panel and system rear-cover should be taken into account for gap design. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
2	**Design gap B1 & B2 between panel & protrusions**

<table>
<tr><td colspan="2"> 
</td></tr>
<tr><td>Definition</td><td>Gap between panel & protrusions is needed to prevent shock test failure. Because protrusions with small gap may hit panel during the test. Issue such as cell crack, abnormal display may occur.
The gap should be large enough to absorb the maximum displacement during the test. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.</td></tr>
<tr><td>3</td><td>Design gap C between system front-cover & panel surface.</td></tr>
<tr><td colspan="2"> 
</td></tr>
<tr><td>Definition</td><td>Gap between system front-cover & panel surface is needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near system font-cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test, or during pooling inspection procedure.
To remain sufficient gap, design with system rib higher than maximum panel thickness is recommended.
Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.</td></tr>
<tr><td>4</td><td>Design gap D1 & D2 between system front-cover & PCB Assembly.</td></tr>
</table>

	
Definition	Same as point 2 and 3, but focus on PCBA side.
5	**Interference examination of antenna cable and WebCam wire**
	
Definition	Antenna cable or WebCam wire should not overlap with panel outline. Because issue such as abnormal display & white spot after backpack test, hinge test, twist test or pogo test may occur. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
6	**Interference examination of antenna cable and Web Cam wire**
	
	If the antenna cable or Web Cam wire must overlap with the panel outline, both sides of the antenna cable or Web Cam wire must have a sponge(Sponge material can not contain NH3) and sponge require higher antenna cable or Web Cam wire.(Antenna cable or Web Cam wire should not overlap with TCON,COF/FPC,Driver IC) Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer

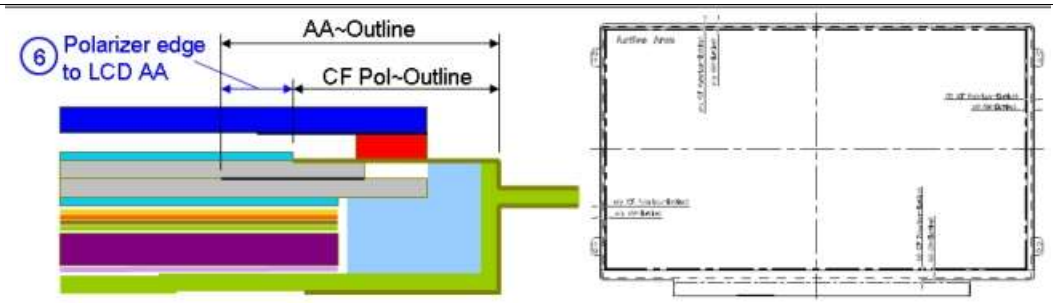
	reference.
7	**System rear-cover inner surface examination**
	
Definition	Burr at logo edge, steps, protrusions or PCB board may cause stress concentration. White spot or glass broken issue may occur during reliability test.
8	**Tape/sponge design on system inner surface**
	
Definition	To prevent abnormal display & white spot after scuffing test, hinge test, pogo test, backpack test, tape/sponge should be well covered under panel rear-cover. Because tape/sponge in separate location may act as pressure concentration location.
9	**Material used for system rear-cover**
	
Definition	System rear-cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test, or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Pooling issue may occur because screw's boss positioning for module's bracket are deformed during open-close test. Solid structure design of system rear-cover may also influence the rigidity of system rear-cover. The deformation of system rear-cover should not caused interference.
10	**System base unit design near keyboard and mouse pad**
	
Definition	To prevent abnormal display & white spot after scuffing test, hinge test, pogo test, backpack

	test, sharp edge design in keyboard surface may damage panel during the test. We suggest to use slope edge design, or to reduce the thickness difference of keyboard/mouse pad from the nearby surface.
11	**Screw boss height design**
	
Definition	Screw boss height should be designed with respect to the height of bracket bottom surface to panel bottom surface + flatness change of panel itself. Because gap will exist between screw boss and bracket, if the screw boss height is smaller. As result while fastening screw, bracket will deformed and pooling issue may occur.
12	**Assembly SOP examination for system front-cover with Hook design**
	
Definition	To prevent panel crack during system front-cover assembly process with hook design, it is not recommended to press panel or any location that related directly to the panel.
13	**Assembly SOP examination for system front-cover with Double tape design**
	
Definition	To prevent panel crack during system front-cover assembly process with double tape design, it is only allowed to give slight pressure (MAX 3 Kgf/50mm2) with large contact area. This can help to distribute the stress and prevent stress concentration. We also suggest putting the system on a flat surface stage to prevent unequal stress distribution during the

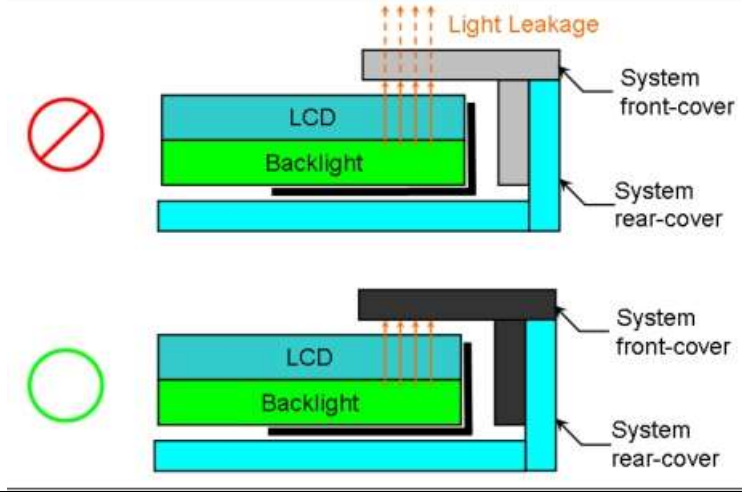
	assembly.
14	**System front-cover assembly reference with Double tape design**
	
Definition	To prevent system front-cover peeling at double tape contact area, Height difference between system front-cover assembly reference such as wall or components stack (wire, spacer) and double tape top surface must be less than 0.05mm.
15	**Touch Application : TP and LCD Module Combination for White Line Prevention**
	

Parameter consideration for White Line Issue :	
1	TP VA to LCD AA distance
2	TP Assembly tolerance
3	TP Ink Printing tolerance
4	Sponge thickness and tolerance
5	Inspection/Viewing Angle specification
6	Polarizer edge to LCD AA distance and tolerance

Polarizer edge to LCD AA distance can be derived by “AA~Outline” – “CF Pol~Outline” with respect to INX 2D Outline Drawing on each side.

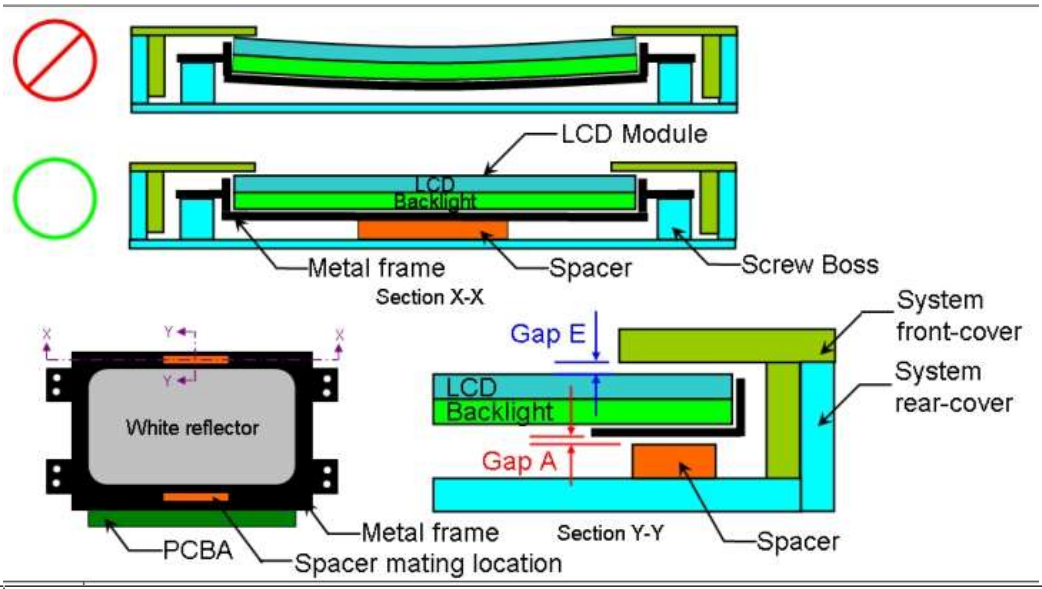


Definition	For using in Touch Application: to prevent White Line appears between TP and LCD module combination, the maximum inspection angle location must not fall onto LCD polarizer edge, otherwise light line near edge of polarizer will be appear. Parameters such as TP VA to LCD AA distance, TP assembly tolerance, TP Ink printing tolerance, Sponge thickness and tolerance, and Maximum Inspection/Viewing Angle, must be considered with respect to LCD module's Polarizer edge location and tolerance. This consideration must be taken at all four edges separately. The goal is to find parameters combination that allow maximum inspection angle falls inside polarizer black margin area. Note: Information for Polarizer edge location and its tolerance can be derived from INX 2D Outline Drawing ("AA ~Outline" - "CF Pol~Outline"). Note: Please feel free to contact INX FAE Engineer. By providing value of parameters above on each side, we can help to verify and pass the white line risk assessment for customer reference.
16	**Color of system front-cover material**



Definition	To prevent light leakage is seen at system front-cover due to material transparency, we suggest using dark color material (black) for system front-cover design.
17	**Inspection spec of gap E between system front-cover to LCD module surface**

PRODUCT SPECIFICATION

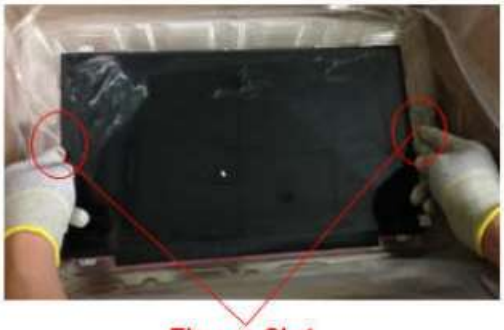


Definition	To maintain gap E (gap of system front-cover to LCD module) in its inspection spec, especially at location with maximum LCD deformation (center of LCD length), we recommend adding spacer with design gap A smaller or equal to gap E. The allowable spacer mating location is on module metal frame outside LCD Active-Area. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.

PRODUCT SPECIFICATION

Appendix. LCD MODULE HANDLING MANUAL

Purpose	• **This SOP is prepared to prevent panel dysfunction possibility through incorrect handling procedure.** • **This manual provides guide in unpacking and handling steps.** • **Any person which may contact / related with panel, should follow guide stated in this manual to prevent panel loss.**
1.	**Unpacking**
	
2.	**Panel Lifting**



Use slots at both sides for finger insertion.
Handle panel upward with care.

3.	Do and Don't

Do :

- Handle with both hands.
- Handle panel at left and right edge.

Don't :

- Lifting with one hand.

- Handle at PCBA side.

Don't :

- Stack panels.

- Press panel.

Don't :

- Put foreign stuff onto panel

- Put foreign stuff under panel

Don't :

- Paste any material unto white reflector sheet

Don't :

- Pull / Push white reflector sheet

Don't :

- Hold at panel corner.

Don't :

- Twist panel.

Do :

- Hold panel at top edge while inserting connector.

Don't :

- Press white reflector sheet while inserting connector.

Do :

- Remove panel protector film starts from pull tape

Don't :

- Remove panel protector film From film another side.

Don't :

- Touch or Press PCBA Area.