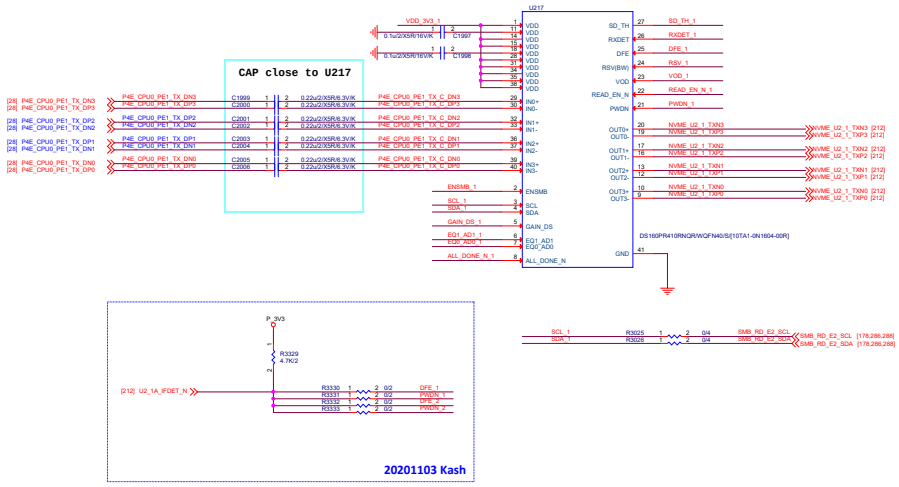
CPU0 PCIE PORT 1 TX [0:3]



NVMe U2_1 SLOT TX [0:3]

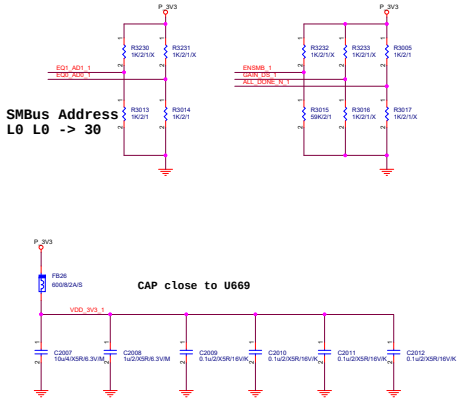


Table 1. 4-Level Control Pin Settings

Level	Settings
L0	1 kΩ to GND
L1	13 kΩ to GND
L2	F (Float)
L3	59 kΩ to GND

Hardware Strapping setting

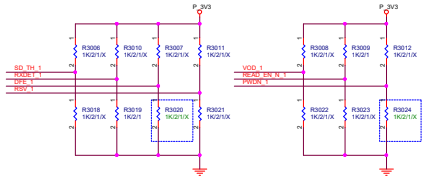
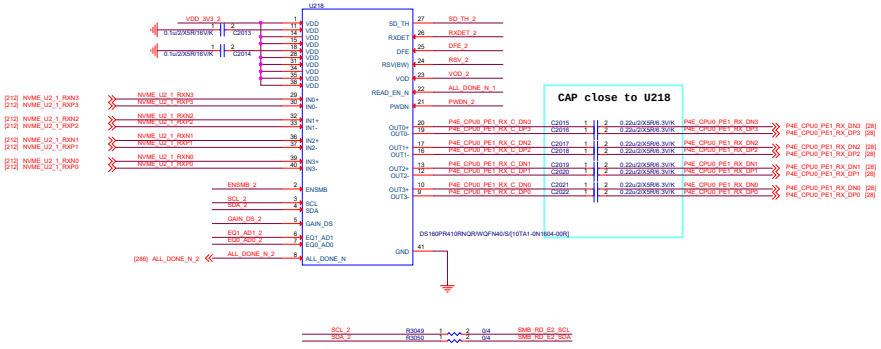


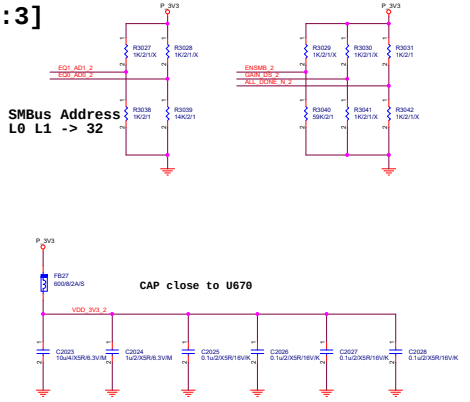
Table 2. SMBUS/I2C Slave Address Settings

EQ1_ADDR1	EQ0_ADDR0	Address (Dec)	Address (Hex)
L0	L0	48	30
L0	L1	50	32
L0	L2	52	34
L0	L3	54	36
L1	L0	56	38
L1	L1	58	3A
L1	L2	60	3C
L1	L3	62	3E
L2	L0	64	40
L2	L1	66	42
L2	L2	68	44
L2	L3	70	46
L3	L0	72	48
L3	L1	74	4A
L3	L2	76	4C
L3	L3	78	4E

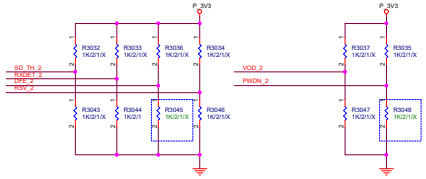
NVMe U2_1 SLOT RX [0:3]



CPU0 PCIE PORT 1 RX [0:3]

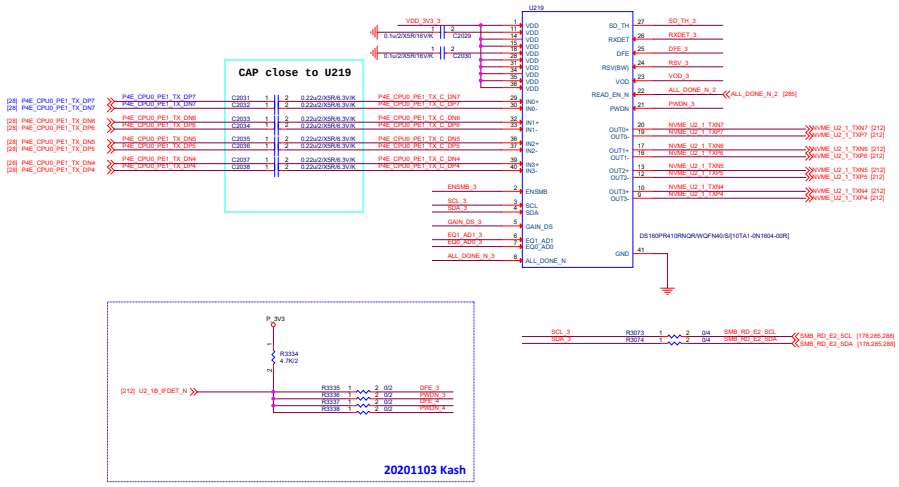


Hardware Strapping setting

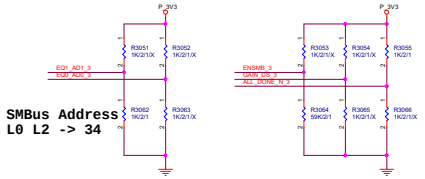


Title	CONN_FP SIGNAL BUFFER		
Size D	Document Number MY62-EX0		Rev 1.1
Date: Thursday, June 16, 2022	Sheet 285 of 300		

CPU0 PCIE PORT 1 TX [4:7]



NVMe U2_1 SLOT TX [4:7]



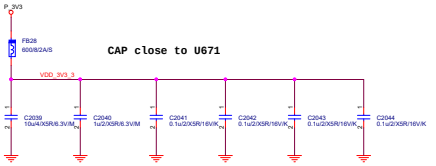


Table 1. 4-Level Control Pin Settings

Level	Settings
L0	1 kΩ to GND
L1	13 kΩ to GND
L2	F (Float)
L3	59 kΩ to GND

Hardware Strapping setting

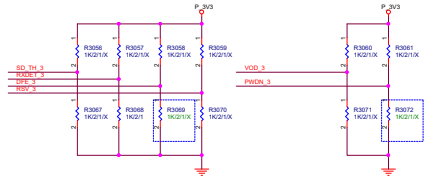
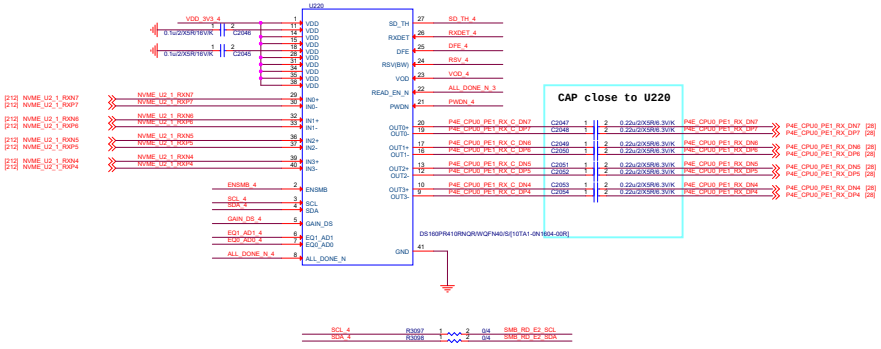


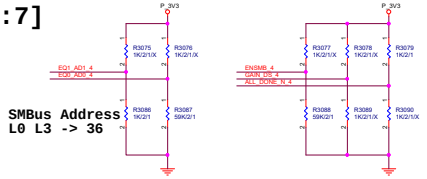
Table 2. SMBUS/I2C Slave Address Settings

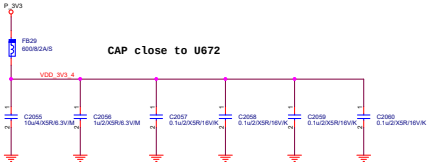
EQ1_ADDR1	EQ0_ADDR0	Address (Dec)	Address (Hex)
L0	L0	48	30
L0	L1	50	32
L0	L2	52	34
L0	L3	54	36
L1	L0	56	38
L1	L1	58	3A
L1	L2	60	3C
L1	L3	62	3E
L2	L0	64	40
L2	L1	66	42
L2	L2	68	44
L2	L3	70	46
L3	L0	72	48
L3	L1	74	4A
L3	L2	76	4C
L3	L3	78	4E

NVMe U2_1 SLOT RX [4:7]

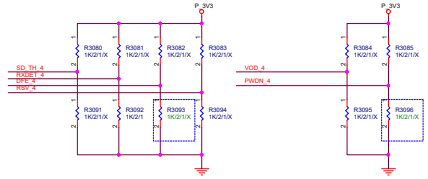


CPU0 PCIE PORT 1 RX [4:7]





Hardware Strapping setting



Title	CONN_FP SIGNAL BUFFER		
Size D	Document Number MY62-EX0		Rev 1.1
Date: Thursday, June 16, 2022	Sheet 288 of 300		