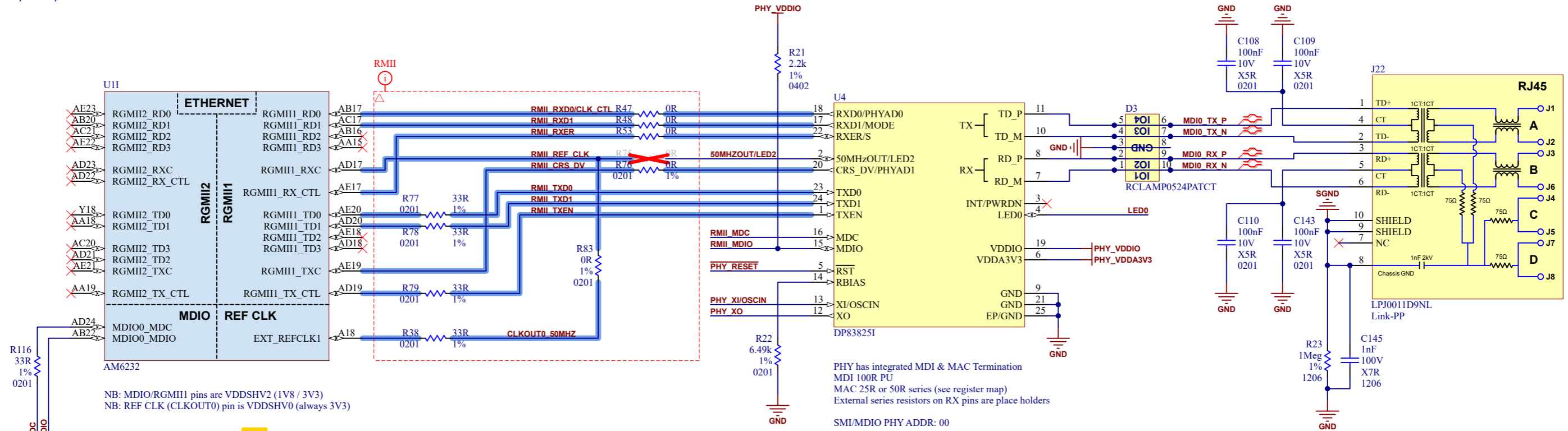


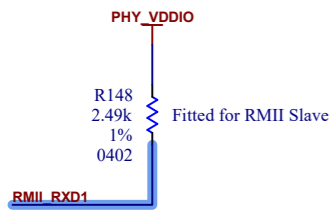
Ethernet, RJ45, PHY Connections



NB: MDIO/RGMI1 pins are VDDSHV2 (1V8 / 3V3)
 NB: REF CLK (CLKOUT0) pin is VDDSHV0 (always 3V3)

PHY has integrated MDI & MAC Termination
 MDI 100R PU
 MAC 25R or 50R series (see register map)
 External series resistors on RX pins are place holders
 SMI/MDIO PHY ADDR: 00

Strapping / Debug LEDs



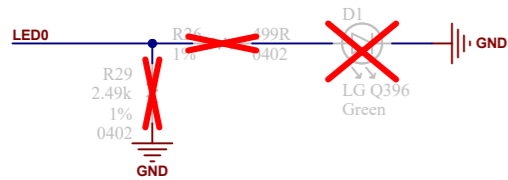
PHY Address: RX_D0/CRS_DV
 Internal pull-down sets default as 00

RMII MAC Mode: RX_D1
 Internal pull-down sets default as 0
 0: RMII Master Mode
 1: RMII Slave Mode

RMII MAC Mode: 50MHzOut/LED2
 Internal pull-down sets default as 0
 0: Pin 20 configured as CRS_DV
 1: Pin 20 configured as RX_DV (RMII Repeater Mode)

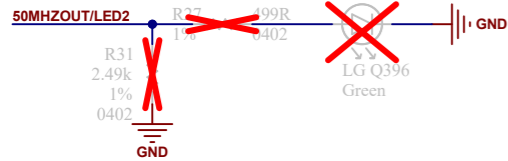
Auto Negotiation: RX_ER
 Internal pull-down sets default as 0
 0: Auto MDIX Enabled
 1: Auto MDIX Disabled

Auto Negotiation: LED0
 Internal pull-down sets default as 0
 0: Auto Negotiation Enabled
 1: Auto Negotiation Disabled. Force Mode 100M enabled



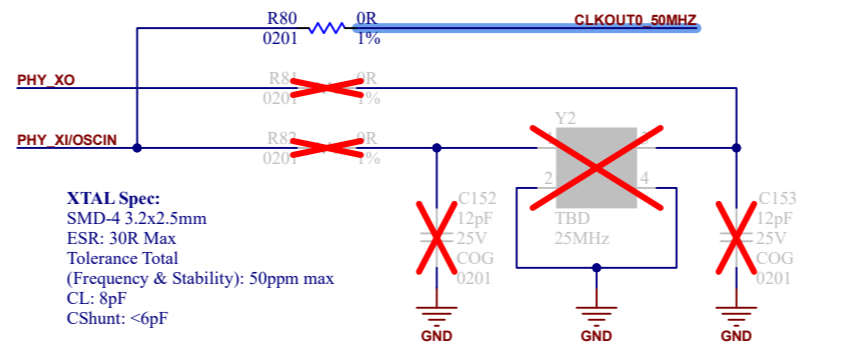
LED0/2 default function
 LED0: Activity & Link Status
 LED2: RX/TX Activity
 See: IO_CFG_Register
 See: LEDCFG_Register

Although LED_1 exists in register map
 no pin is available on DP83825i



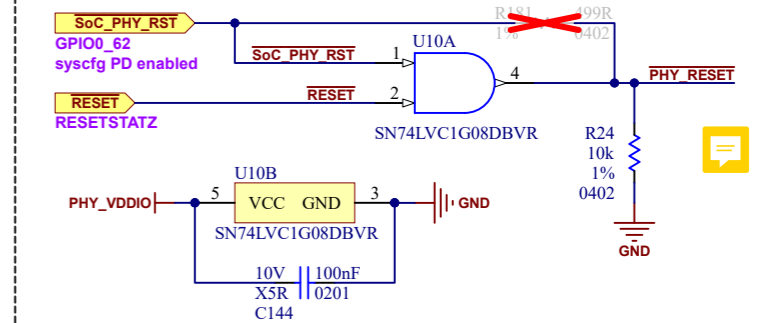
NB: typo in Table 86 DP83825i Datasheet
 LED_2 Control: Selects the source for LED_2

PHY Clock Input

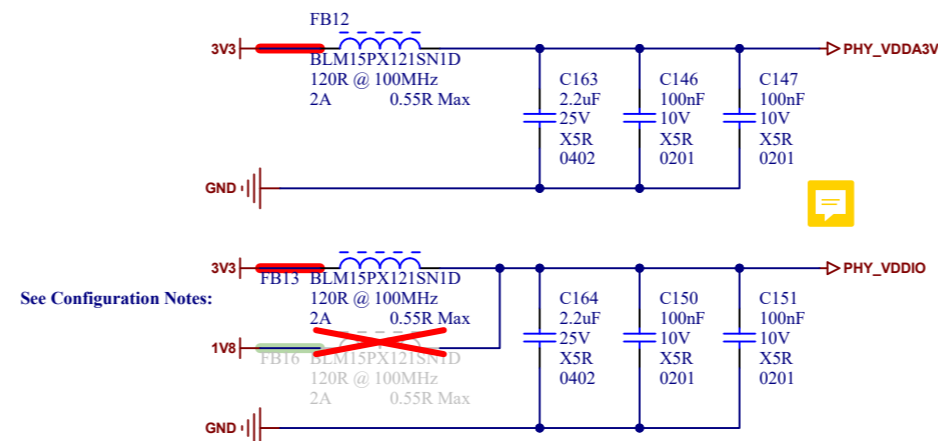


PHY Reset

AND gate must support level translation for 1V8 VDDIO application
 As XI clock is not guaranteed during power ramp,
 an additional reset pulse may be required from Sitara after power-up



PHY Decoupling



PHY Configuration Notes

- Option 1: PHY Slave, AM6232 EXT_REFCLK1/CLKOUT0 source**
 CLKOUT0 to be configured for 50MHz, 3V3 operation, +50ppm total required
 PHY_XO should be floating in this configuration
 In this configuration VDDIO must be 3V3, as CLKOUT0 is always 3V3
 PHY configured as RMII slave and CLKOUT0 routed back to MAC_REF_CLK input
- Option 2: 25MHz XTAL**
 PHY may be configured as RMII master or slave
 -> See strapping config
 In this configuration VDDIO may be 3V3 or 1V8
 -> PHY_VDDIO setting must follow VDDSHV2 setting