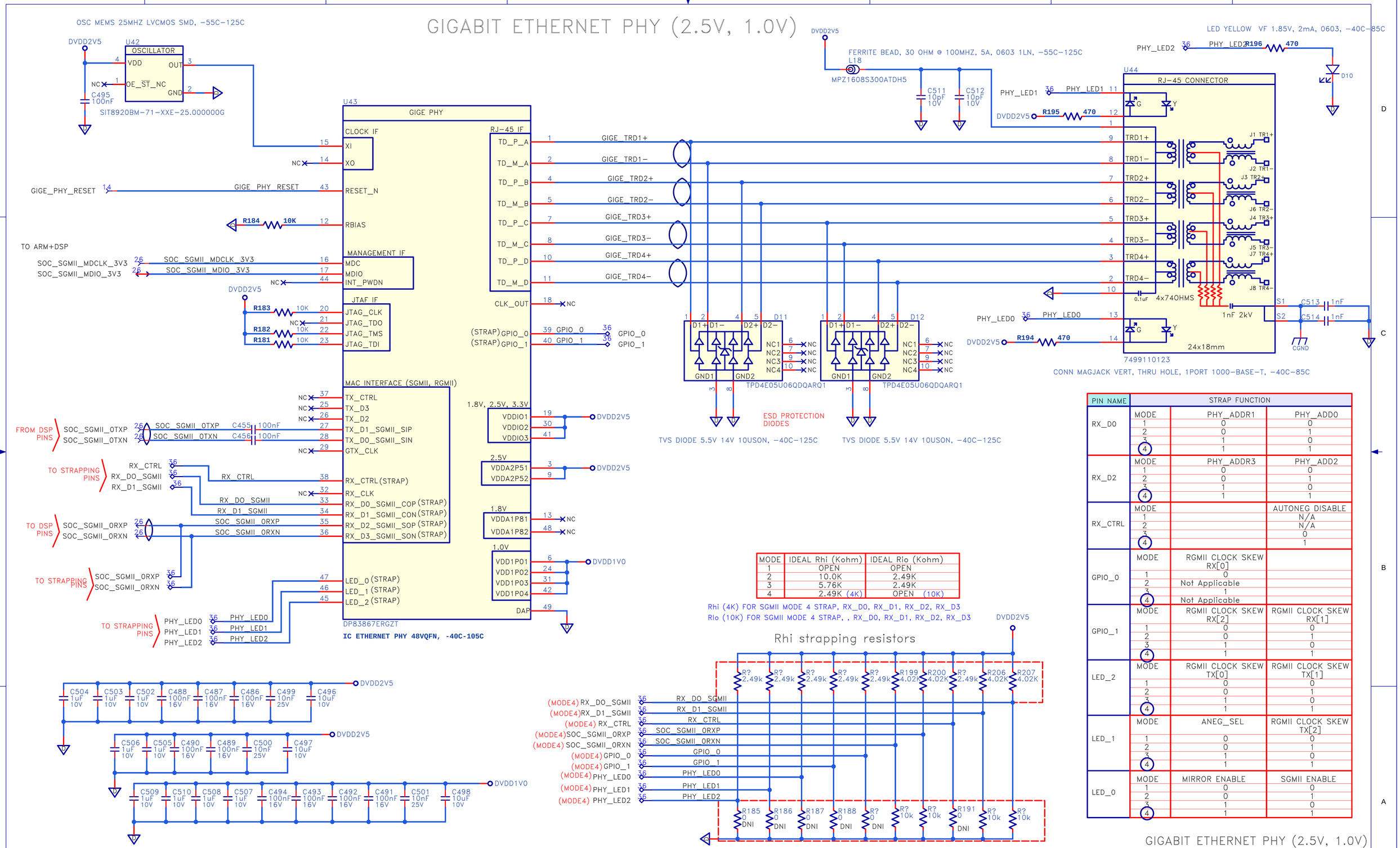
GIGABIT ETHERNET PHY (2.5V, 1.0V)



MODE	IDEAL Rhi (Kohm)	IDEAL Rio (Kohm)
1	OPEN	OPEN
2	10.0K	2.49K
3	5.76K	2.49K
4	2.49K (4K)	OPEN (10K)

Rhi (4K) FOR SGMII MODE 4 STRAP, RX_D0, RX_D1, RX_D2, RX_D3
Rio (10K) FOR SGMII MODE 4 STRAP, , RX_D0, RX_D1, RX_D2, RX_D3

PIN NAME	STRAP FUNCTION		
RX_D0	MODE	PHY_ADDR1	PHY_ADD0
	1	0	0
	2	0	1
	3	1	0
	4	1	1
RX_D2	MODE	PHY_ADDR3	PHY_ADD2
	1	0	0
	2	0	1
	3	1	0
	4	1	1
RX_CTRL	MODE		AUTONEG DISABLE
	1		N/A
	2		N/A
	3		0
	4		1
GPIO_0	MODE	RGMII CLOCK SKEW RX[0]	
	1	0	
	2	Not Applicable	
	3	1	
	4	Not Applicable	
GPIO_1	MODE	RGMII CLOCK SKEW RX[2]	RGMII CLOCK SKEW RX[1]
	1	0	0
	2	0	1
	3	1	0
	4	1	1
LED_2	MODE	RGMII CLOCK SKEW TX[0]	RGMII CLOCK SKEW TX[1]
	1	0	0
	2	0	1
	3	1	0
	4	1	1
LED_1	MODE	ANEG_SEL	RGMII CLOCK SKEW TX[2]
	1	0	0
	2	0	1
	3	1	0
	4	1	1
LED_0	MODE	MIRROR ENABLE	SGMII ENABLE
	1	0	0
	2	0	1
	3	1	0
	4	1	1

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SIZE	FSCM NO.	DWG NO.
D	12934	80110000
Rev AAAA	10/22/2018:09:31	SHEET 36 OF 49

DISTRIBUTION STATEMENT
NEEDS COMPLIANCE