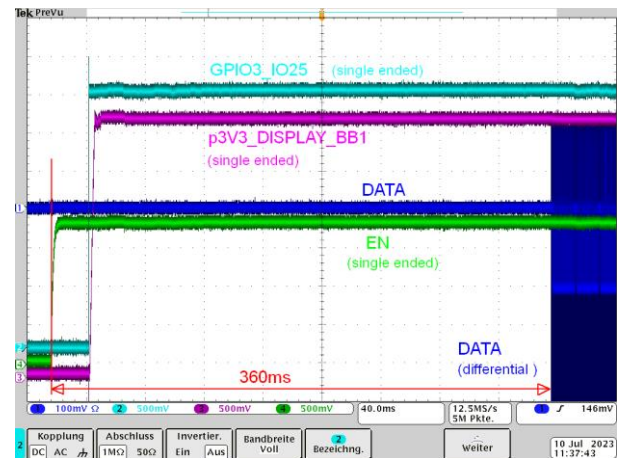
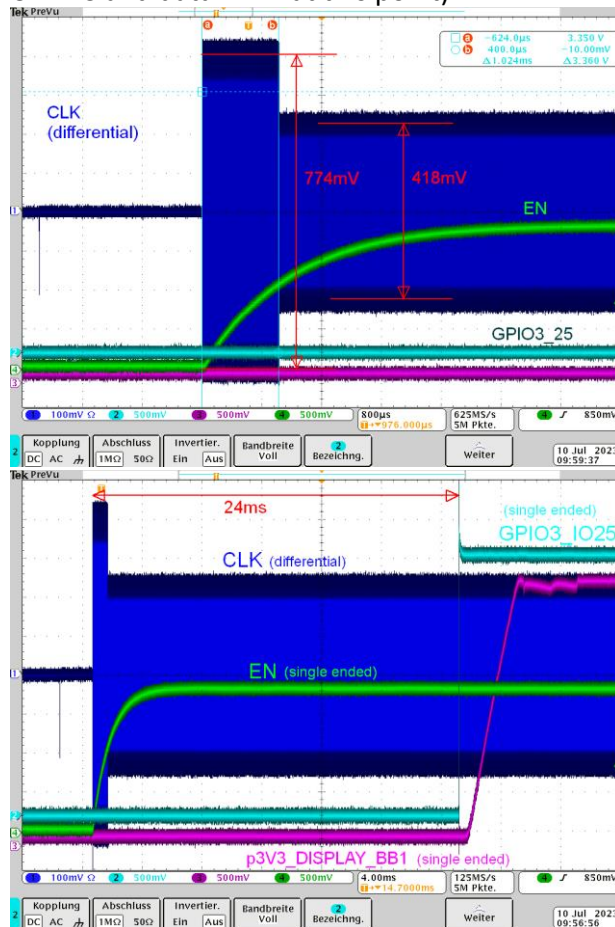


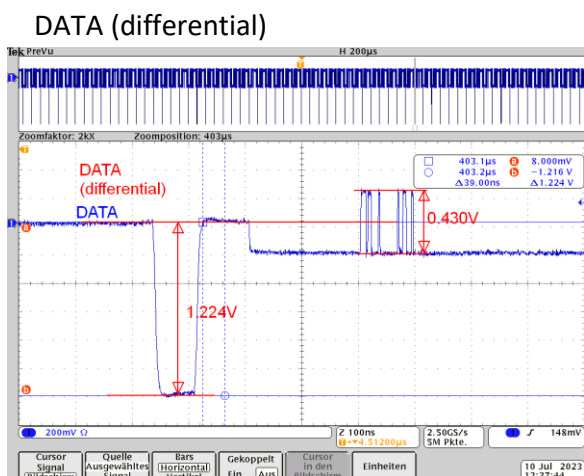
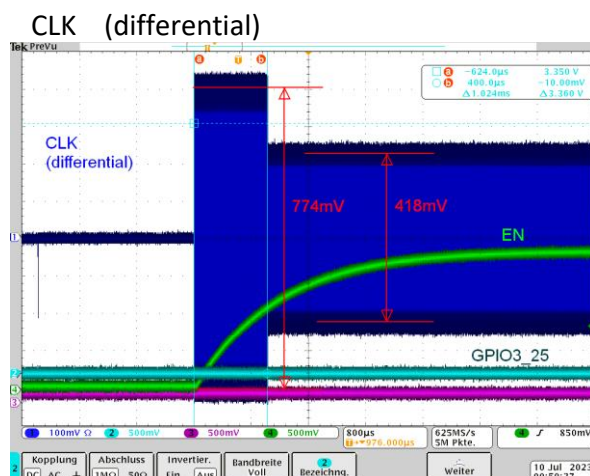
1.- Measure **DSI CLK**, **DSI data**, **DSI83 EN pin** and the **LCD ON gpio3 25** (this GPIO is set high on right after finishing the DSI83 I2C configuration, as per the DSI83 datasheet the DSI must be in CLK-HS and data-LP11 at this point).



- Clock signal is present before enable signal. Clock signal has two different levels (peek to peek).

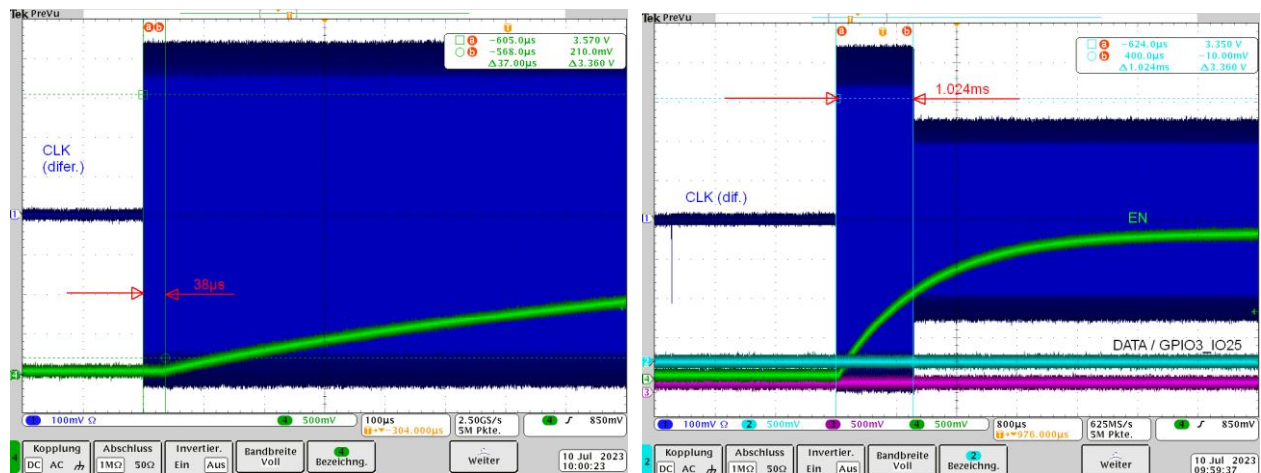
2.- The TI support group shared with us the following considerations to analyse the measured signals: When DSI-CLK and Data are differential, HS mode peak to peak voltage is 140mV min, 200mV nominal, and 270mV max.

If they are single ended, HS mode peak-to-peak voltage is 280mV min, 400mV nominal, and 540mV max. LP11 mode is just a constant high at 1.2V. Can you confirm if this is what you are reading? The data lanes must stay in LP11 mode while EN pin ramps from low to high.



CLK (dif.) : 418mV peek to peek (short : 774mV p2p) DATA (dif.) : 430mV peek to peek ( 1224mV peek to low)

3.- Could you please share with us measurements while DSI83-EN ramps from low to high and measurements where it can be seen a longer section?



4.- Using the binaries provided today, could you determine if one of those is more stable than the other? Or if check if the issue occurs sporadically without a pattern in both?

- error rate between ~ 1/50 and ~1/70

- both versions are the same. Two events can occur in quick succession or at a greater distance. (No pattern recognizable)

