Schematic Review Form

Customer/Project

Pin #	Name	Info	Violations	Description
1	IN_D2p			Channel 2 differential input
2	IN_D2n			Channel 2 differential input
4	IN_D1p			Channel 1 differential input
5	IN_D1n			Channel 1 differential input
6	IN_D0P			Channel 0 differential input
7	IN_D0n			Channel 0 differential input
9	IN_CLKp			Clock differential input
10	IN_CLKn			Clock differential input
29	OUT_D2n			TMDS data 2 differential output
30	OUT_D2p			TMDS data 2 differential output
26	OUT_D1n			TMDS data 1 differential output
27	OUT_D1p			TMDS data 1 differential output
24	OUT_D0n			TMDS data 0 differential output
25	OUT_D0p			TMDS data 0 differential output

21	OUT_CLKn			TMDS data clock differential output
22	OUT_CLKP			TMDS data clock differential output
3	HPD_SRC			Hot plug detect output
28	HPD_SNK			Hot plug detect input
39	SDA_SRC			Source side TMDS port bidirectional DDC data line
38	SCL_SRC			Source side TMDS port bidirectional DDC data line
33	SDA_SNK			Sink side TMDS port bidirectional DDC data lines
32	SDA_SNK			Sink side TMDS port bidirectional DDC data lines
36	OE		recommend that the capacitor to group is 200nF.	Operation enable/reset pin OE = L: Power-down mode OE = H: Normal operation Internal weak pullup: Resets device when transitions from H to L
34	SLEW_CTL			Slew rate control when I2C_EN/PIN = Low. SLEW_CTL = H, fastest data rate (default) SLEW_CTL = L, 5-ps slow SLEW_CTL = No Connect, 10-ps slow When I2C_EN/PIN = High Slew rate is controlled through I2C
16	PRE_SEL			PRE_SEL = L: - 2-dB de-emphasis PRE_SEL = No Connect: 0-dB PRE_SEL = H: Reserved Note: (3 level for pin strap programming, but 2 level when I2C address)
17	EQ_SEL/ A0			Input Receive Equalization pin strap when I2C_EN/PIN = Low EQ_SEL = L: Fixed EQ at 7.5-dB EQ_SEL = No Connect: Adaptive EQ EQ_SEL = H: Fixed at 14-dB When I2C_EN/PIN = High Address bit 1 Note: (3 level for pin strap programming but 2 level when I2C address)
8	I2C_EN/ PIN		use 65K resistor to pull up or pull down, do not leave floating.	I2C_EN/PIN = High; puts device into I2C control mode I2C_EN/PIN = Low; puts device into pin strap mode
13	SCL_CTL		pull up or pull down using 65K resistor.	I2C clock signal Note: When I2C_EN/PIN = Low Pin strapping take priority and those functions cannot be changed by I2C

14	SDA_CTL		pull up or pull down using 65K resistor.	i2C data signal Note: When I2C_EN/PIN = Low Pin strapping take priority and those functions cannot be changed by I2C
18	Vsadj			TMDS-compliant voltage swing control nominal resistor to GND
23	HDMI_SEL/ A1		pull up or pull down using 65K resistor.	HDMI_SEL when I2C_EN/PIN = Low HDMI_SEL = High: Device configured for DVI HDMI_SEL = Low: Device configured for HDMI (Adaptor ID block is readable through I2C When I2C_EN/PIN = High Address bit 2 Note: Weak internal pull down
11	VCC		needs one bulky cap + for each pin connected to VCC needs one 0.1uF capacitor. so total 2 .1uF and one bulky.	3.3-V power supply
37	VCC			3.3-V power supply
12	VDD		make sure is 1.1V needs one bulky cap + for each pin connected to VDD needs one 0.1uF capacitor. so total 5 .1uF and one bulky.	1.1-V power supply
19	VDD		make sure is 1.1V	1.1-V power supply
20	VDD		make sure is 1.1V	1.1-V power supply
31	VDD		make sure is 1.1V	1.1-V power supply
40	VDD		make sure is 1.1V	1.1-V power supply

Comments

The lanes used seem to be swapping, is this intended?

Cannot find datasheet for ESD. Please make sure that the working voltages and capacitances are HDMI1.4 compliant.

Cannot find datasheet for common mode chokes, make sure that the CMC bandwidth is within HDMI 1.4 spec.

1V1_SYS is going to 1.2VA. Is this as 1.1V or 1.2V signal. Need to be 1.1V

recommend using HPD gating as some monitor/ panels have HPD leakage.