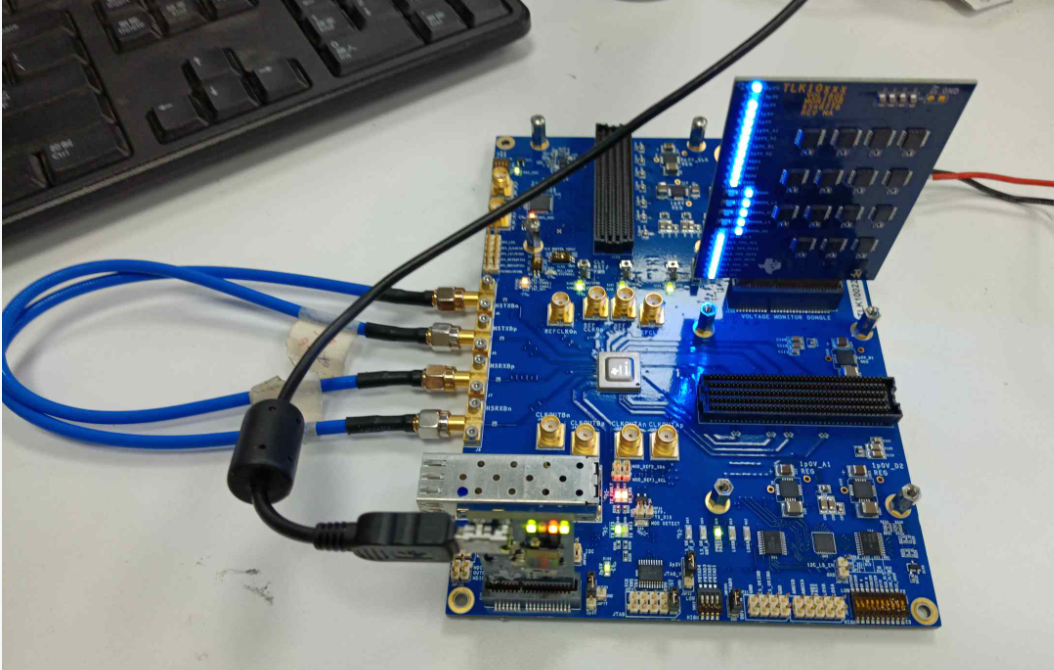
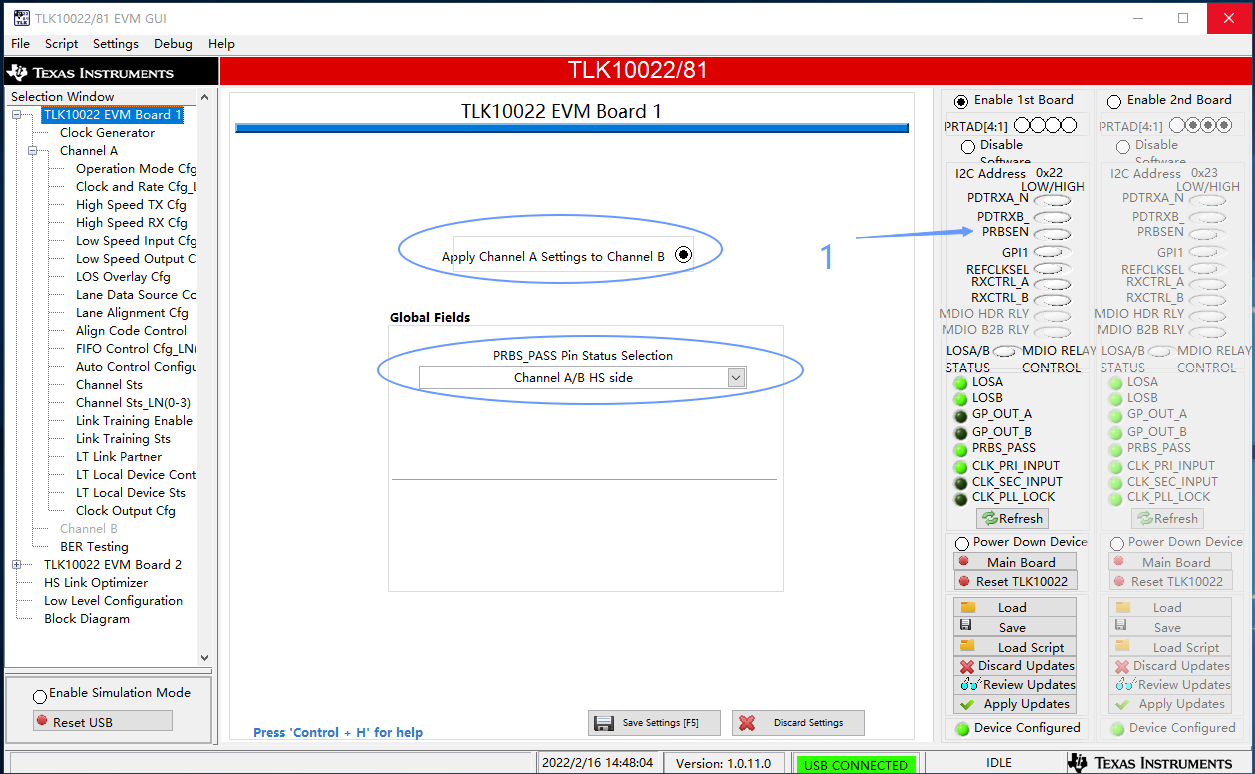
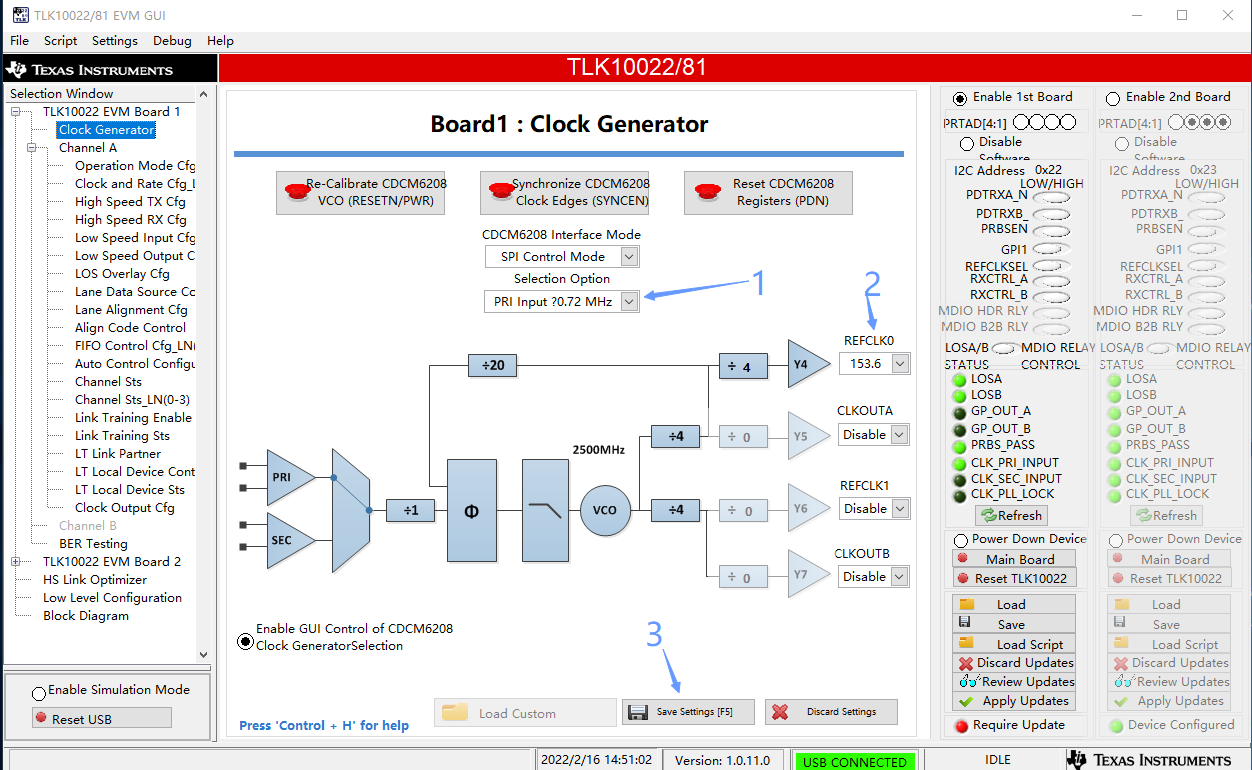
1. connect to EVM board, power on. And connect HS TX to HS RX by Blue Cable.



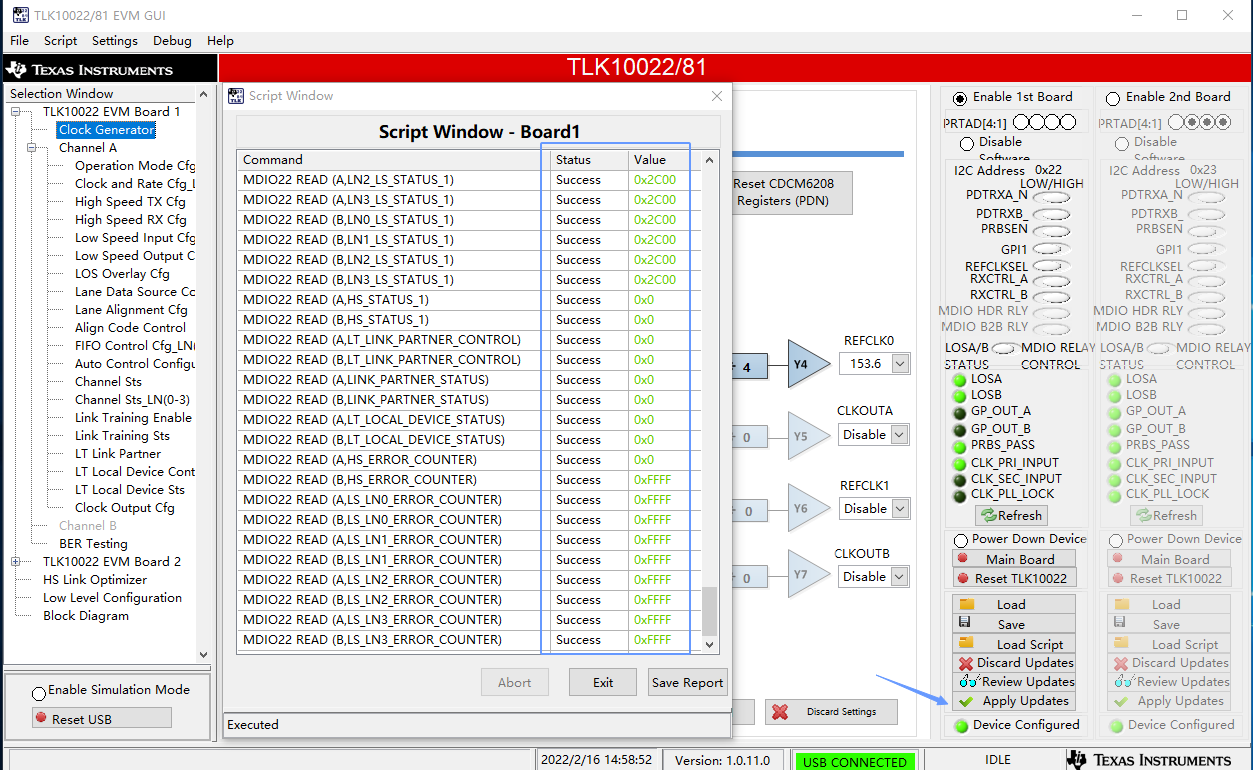
1. apply channel A to B, and PRBSEN turn high. Then save settings.



1. clock generator，select PRI Input? 0.72MHz, REFCLK0 153.6MHz

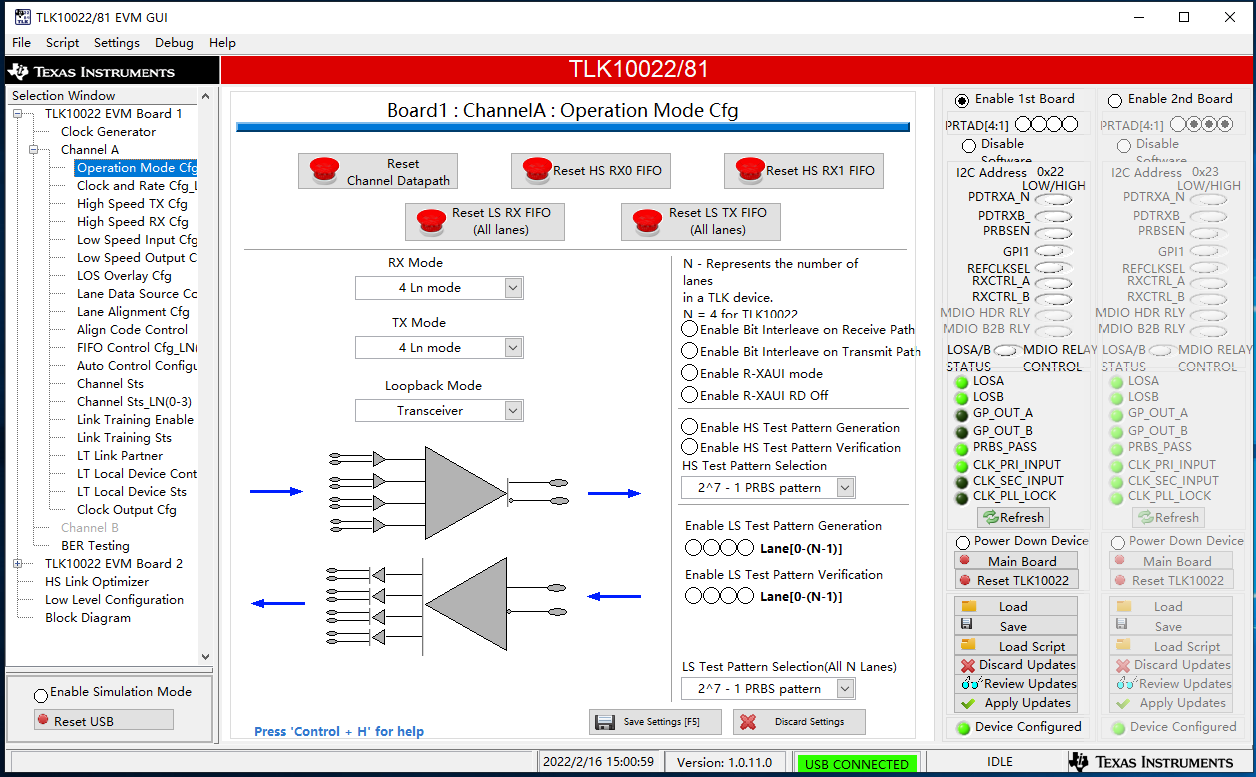


1. apply updates，and all success, and power from 5V\*1.55A to 5V\* 2.24A

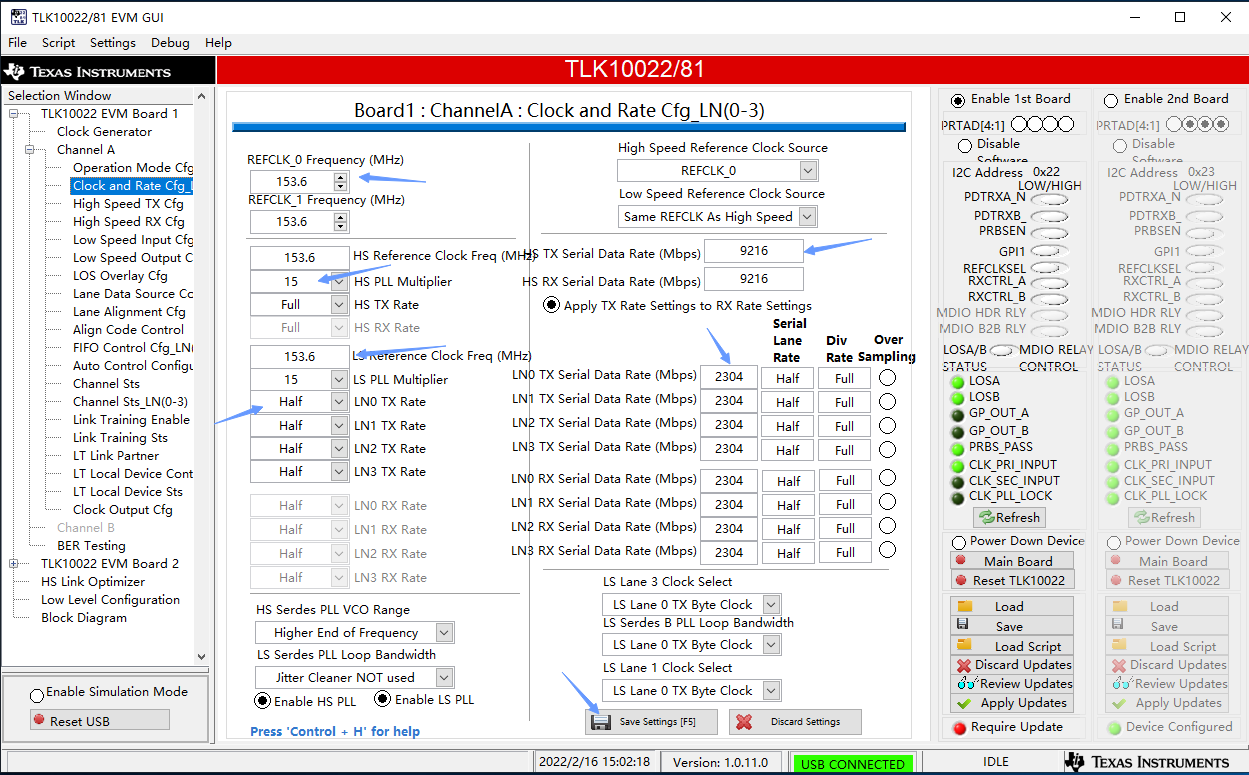


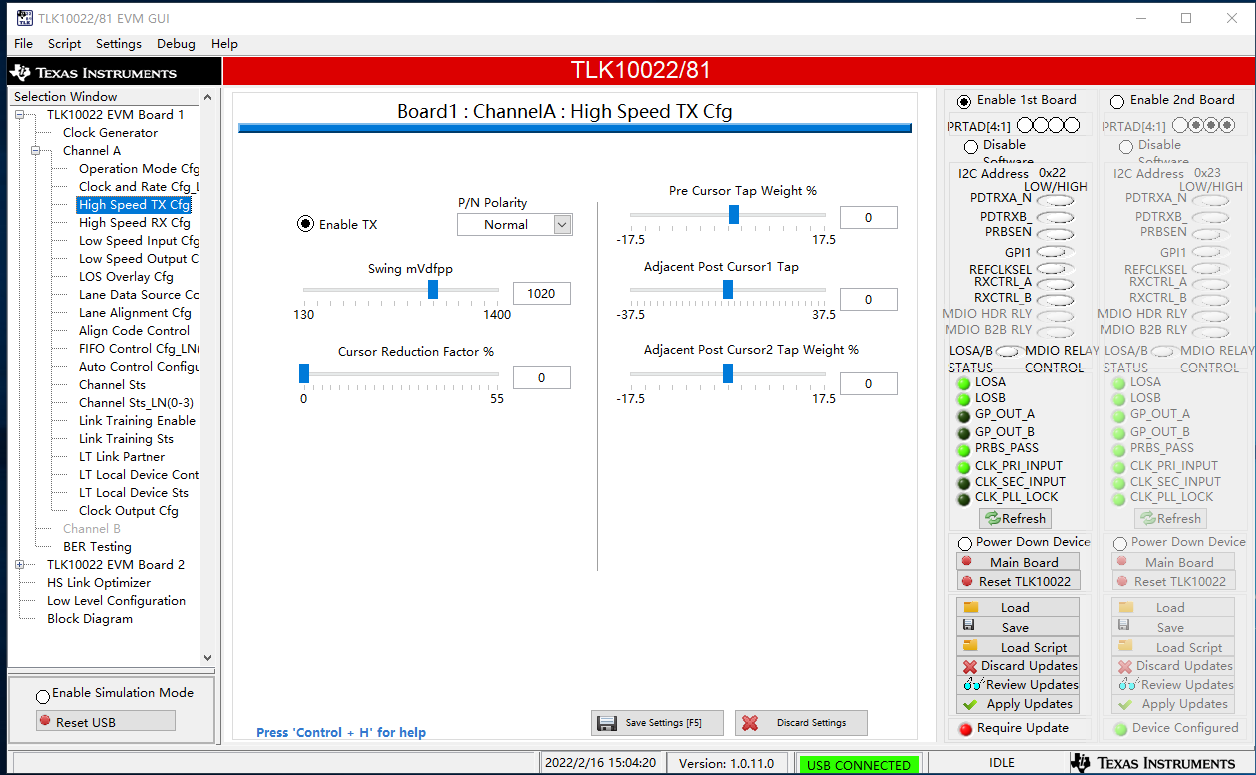
1. operation mode

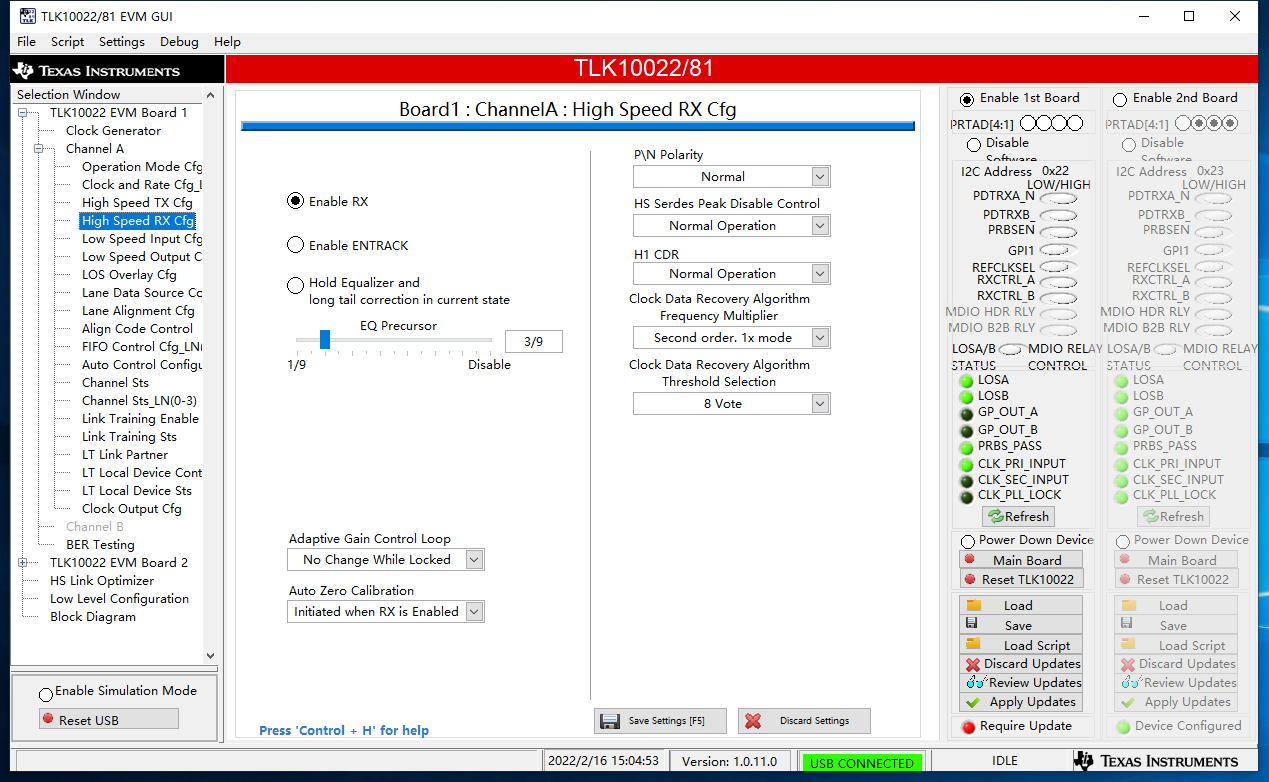


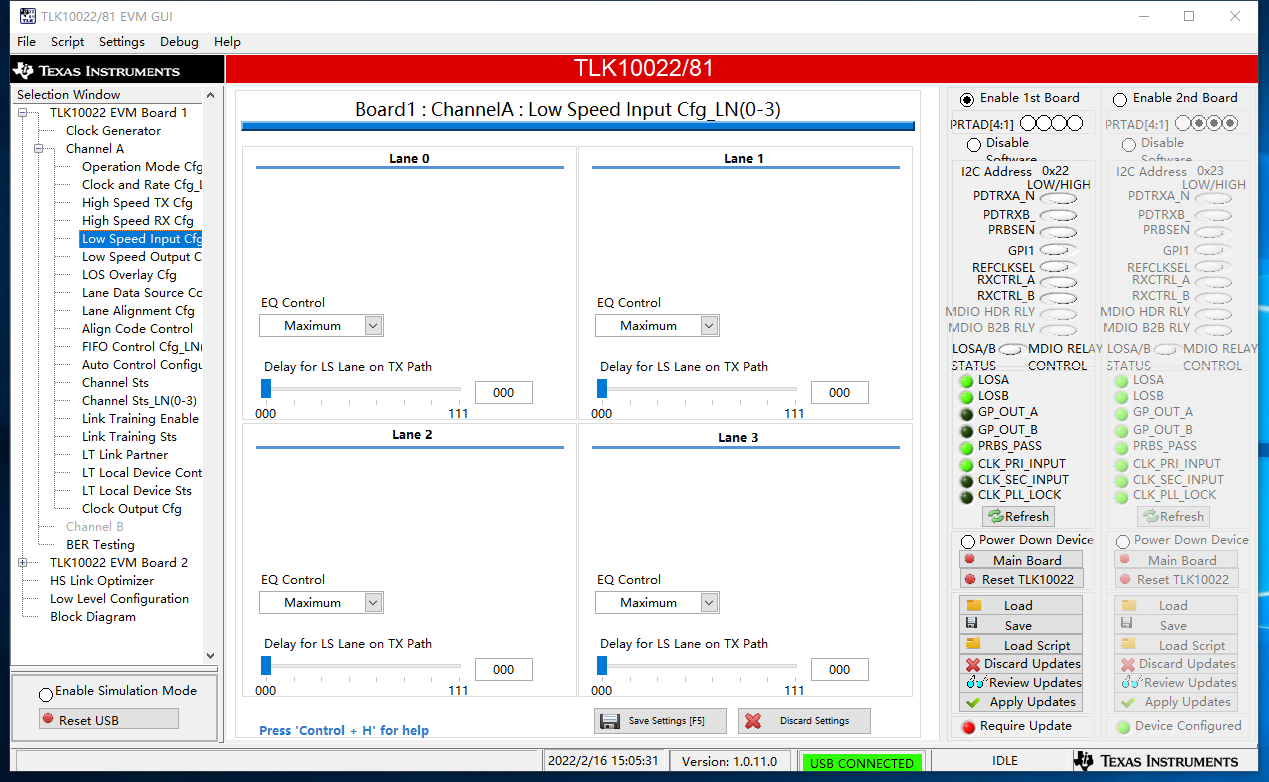
1. Clock and rate cfg , 2304M to 9216M, and save settings.

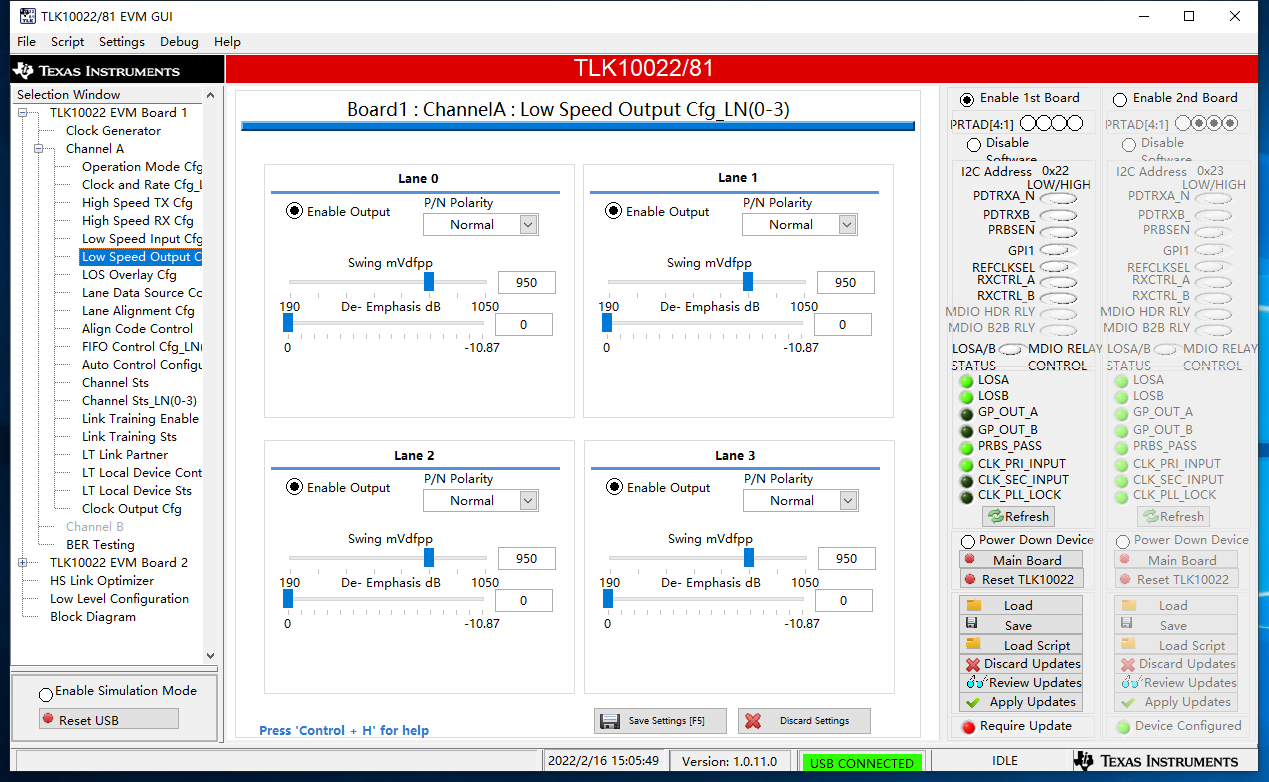


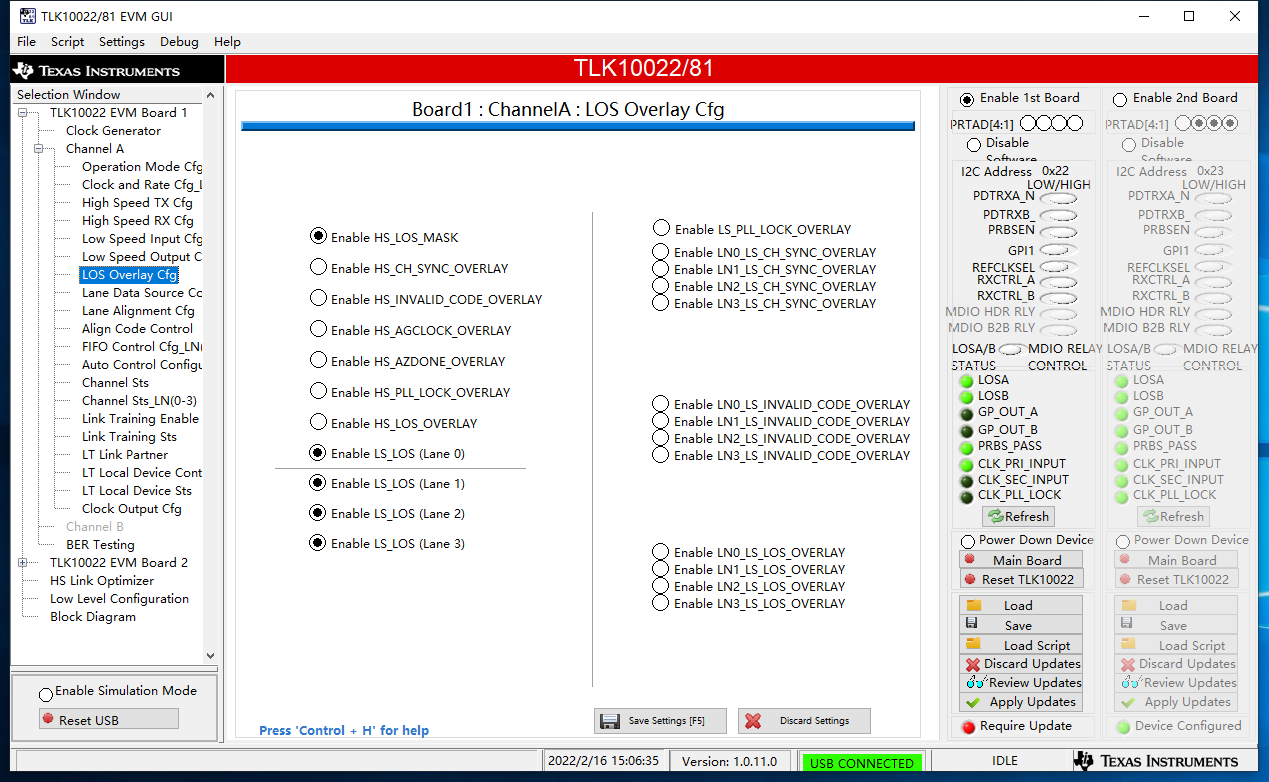
1. TX RX hs and ls CFG, not change



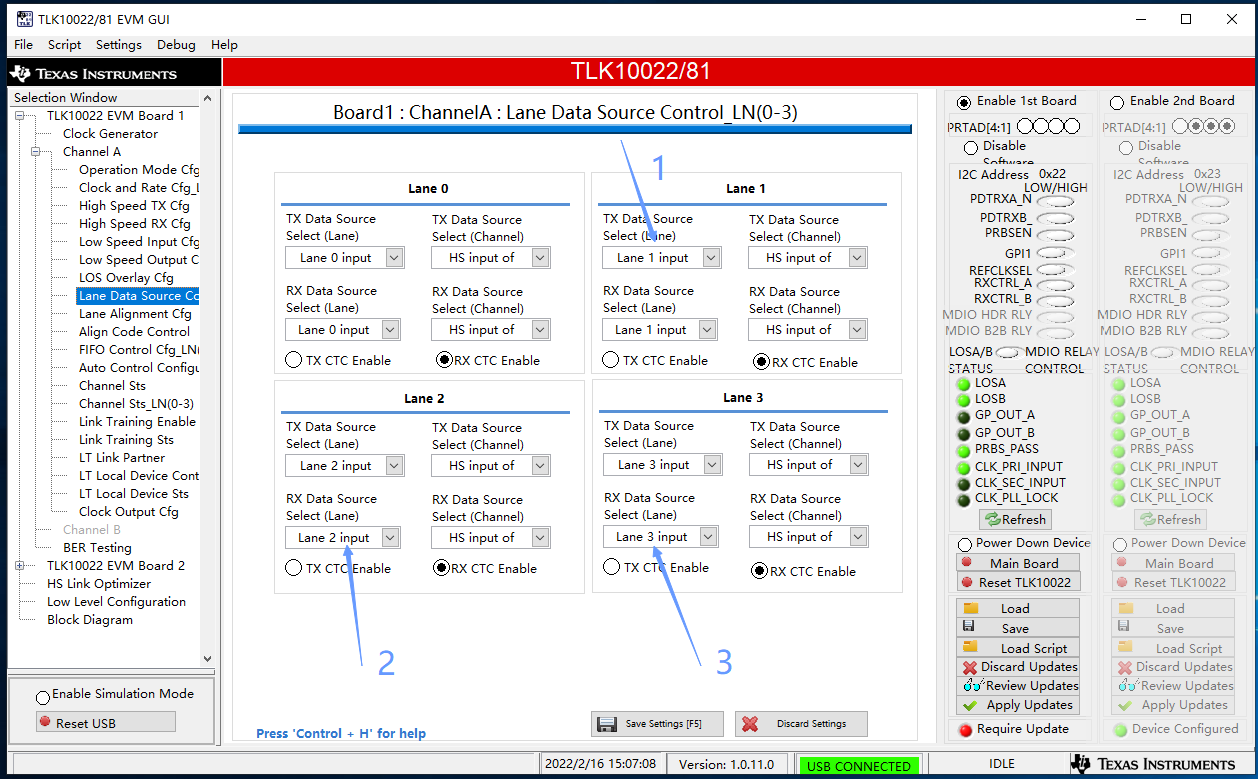




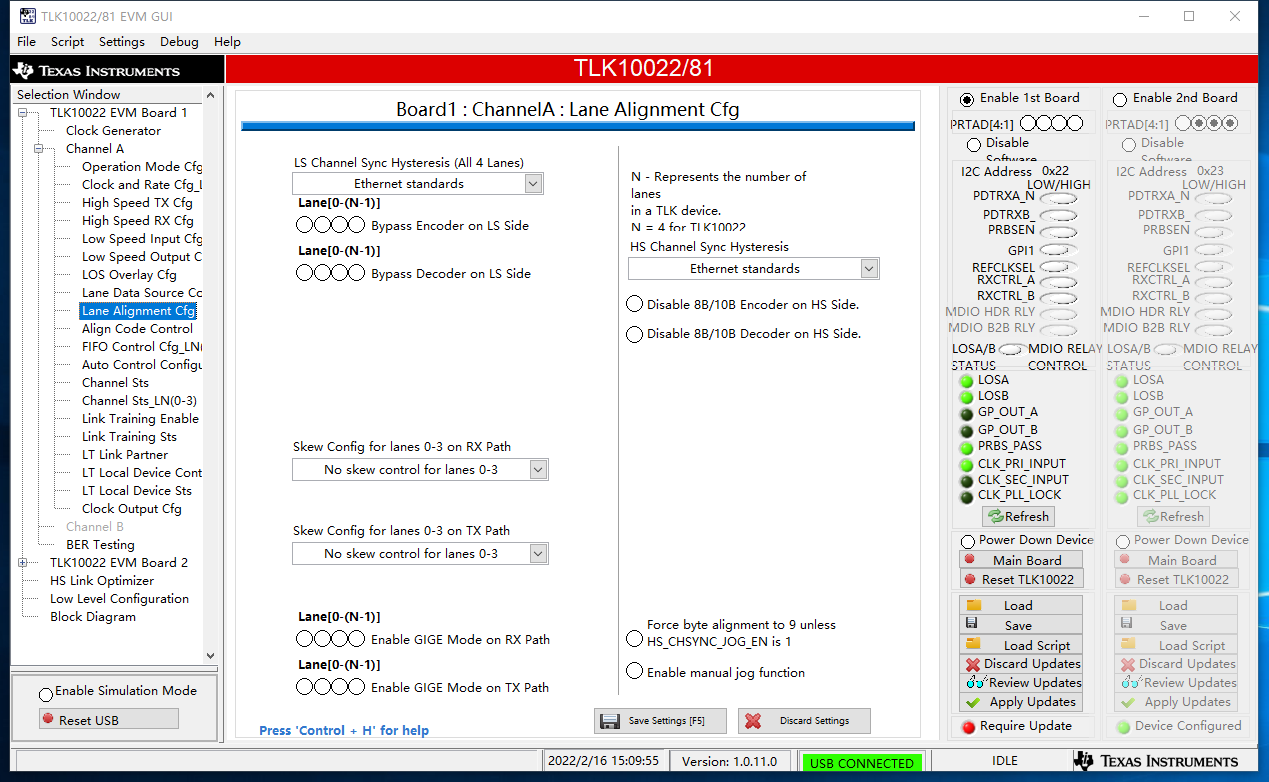


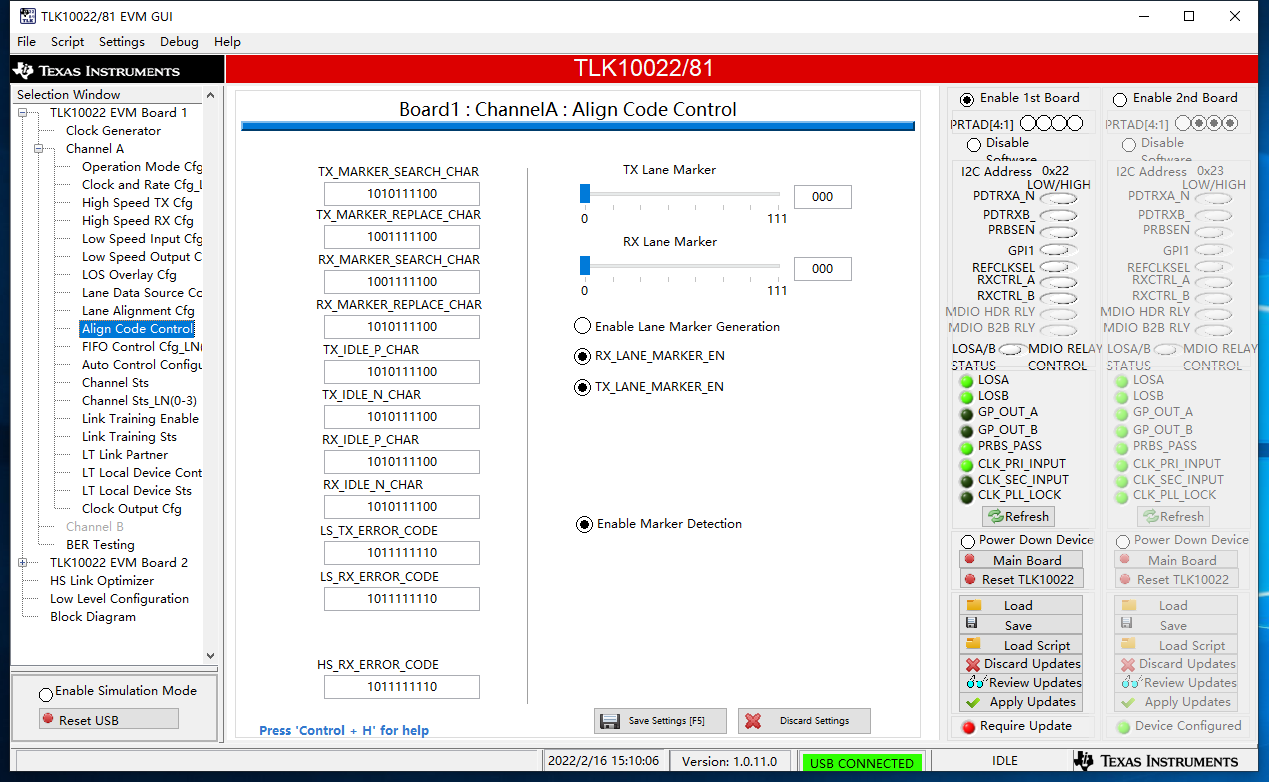


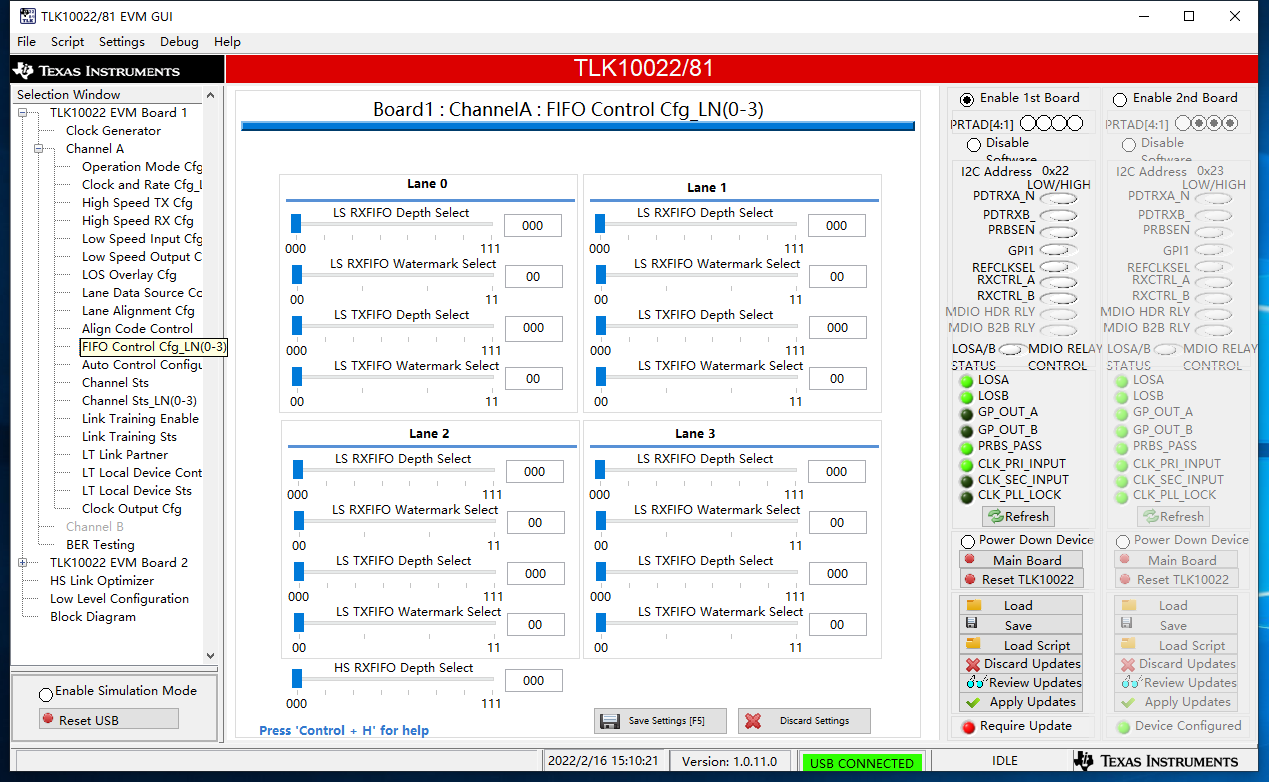
1. Lane data source control LN(0-3), lane1-lane1, lane2-lane2, lane3-lane3

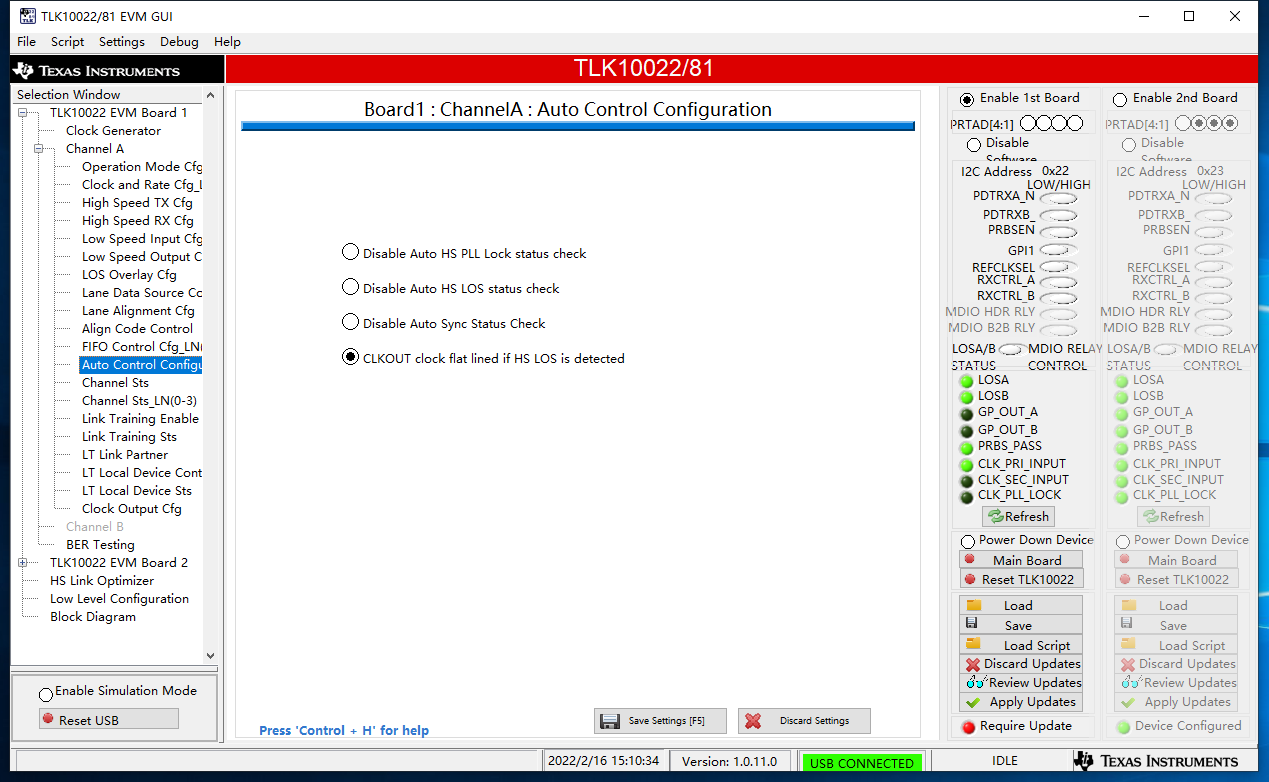


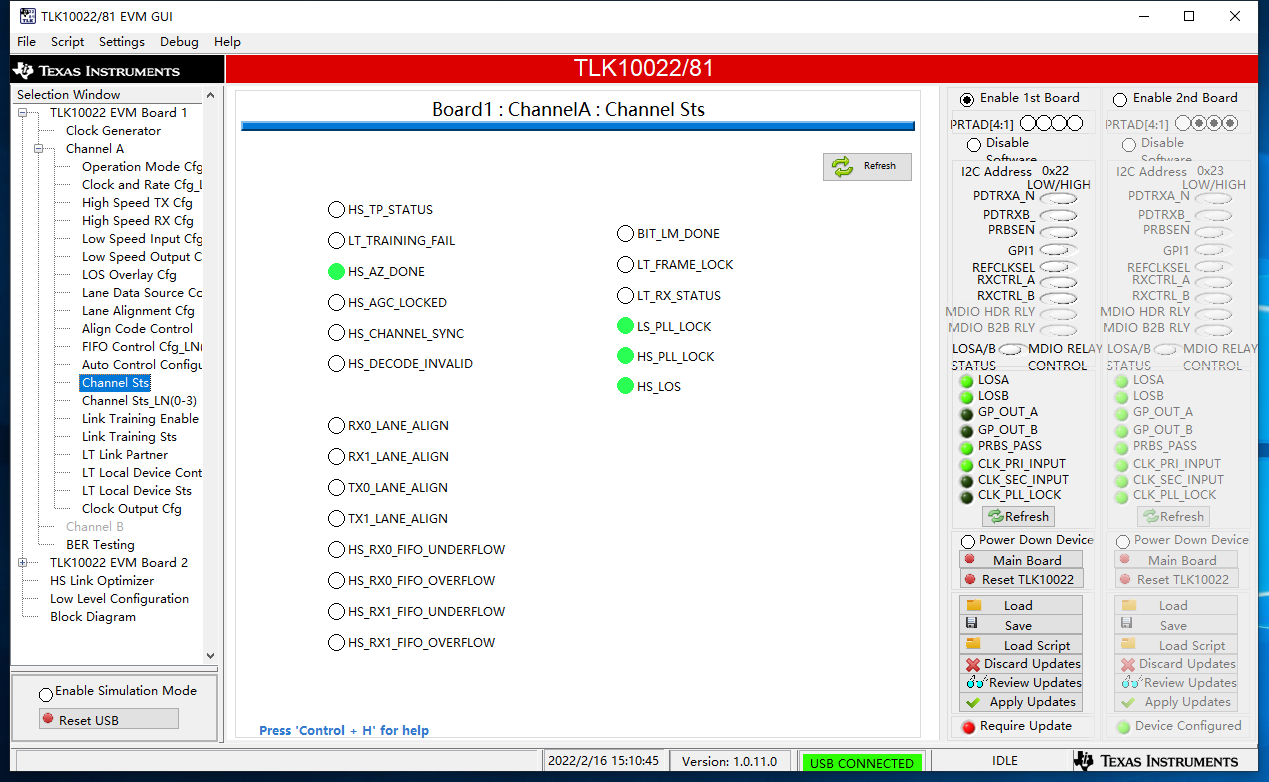
1. The rest is not change.

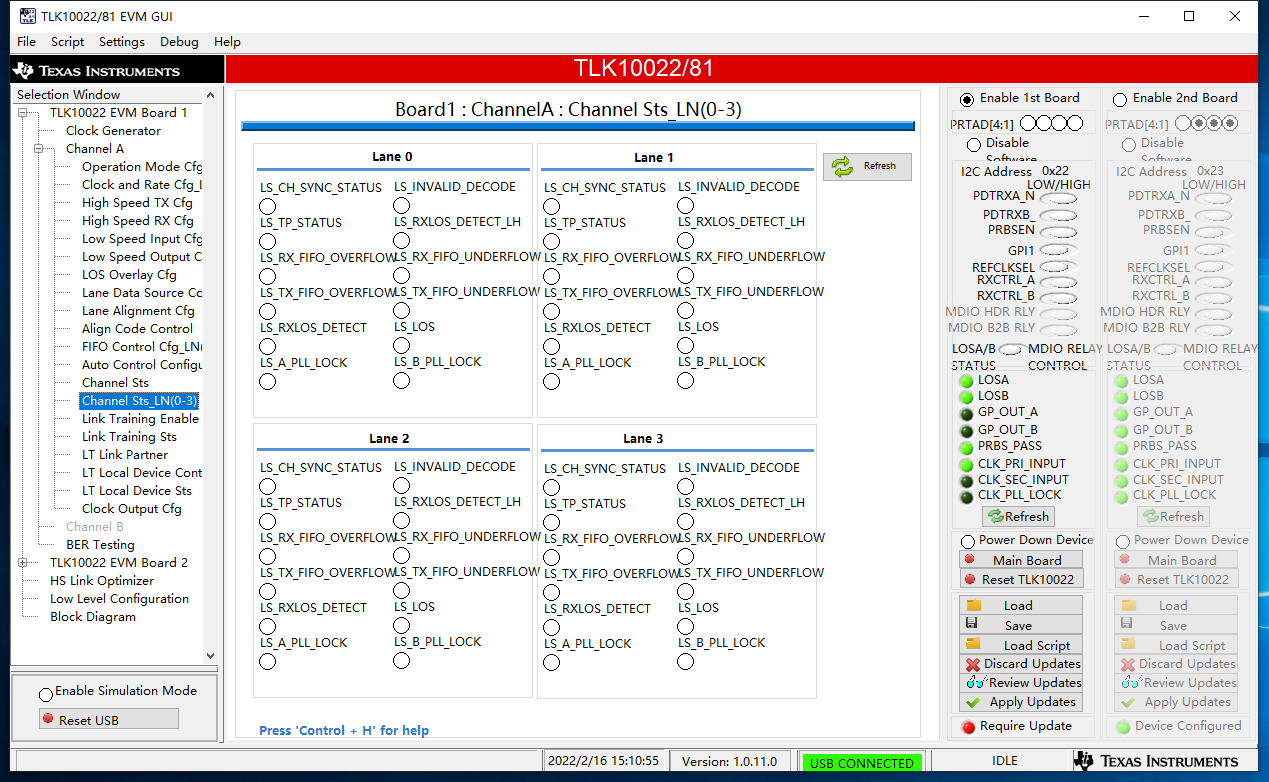
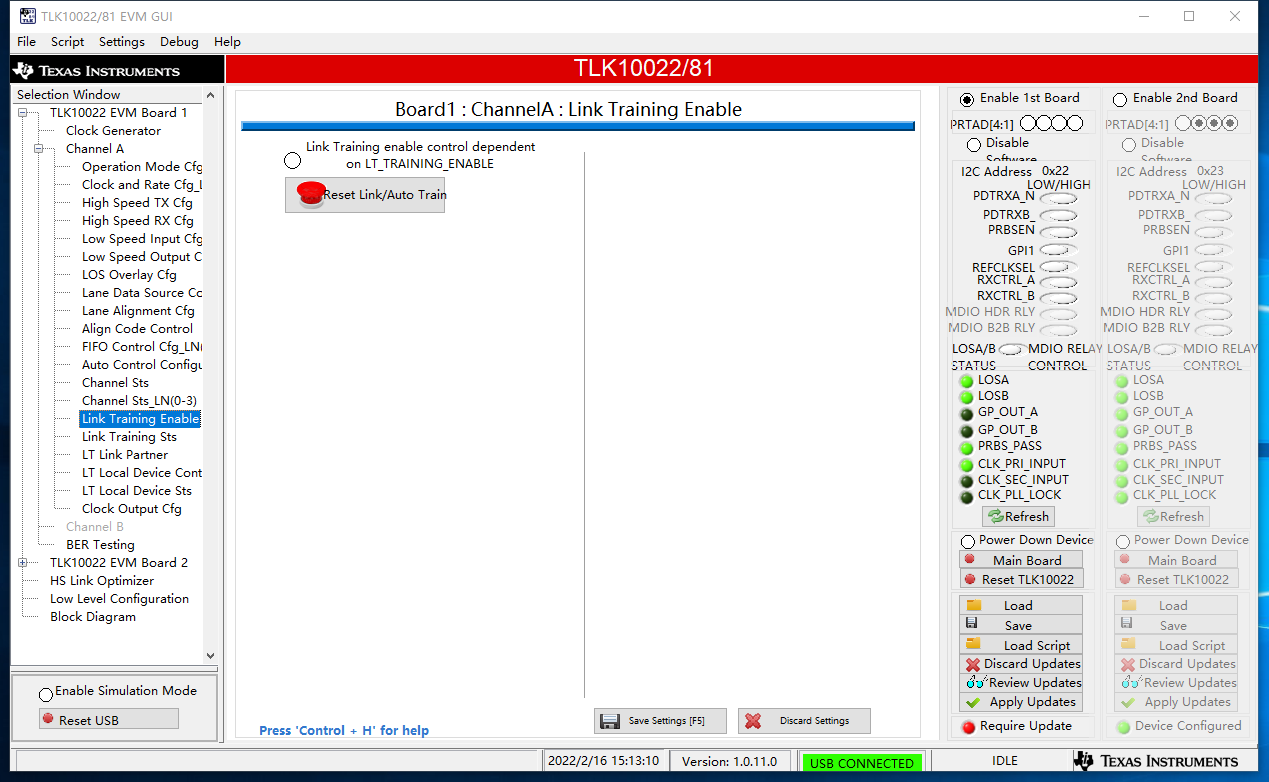


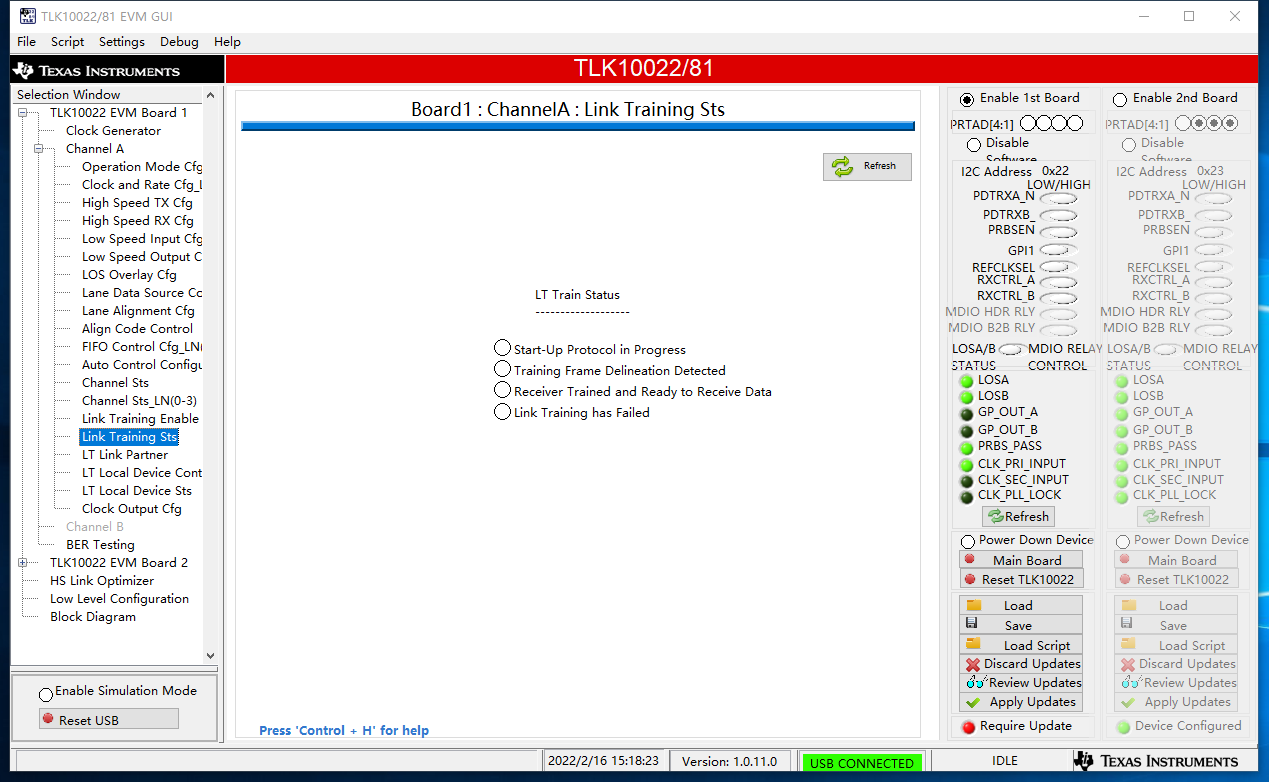


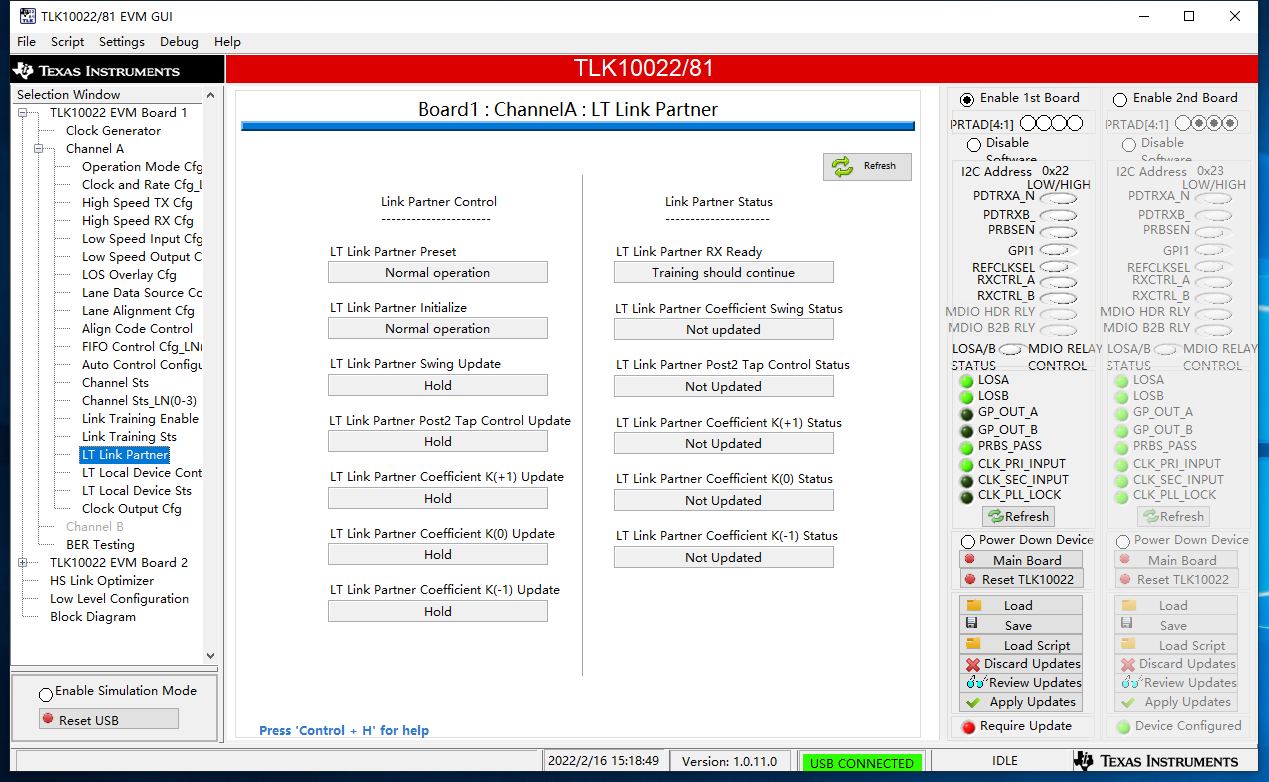


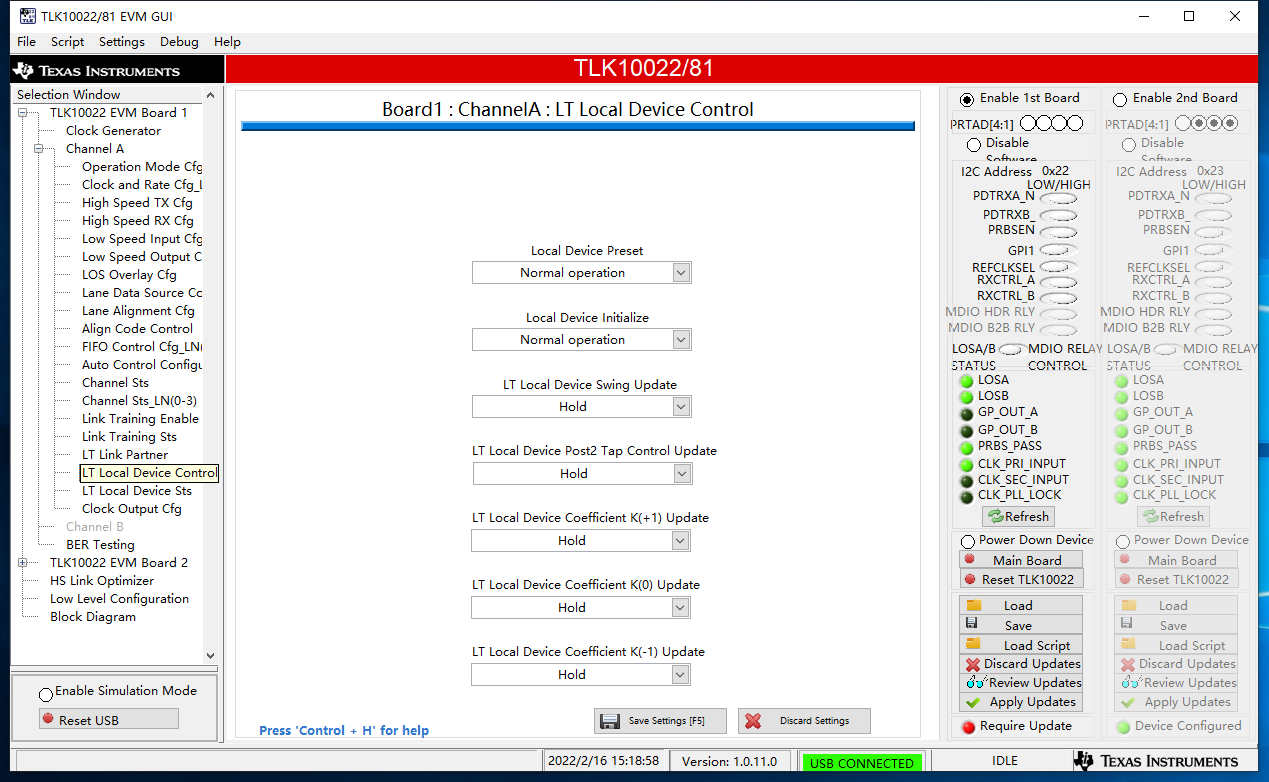


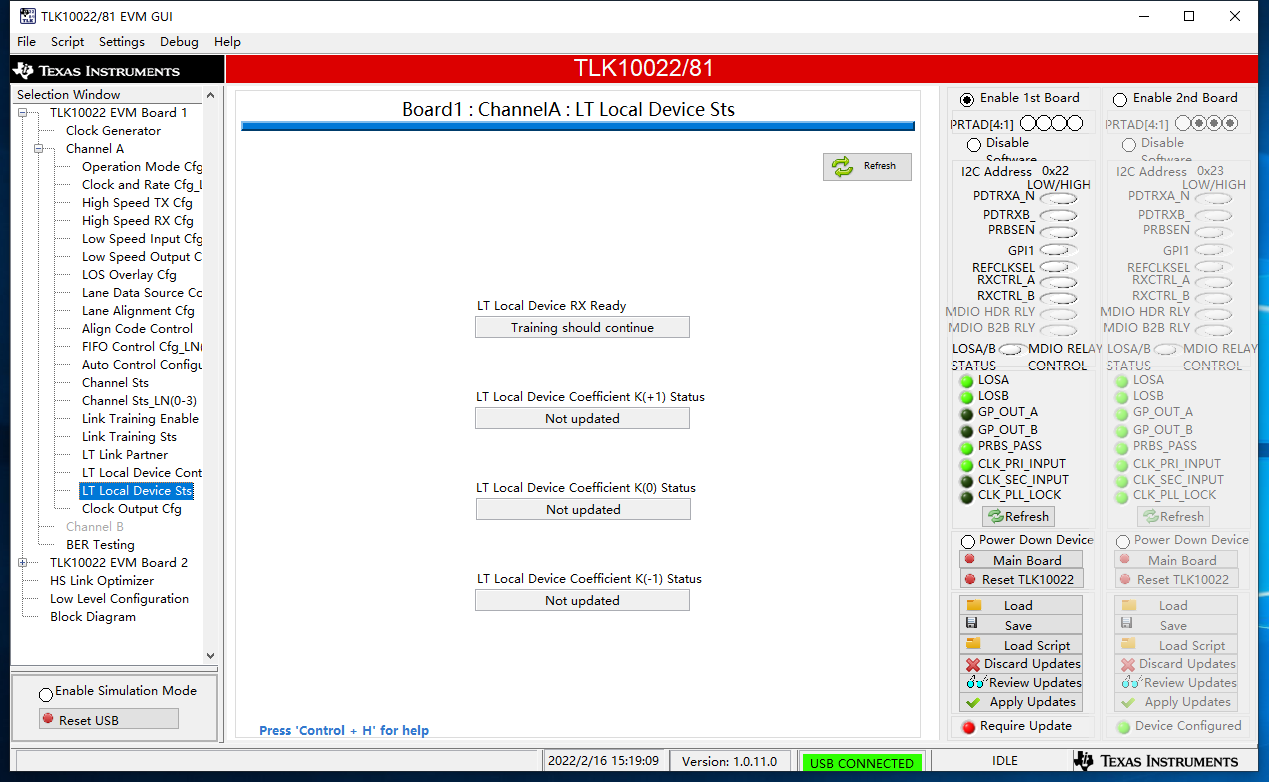


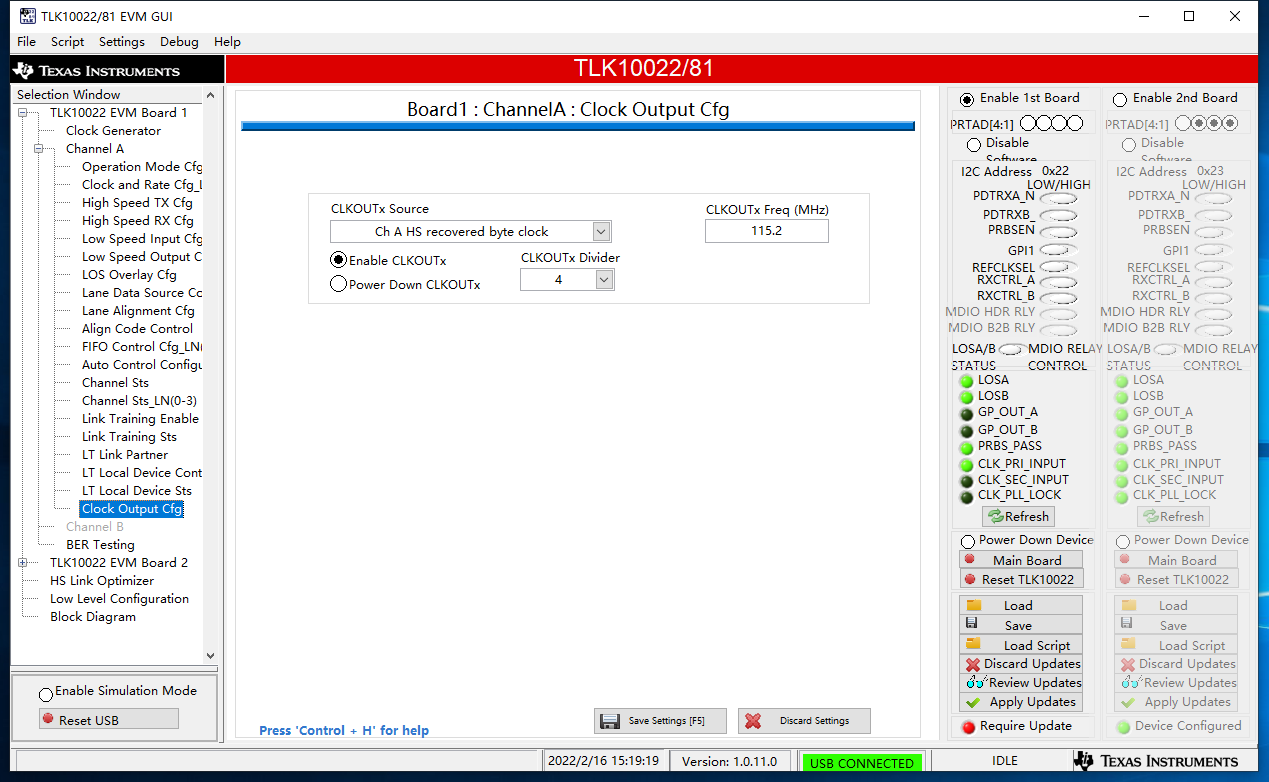
[[1]](#endnote-1)

1. 

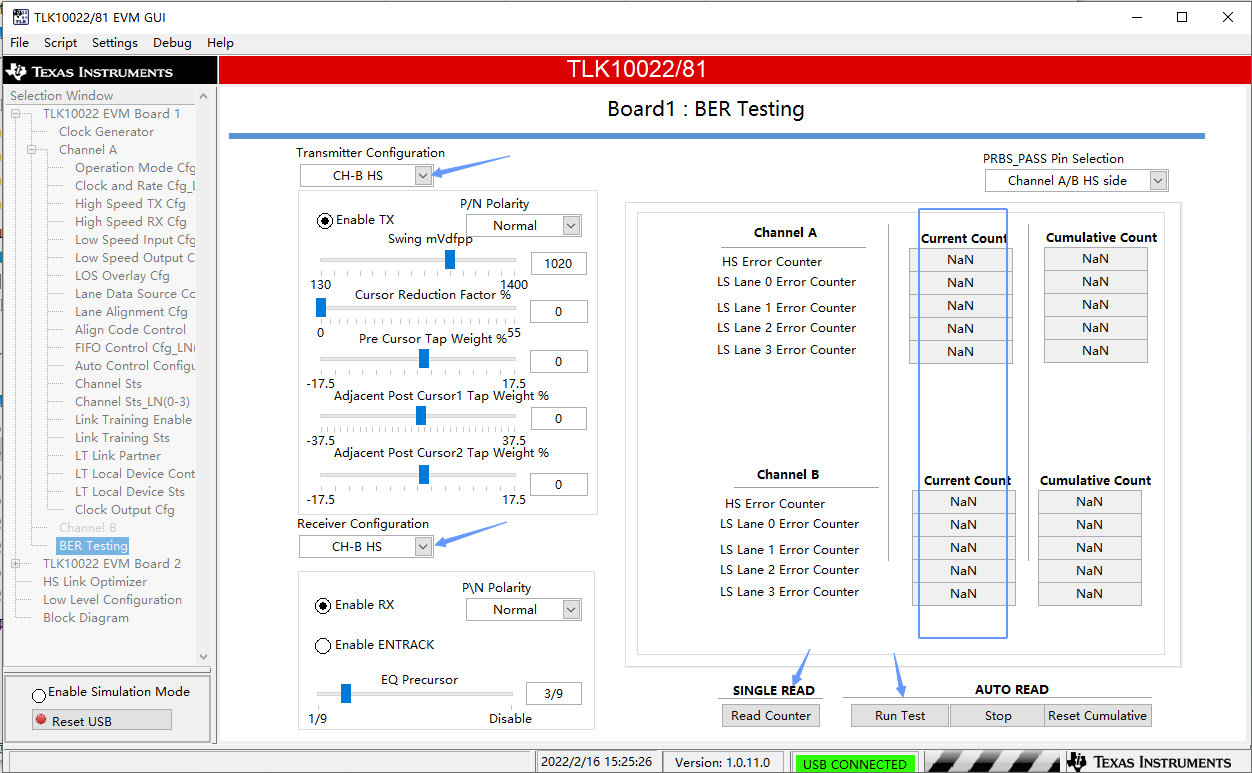
   

   And then, apply updates. And BER testing, NAN。。。,please tell me what’s the problem is? Thanks.

    [↑](#endnote-ref-1)